

# Adjustable PRPG for Low Power Test Patterns

B. Nadimulla, S. Aruna Mastani



**Abstract:** As the power consumption is more in the processes of testing, test vector set compression and controlling of toggling plays a crucial role in reducing the power consumption during test mode. In exploring the controlling techniques of toggling, Pre-Selected Toggling (PRESTO) of test patterns is a technique that can control the toggling of a test patterns in a precise manner in Built-in Self-Test (BIST) architectures. In this paper we modify the architecture of existing Full Version PRESTO that can be used to generate test vectors and in addition binary sequences used as scan chains such that the controlling of sequence of test vectors depends on number of 1's present in the switch code which is user defined thus reducing the testing time with significant fault coverage, and in addition the optimization is also observed in area and power. The area has decreased by 12.2% and power consumption by 15.43%. The Synthesis and implementation of the architectures are done using Artix7 (xc7a100tcs324-3) FPGA family. The simulation results have been analyzed through Mentor-graphics Questa-sim 10.7C.

**Keywords:** Pseudo Random Pattern Generator (PRPG), Linear Feedback Shift Register (LFSR), Pre-Selected Toggling (PRESTO)

## I. INTRODUCTION

The test vector compression concept introduced long back, has become popular in Designing for Testability (DFT) technology. An another DFT methodology that gained acceptance rapidly is Built-in-Self-Test (BIST) methodology. Due to advances in technology that results in small feature size much complex systems are fabricated on a chip has resulted in a hybrid technique of merging BIST (built-in-self-test) with Test compression.

In the evolution of test compression techniques with the BIST some of the LFSR (Liner Feed Back Shift Register) encoding techniques such as LFSR coding [1], LFSR reseeding [2],[3] and Dynamic LFSR Reseeding [4],[5] are evolved. In the above techniques the LFSR's are encoded in such a way that they can deliver a compressed test data.

In the hybrid schemes and scan-based testing, test compression plays a significant role as high volume of data is associated in the testing process that draws more power compare to circuit in its functional mode. This is due to the high toggling rate of patterns that are applied to the circuit as stimulus. This over stressing of the circuits in the processing of testing may result in the thermal issues, voltage noise,

excessive peak power over multiple cycle switch, power droop that may lead to instant device damage.

In exploring some various low power techniques there are solutions to keep the BIST to an average peak power below the threshold [6] and some power aware BIST solutions as in [7], [8]. Some of the techniques in [9] consist of the linear feed-back shift register to feed scan chains through a logic which is biasing a T flip-flop which hold the previous value when input becomes one. The LFSR [10] of dual speed with two clocks for low speed and high speed generate a different way of low switching patterns with significant fault coverage. Especially for huge test data used in scan-based techniques of BIST. Gated scan cells are proposed in [14] in which gates are added at each cell to control the switching activity. An inhibiting scheme [16] was designed for an LFSR which produces a very lengthy test vectors which detect faults. Reducing of such lengthy test vectors sets will reduce the

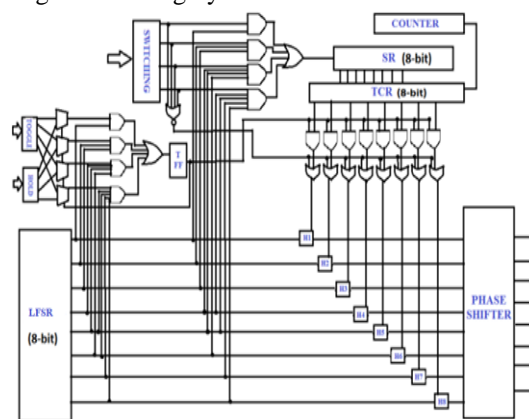


Fig.1 Full version PRESTO architecture

A new approach of producing binary sequences (Test patterns) with Pre-selected Toggling activity through controlling of PRPG is introduced by Michel Filipek, Grzegorz Mursalski Et al. [11],[12] in 2015. This technique is based upon the controlling the toggling rates by switch codes using additional hardware in fine tuning the test vector generator for improved fault coverage to test pattern count. This paper suggests a modification to the existing architecture for PRESTO thus increasing controlling capability of toggling yet reducing the Area and also the power.

## II. FULL VERSION PRESTO ARCHITECTURE

The Full version PRESTO (Pre-selected toggling) architecture was investigated by Michel Filipek, Grzegorz Mursalski Et al. [11][12] as shown in fig.1, it is a low power programmable test pattern generator with controllable toggling rates to produce desired binary sequences.

Manuscript received on March 06, 2020.  
Revised Manuscript received on March 18, 2021.  
Manuscript published on March 30, 2021.

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## Adjustable PRPG for Low Power test Patterns

This aims to reduce the switching activity in scan loading due to its Pre-selected toggling. This generator has variety of configuration that allows the given scan chain driven by either PRPG itself or by a value driven constantly for a period of time.

By using this, power dissipation can be significantly reduced and it allows fully selection of controls which results in test pattern feature with user defined toggle rates. This PRESTO has an additional feature of combining BIST with ATPG – based embedded test compression.

This Test compression scheme is first of its kind integrated in every way with the BIST environment. In addition to reduce the structural dependency of patterns, the fine-tuned test patterns are passed through a phase shifter

[13] whose outputs drive the multiple scan chains in an BIST approach. Overall, it is a PRPG for LP-BIST that aims at reducing switching activity during scan loading by pre-selected toggling levels. As seen from fig.1 the output of LFSR is fed through hold latches which are controlled by external hardware that consists of the weighted logics of AND structure, MUX structure and TCR (Toggle-control

register) and a shift register. This allows selecting a user-defined level of switching activity and thus the expected toggling ratio with wide-range of desired switching rates.

Though it has many features of controlling the PRPG, yet there is a scope to reduce the hardware required for controlling the switching activity and also avoiding the chance of enabling all the hold latches that leads to more switching activity. The detailed explanation is in the upcoming section.

### III. PROPOSED ARCHITECTURE

The Proposed architecture for PRESTO in a BIST environment is shown in fig.2. PRESTO is an additional circuitry to the LFSR which is used to generate the controlled test patterns through toggling of latches. This hardware is optimized in area and power than the existing Full- version PRESTO architecture by replacing weighted AND block and MUX block with Circular shifter register and a down counter.

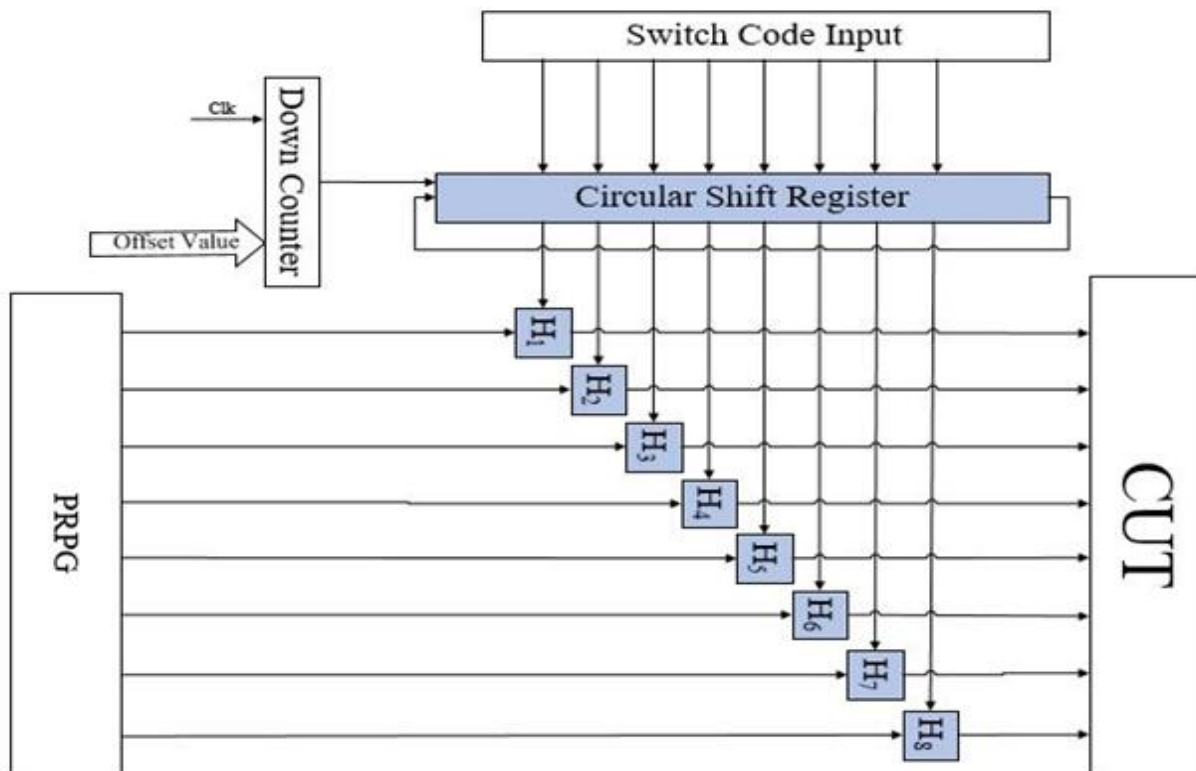


Fig. 2. Proposed PRESTO Architecture

The basic concept of PRESTO is to control the switching activity in the test patterns so as to generate desired pattern sequences. This is made through latches from the fig.2 which are controlled as per user defined requirement. The Circular shift register is n bit register with parallel-in-parallel-out functionality. Parallel in is a user defined n-bit switch code and parallel out are fed to the hold latches which acts as enable signals transparent for data to move from PRPG to the circuit under Test. This circular shift register will generate the number of combinations based upon the switch code by Right shifting the data for each cycle. The switch code selected can control the number of 1's in the output patterns.

i.e. if the switch code has only two 1's for example, if switch code is 10100000, the toggle rate is of 25%. Here toggle rate refers to number of 1's in the pattern to total number of bits in the pattern, thus all the output patterns generated will have either at max two 1's. Hence the number of 1's in the output patterns can be controlled through selection of appropriate switch code that generate appropriate percentage level of toggling. This enhances the control over switching activity,

thus generating test pattern sequences that leads to low dynamic power. This controlling capability helps to achieve maximum fault coverage to pattern count ratio. Desired pattern sequences up to a given offset value can be generated by adjusting the offset value of the counter. Phase-shifter can also be combined at the outputs of hold latches to reduce the structural dependency problem.

If the user wants to turn off the toggling control of latches then a switch code of 11111111 is given to switch code register. For more understanding of this architecture the processes of working are explained through an example.

Table. 1. Comparison of Full Version PRESTO with the Proposed PRESTO Architecture

ARCHITECTURE	#LUT	POWER(W)	#FF	FREQUENCY(MHz)
Full-version PRESTO Architecture	49	0.149	50	628
Proposed PRESTO Architecture	43	0.126	41	628

In this architecture there are mainly three user defined inputs they are the switch code, the offset value to the counter and the LFSR seed value. For example, if an 8 bit LFSR is considered with the generating polynomial as  $x^8 + x^5 + x^3 + x^2 + x = 1$  and seed value as 10110010. Then the output of LFSR is fed to the hold latches. The circular shift. The circular shift register in the architecture will perform parallel-in-parallel-out functionality in which the parallel in will be the user defined switch code of 8 bit

The switch code driven to the circular shift register is 10010000, as we can notice there are only 2 ones in the switch code in which it will enable the 1<sup>st</sup> and the 4<sup>th</sup> Hold latches. The values that are present in those two latches will be transparent to move the data from the LFSR to the circuit under test. In the second cycle the switch code is right shifted i.e., 01001000 thereby enabling 2<sup>nd</sup> and 5 the latch thus allowing data from the LFSR to the output. Then the 2<sup>nd</sup> and the 5<sup>th</sup> latches will be enabled and the data present in those latches coming from the LFSR will be driven to the circuit under test. This process goes on generating the user defined test patterns up to offset value of the down counter.

compared with Full version PRESTO Architecture. Both the present and proposed architectures are of 8-bit designs, the architecture can be further designed for 32 or 64 bits. Coding has been done in Verilog VHDL.

IV. RESULTS

Synthesis and implementation of both proposed and existing architectures are done using Artix7 (xc7a100tcs324-3) FPGA family for making apt comparison with respect to area and power. The controlling activity of the architecture can be interpreted from the fig.3 which shows the patterns generated by the two. As Proposed architecture controls the number of 1, s in the pattern in contrast to no predefined control in the existing architecture, the pattern sequences can be made user defined thus reducing the dynamic power as Tabulated below and shown in Fig 4 and 5 as Bar graph representation. Fig 6 and 7 shows the Schematic of both the present and Proposed architectures by which we can visually observe the area difference in both the schematics.

The Efficiency of the proposed architecture is also compared with respect to Area and Power. The percentage reduction in area and power is taken in terms of decrease in number of LUTs and reduction in power respectively are defined below

$$\%Decrease = \frac{Intital\ value - final\ value}{/Initial\ value/} \times 100$$

By this above formula we can say that there is a decrease of 12.2% in terms of Area and 15.43% in terms of power when

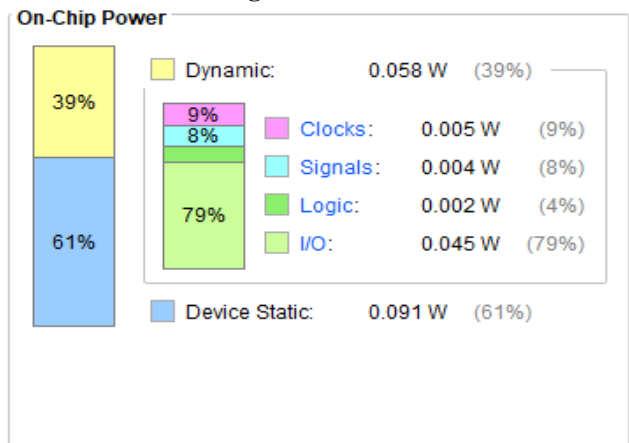


Fig.4. Power report of full version PRESTO Architecture

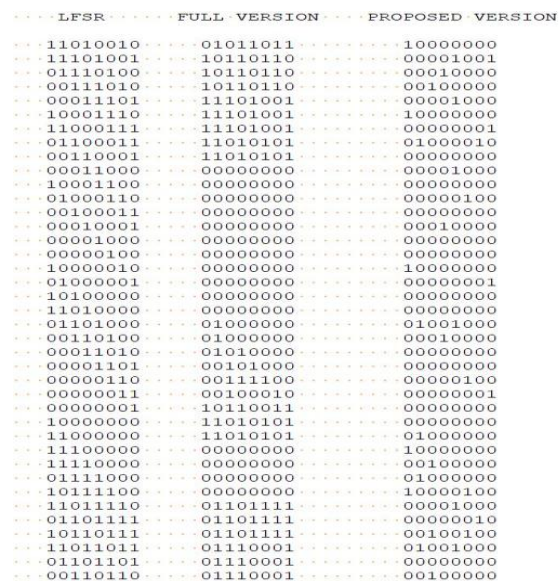


Fig.3. Output patterns of LFSR, Full version PRESTO and Proposed Architectures

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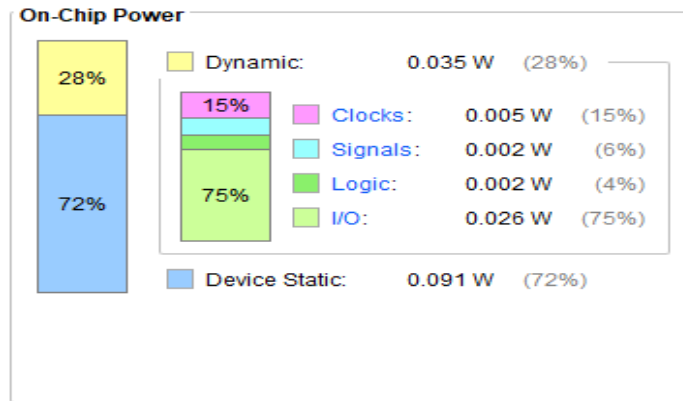


Fig. 5. Power report of Proposed PRESTO Architecture

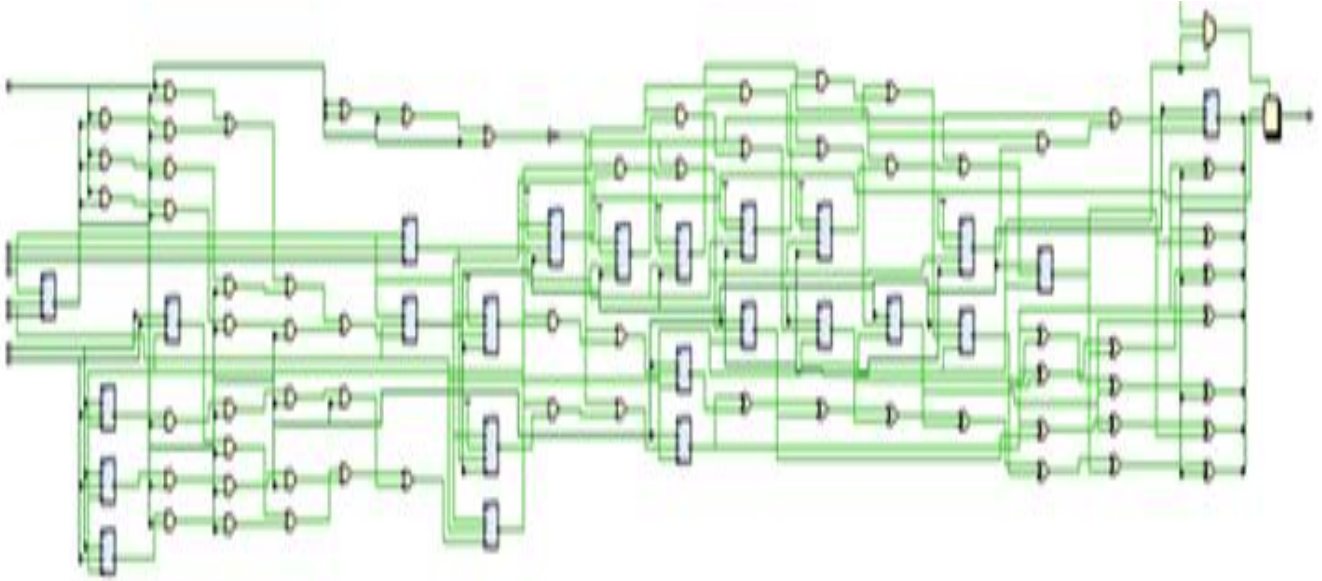


Fig.6. Schematic of full version PRESTO Architecture

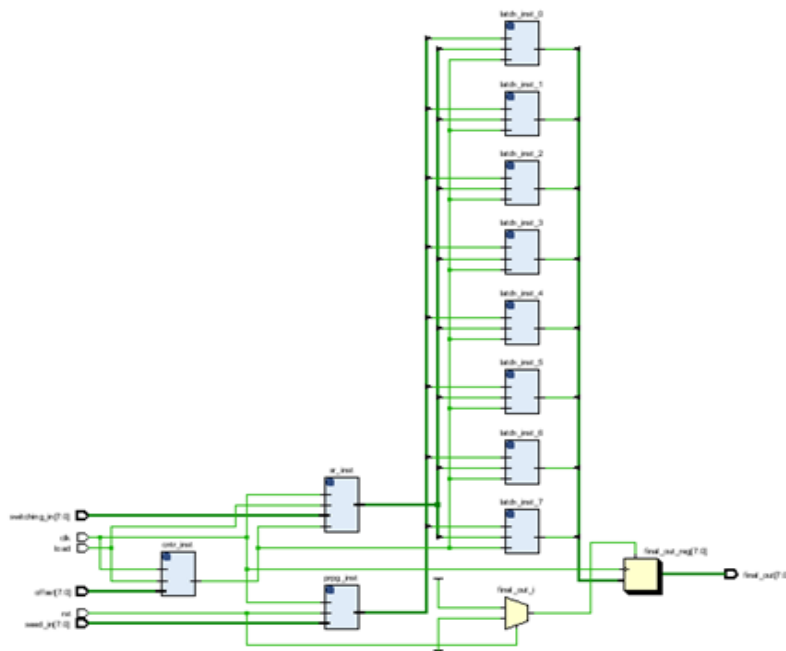


Fig.7. Schematic of Proposed PRESTO Architecture

## V. CONCLUSION

In this paper, a modified PRESTO architecture is proposed by maintaining the same functionality of controlling toggling of the patterns. By this there will be a significant control in the number of 1's so that the dynamic power will be decreased that impacts the power envelop in terms of testing of a circuit. Furthermore, there is a decrease in architectural Area and Power which yields to better results. By this we can conclude that by using the proposed architecture for test pattern generation there will be significant decrease in the switching activity, due to which the thermal issues and Damage of circuit in the test mode can be significantly reduced.

## ACKNOWLEDGMENT

I would like to thank my guide Dr. S. Aruna Mastani, Assistant Professor, at Jawaharlal technological university Anantapur, for giving me this Opportunity and helping me to complete my project work till the end.

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