

Complicity of High-End SOC-FPGA's for Data Centers



Retikal Anil Kumar

Abstract: As the network traffic increasing significantly due to increase in Data streaming, Big Data Analytics, Cloud Computing, Increasing the load on Data Centers, Which leads to demand for high computational capabilities, low latency, high-bandwidth, power efficient data accelerators. As Re-Configurability of FPGA's are more flexible for developing customized applications, so the FPGA hardware based data accelerators are the potential devices to achieve low latency and power efficient requirements. The modern FPGA's are coming up with the embedded communication hard IP's like PCIe, Ethernet, & DDR based memory controllers, which makes easy for the deployment of network attached FPGA's in data centers. This paper presents the role of FPGA's in datacenters and analysis of high-end FPGA's by various vendors, which are suitable for deployment in data centers.

Keywords : ASIC, Data Center, FPGA, Re-configurable logic, EFPGA, Big Data Analytics, Cloud computing.

I. INTRODUCTION

The growth of embedded system & IoT is in such a way that in nearby future every electronic device in the world will connects to Internet to manage/operate many things. Due to which network traffic will also increase as the increase in Audio Video data streaming, data managing, controlling devices over Internet. Therefore, the load on the data centers increasing rapidly according to the article "Cisco Visual Networking Index: Forecast and Trends" by 2021 the Annual global IP traffic will reach 3.82ZB per year or 319EB per month. Among the total traffic, the traffic from the mobile and wireless devices will be around 71 percentage of total IP traffic. 5G also expected in the market by 2021, by 5G enabled devices the speed of the devices for data accessing, Uploading and downloading will be higher than the current speed. These all factors making the requirement of very low latency, High bandwidth, high throughput and high computations capable for offloading devices at data centers.

The conventional data centers uses the CPU & GPU based data accelerators, recently from past 2-3 years high-end FPGA's are became alternate to CPU & GPU's in data centers due to its advantages like higher data transmission, High throughput, power efficient and flexibility. The main

advantage of FPGA's is its re-configurability by which users can make their own application specific data accelerator, and the performance of the applications can also increase by the machine learning in FPGA's. FPGAs are very much flexible devices for integrating with peripherals, depending on its application user can integrate it to system through Ethernet, PCIe, SATA, etc., the way of the FPGA integration with the system defines the type of data processing. This paper consists of seven sections, the section-I will gives the introduction, Section-II briefs the role of FPGA's in data centers and section-III to section-VI describes about high-end FPGA's by various vendors and their specifications, Section VII gives conclusion of the paper. The major vendors of FPGAs are: (In this paper, considered SOC-FPGA's embedded with features like PCIe Gen4 or 5 / Ethernet / SATA / Memory Controllers).

- Xilinx (Acquired By AMD)
- Microsemi (A Microchip Company)
- Altera (Now Intel)
- Achronix

The information presented in this paper collected from various sources like reference manual, Data books, user guides and Specifications provided by the vendors of that particular FPGA in their websites or from their marketing web portals, then analyzed and presented.

II. FPGA ROLE IN DATA CENTERS

Data center requirements & solutions by FPGA is explained with the help of diagram shown in Fig.1.

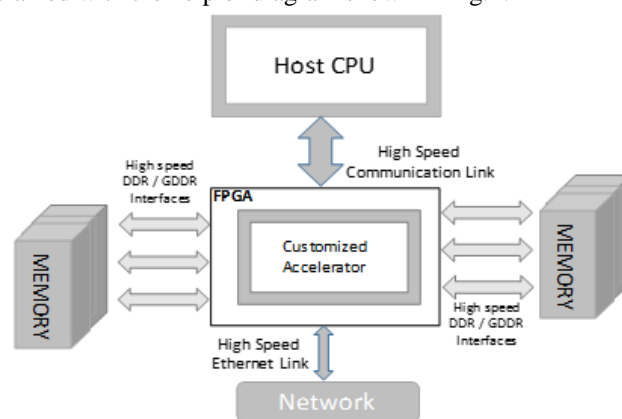


Fig. 1.FPGA based custom accelerator in data center

FPGAs will play major role in computing platforms by enabling flexibility in data acceleration and data processing. Among the several functions of datacenters FPGAs can help in:

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* Correspondence Author

Retikal Anil Kumar, Working as a Sr. Design Engineer, In Sion Semiconductors Private Limited, Bangalore, India, Email:anilretikal@gmail.com

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- Storage / Data Backup
- Data Acceleration
- Network Acceleration
- High Performance computing
- Machine Learning
- Scheduling & Managing tasks
- Security / Threat management / Monitoring

A. Storage / Data Backup

Higher the data rate will improve the bandwidth & decreases the latency significantly. The data rate of DDR3 is in between 800MT/s to 2133MT/s, DDR4 is in between 2133MT/s and 4266MT/s and DDR5 can serve max up to 6400MT/s.

Table- I: DDR Versions and their data rates

Type	Parameter	
	Data Rate	Transfer Rate
DDR	400MT/s	3.2GBps
DDR2	800MT/s	6.4GBps
DDR3	1600MT/s	12.8GBps
DDR4	3200MT/s	25.6GBps
DDR5	6400MT/s	32GBps

On the other hand, GDDR5, GDDR6 can provide maximum speed up to 8GT/s, 16GT/s respectively, The GDDR type with its data rate and transfer rate is explained in the below table.

Table- II: GDDR Versions and their data rates [2]

Type	Parameter	
	Data Rate @ Memory Clock	Transfer Rate
GDDR3	2.5GT/s @ 625MHz	19.9GB/s
GDDR4	2.2 GT/s @ 275MHz	17.6GB/s
GDDR5	5GT/s @ 625MHz 8GT/s @ 1000MHz	40-64GB/s
GDDR5X	10GT/s @ 625MHz 12 GT/s @ 875MHz	80-112GB/s
GDDR6	14GT/s @ 875MHz 16GT/s @ 1000MHz	112-128GB/s

The latest FPGAs coming up with the DDR3/4/5 or GDDR4/5/6 Interfaces and controllers, more the data rate means more the speed, and high bandwidth.

Hence, the FPGAs with embedded memory controllers as DDR/GDDRs are more flexible to handle the data backup process and able to solve storage requirements by the datacenters. In addition, few newer FPGAs also Offers co-packed DRAM structures by integrating High bandwidth DRAM memories (HBM) in FPGA Package with silicon stacking technology to provide more bandwidth and moderate latency.

B. Data & Network Acceleration

The functions like handling of TCP/IP messages or UDP/IP messages, Memory read/write, Network Function Virtualization can be offload into FPGA without the delay & latency of software systems.

EFPGA's / SOC-FPGA's / FPGA Boards are flexible to make Network attached FPGA's and also able to achieve higher data rates with standard high-speed protocols like PCIE, NVME, Ethernet.

PCI-Express is the best suitable and fastest interconnect for

establishing the communication link efficiently and reliably between the host CPU and FPGA. As the advancements in PCIE generations, increasing the speed & data rate of the link making PCIE as fastest interconnect technology among currently available.

Table- III: PCI-Express Generations and their data rates with respect to lane configurations

PCIE Generations	Parameter			
	Raw Bit Rate	Link Bandwidth	X8 link Bandwidth	X16 Link Bandwidth
Gen1	2.5GT/S	2Gbps	≈ 4Gbps	≈ 8Gbps
Gen2	5GT/S	4Gbps	≈ 8Gbps	≈ 16Gbps
Gen3	8GT/S	8Gbps	≈ 16Gbps	≈ 32Gbps
Gen4	16GT/S	16Gbps	≈ 32Gbps	≈ 64Gbps
Gen5	32GT/S	32Gbps	≈ 64Gbps	≈ 128Gbps

PCI-Express offers a power efficient robust architecture that supports enumeration & discovery of devices that are connected, and offers power saving modes like L0, L0s, L1, L2 with incremental latencies in each state respectively. Hence, for sending data at higher throughput, lower latency, and low power with high reliability has made PCI-Express is best suitable for deploying in datacenters.

The FPGA we can attach to network with the help of high-speed Ethernet link, in market the current speed / data-rates of the Ethernet are 1Gbps, 2.5Gbps, 5Gbps, 10Gbps, 25Gbps, 40Gbps, 50Gbps, 100Gbps and 400Gbps, in combination of Ethernet for transmission protocols, users can use either TCP (Transmissions Control Protocol) or UDP (User Datagram Protocol). UDP allows higher transmission data rate, as it does not require acknowledgement, IPv4 or IPv6 used for Internet Protocol and most of the high-end FPGAs from all the FPGA vendors are embedded with the Ethernet-MAC and able to provide access to the Physical layer using PHY.

C. Security

The Isolation Design Flows / Security conscious Design Flows by FPGA vendors are able to isolate physically & logically to the application logic of the user. Encryption, Decryption, Safety & Security algorithms gives privileged, un-privileged user modes, the user logic can only access to those un-privileged signals in FPGA, now a day the advanced FPGAs are providing secured boot logic that makes FPGAs more efficient to deploy in datacenters.

D. Flexibility

AI based system requires large number of computations with low latency. The advantage of FPGAs is user can implement their application specific algorithms in hardware level, which reduces the latency, as hardware is very much faster than the software. Developing an algorithm at hardware level may take certain iterations, when any error / update / upgrade needs to fix in the implemented algorithm it is easy to do with FPGA instead of ASIC, as the re-configurability of FPGAs allows users to configure multiple times throughout its lifetime.



The upcoming FPGAs are having on chip floating point DSP units, the architecture of latest FPGAs are in such a way that they are very flexible to implement the Machine Learning, Deep Learning, Deep Neural Network application. Few advantages of FPGAs than CPU and GPU

- Re-Configurability Logic
- Reconfigurable IO
- Low latency
- Power Efficiency
- Safety
- Faster time to market
- Connectivity with various peripherals
- Flexible to integrate with other processors

III. XILINX ACAP SOC FPGAS

Xilinx has recently launched industry's first ACAP (adaptive compute acceleration platform) Solution for datacenter applications, known as Xilinx Versal FPGAs, and announced in three series such as

A. Versal AI Core Series

Features and overview of the Xilinx Versal AI Core series is explained by below table

Table- IV: Features of Xilinx Versal AI Core Series FPGAs [1]

Features / Peripherals	Devices				
	VC1352	VC1502	VC1702	VC1802	VC1902
LUTs	2,46,784	3,64,544	480,256	725,000	899,840
CLB FFs	4,93,568	7,29,088	9,60,512	14,50,000	17,99,680
AI Engines	128	248	320	300	400
DSP Engines	928	1312	1696	1600	1968
NOC Master Slave ports	10	14	18	28	28
PCIE	1xGen4 X8lanes	4xGen4 X8 lanes	1xGen4 X8lanes	4xGen4 X8 lanes	4xGen4 X8 lanes
PCIE with DMA & CCIX	-	1xGen4 X16lanes	-	1xGen4 X16lanes	1xGen4 X16lanes
DDR Controllers Data width	2	2	2	4	4
Ethernet	1	4	3	4	4
GTY Transceivers (32.75Gbps)	8	44	24	44	44

B. Versal Prime Series

Features and overview of the Xilinx Versal Prime series FPGA's are announced in 8 variants, the overview of features is:

- LUTs Count range: from 1,53,472 to 10,20,928
- CLB FlipFlops range: from 3,06,944 to 20,41,856
- NOC Master Slave Interfaces : from 5 to 42
- DDR Memory Controllers : 1 to 4
- PCIE with DMA & CCIX : 1 Gen4 X8 lanes
- PL PCIE : 1-Gen4x8 to 4-Gen4x8lanes
- GTM Transceivers(58Gbps): 0 to 40

C. Versal premium Series

Features and overview of the Xilinx Versal premium series is explained by below table

Table- V: Features of Xilinx Versal Premium Series FPGAs [1]

Features / Peripherals	Devices						
	VP1102	VP1202	VP1402	VP1502	VP1552	VP1702	VP1802
LUTs	7,19,872	9,00,224	10,20,928	17,20,448	17,53,984	25,40,672	33,60,896
CLB FFs	14,39,744	18,00,448	20,41,856	34,40,896	35,07,968	50,81,344	67,21,792
DSP Engines	1904	3984	2672	7440	7392	10896	14352
NOC Master Slave ports	30	28	42	52	52	76	100
PCIE with DMA & CCIX	-	2xGen5x8lanes	-	2xGen5x8lanes	2xGen5x8lanes	2xGen5x8lanes	2xGen5x8lanes
PCIE	2xGen5x4lanes	2xGen5x4lanes	2xGen5x4lanes	2xGen5x4lanes	8xGen5x4lanes	2xGen5x4lanes	2xGen5x4lanes
DDR Controllers, Data width	3	4	3	4	4	4	4
Multi rate Ethernet MAC	6	2	6	4	4	6	8
600G Ethernet MAC	4	1	8	3	1	5	7
600G Interlaken	2	-	2	1	-	2	3
GTY Transceivers (112Gbps)	32	10	48	30	10	50	70

All the Versal FPGAs has on chip

- APU: Dual-core Arm Cortex-A72 [1]
- RPU: Dual-core Arm Cortex-R5F [1]
- 256KB Memory

Onchip Controller/MAC for Communication protocols

- Ethernet
- UART
- CAN-FD
- USB 2.0
- SPI
- I2C
- Multi rate EMAC supported in: 1 x 100GE, 2 x 50GE, 1 x 40GE, 4 x 25GE, and 4 x 10GE configurations [1].

IV. MICROSEMI SOC FPGAS

Microsemi has two midrange SoC FPGAs with on chip high speed serial links (like PCIE) and memory controllers (like DDR) they are

- PolarFire SoC FPGA
- Smart Fusion2 SoC FPGA

A. Polar Fire SoC FPGA

- 2x PCIe Gen 2 with x1, x2, x4 configurations
- DDR3/4 Support [9].



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- LPDDR3/4 support [9].
- Gb-Ethernet with SGMII [9].
- 12.7 Gbps transceivers – power optimized transceivers [9].
- 461k logic elements consisting of a 4-input Look-Up Table (LUT) with a fracture-able D-type flip-flop [9].
- 2MB L2 Cache [9].
- Up to 31.6 Mb of RAM
- Support communication interfaces like 2xCAN, 2xSPI, 5xUART, and USB OTG [9].

B. Salient features of Smart Fusion2 SoC FPGA Family [10]

- 150K LE device reliable flash-based FPGA fabric [10].
- 166 MHz Cortex™-M3 processor[10].
- PCIe Gen2 x4 , x2,x1 configurations
- DDR3 SDRAM
- SRAM & eNVM Support
- SMA connectors for SERDES [10].
- USB Micro-AB, USB mini-B Connectors
- RJ45 for 10/100/1000 Ethernet [10].
- Debug LED/switches
- J60, J30 FMC Connectors [10].

V. INTEL SOC FPGAS

For data center applications Intel announced Agilex SOC FPGAs in three series (F, I, M Series), common features of Agilex series FPGAs are given by:

- On Chip Processing System with
 - Quad-core 64 bit ARM Cortex-A53 with maximum operating frequency up to 1.41 GHz
 - 32 KB Instruction and Data cache
 - NEON coprocessor
 - 1 MB L2 cache
 - Direct memory access (DMA)
 - System memory management unit
 - Cache coherency unit
 - Hard memory controllers
- Supports AES For security
 - On-chip Timers available:
 - General purpose timers x7
 - watchdog timer x4
 - On-chip controllers/MAC for Communication protocols
- USB 2.0x2,
- 1G EMAC x3
- UART x2
- Serial peripheral interface (SPI) x4
- I2C x5
 - High Speed Interconnects in F-Tile
 - PCI Express with Gen4 x16 lanes [7]
 - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) [7]
 - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) [7]
 - 600G Interlaken [7]
 - Supports IEEE 1588 [7]
 - High Speed Interconnects in R-Tile
 - PCIe hard IP block (Gen5 x16) [7]
 - Compute Express Interface (CXL) - Link width supports in

- both x16 lanes and x8 lanes [7]
- SRIOV Support [7]

A. Features of Agilex I-Series FPGAs

Memory Devices Supported:

- DDR4
- QDR IV
- RLDRAM 3

Available Logic Elements

- 2,208,075 in AGI022
- 2,692,760 in AGI027

B. Features of Agilex F-Series FPGAs

Memory Devices Supported:

- DDR4
- QDR IV
- RLDRAM 3

Logic Elements available:

- Available in 7versions consisting of Logical Elements from 3,91,996 to 26,92,760

F-series has extra two tiles they are H-Tile and P-Tile, High speed interconnects available in H-Tile are PCIe hard IP block with Gen3x8lanes configuration, Networking Support with Ethernet MAC 50/100GbE PCS, Supports SR-IOV, Whereas P-Tile has PCIe Gne4 hard IP block with x16lanes [6].

C. Agilex M-series FPGAs

The features of Agilex M-Series FPGAs are yet to be release, and it is expected with HBM & DDR5 memory controllers.

VI. ACHRONIX SPEEDSTER-7T FPGAS

Achronix has announced speedster 7nm FPGAs for High Bandwidth applications in 4variants, Features of speedster 7t FPGA is given in below table.

Table- VI: Features of Achronix Speedster FPGAs [8]

Features / Peripherals	Devices			
	AC7t750	AC7t1500	AC7t3000	AC7t6000
6-input LUTs	363K	692K	1.3M	2.6M
Embedded memory	100 Mb	190 Mb	192 Mb	385 Mb
MLP blocks	336	2,560	880	1,760
Dedicated GPIO	32	64	50	100
Additional GPIO	150	150	300	600
DDR5 channels	1	1	2	4
GDDR6	8 channels	16 channels	16 channels	16 channels
PCIe Gen5	One ×16	One ×16 and one ×8	One ×16 and one ×8	Two ×16
Ethernet	8 lanes, 2×400G or 8×100G	16 lanes, 4×400G or 16×100G	16 lanes, 4×400G or 16×100G	32 lanes, 8×400G or 32×100G
SerDes (112Gbps)	24 + 16	32 + 0	40 + 32	72 + 0



VII. CONCLUSION

Industry giants like Microsoft, Intel, AMD started to push the FPGA based data accelerators into the data centers. High-end SoC FPGA's / EFPGA's are one of the major solutions for demand handling data traffic in various aspects.

In this paper, introduced the various requirements of datacenters and briefed the data rates of high-speed connectivity protocols like PCIe, Ethernet & Memory controllers like DDR & GDDR versions, explained the FPGA compliance in datacenter applications and analyzed the latest SOC-FPGA architectures with their features like on-chip peripherals and controllers, supported protocols, Interconnects, Network connectivity, Bandwidth.

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AUTHORS PROFILE



R Anil Kumar Working as Sr. Design Engineer in Sion Semiconductors Private Limited Bangalore, Completed post-graduation M.Tech in VLSI System Design from Anurag Group of Institutions, his areas of interest are, ASIC Design, SOC Architectures, FPGA Design and Serial Link interconnects like PCI-Express,

Ethernet.