

# Effect of CNTs Parameter Variation on the Performance of Analog Device

Shailendra K. Tripathi



**Abstract:** Carbon nanotubes (CNTs) have emerged as a prominent material for present day nano-scale systems design. In spite of their widespread use in biology, and nano-electro mechanical systems (NEMS, CNTs have encroached upon conventional MOSFETs for the design of low power and high speed circuits. Because CNT possesses higher current carrying capability, higher transconductance and near ballistic transport of charge carriers. The diameter of the CNTs laid from the Source to the Drain in a CNFET has the significant influence on the characteristics of the device itself as well as on the features of circuits implemented using the said CNFET. Such variations in circuit parameters with CNT diameter can be shown to be more pronounced in analog circuits as compared to digital CNFET-based designs. The present work attempts to investigate the effect of diameter variation on a versatile analog building block (ABB) viz. the inverting current conveyor. It is demonstrated that various parameters of the ICC-II under scrutiny, like voltage bandwidth, current bandwidth, average power dissipation, etc. depend on the diameter of CNT(s) used in the CNFETs. HSPICE simulations performed on a 0.9V; 32nm CNFET-based ICC-II are included to exemplify the dependencies studied.

**Keywords:** Analog Circuits, Nano-electronics, CNFET, CMOS

## I. INTRODUCTION

The present trends and overall needs for ICs are low power supply, high packaging density, and low power consumption. The accuracy for signal processing is another requirement in various applications [1-2]. From the last thirty years, the electronic industry has achieved a notable scaling of transistor sizes with the number of devices (transistors) on an integrated circuit approximately raising double in every 18–24 months [3]. Moreover, it is being projected that processing technology based on Silicon will reach to its capacity with channel length of CMOS around sub-10 nm. As the channel length lines sub-10 nm regime, secondary effects and tunneling occur, which stop further scaling of MOSFET device [4]. On account of this, the electronic industry is putting efforts for alternate materials and technology to amalgamate with current MOSFET-based fabrication techniques. The technologies beyond-CMOS like as CNFET

[5], Tunnel-FET and Single Electron Transistor (SET) [6], are came into the picture. Among above technologies, the CNFET is the most protuberant due to its superior features which are added because of carbon nanotube (CNT). The CNTs have near ballistic transport of charge carrier and alterable band gap, which make them a superior channel material for low power and high-speed futuristic electronics [7].

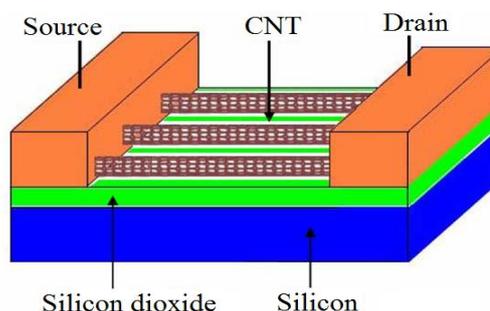


Fig. 1: CNFET Structure

Figure 1 shows the block diagram of a CNFET. The CNFET offers higher transconductance, higher drive current, higher carrier mobility, and better control over channel [8], [9].

## II. THEORETICAL BACKGROUND OF CNFET

A carbon nanotube contains two arrangements, (i) Single-walled carbon nanotube (SWCNT) and (ii) Multi-walled carbon nanotube (MWCNT) as presented in Figure 2. SWCNTs are basically the rolled sheets of Graphene. The diameter of SWCNTs is 1 nm -2 nm and length around 0.2 μm -5 μm. The MWCNTs look like as a coaxial cable with the assemblage of SWCNTs. The diameter of MWCNTs fluctuates from 2-25 nm, and inter-layer space is around 0.36 nm [10], [11].

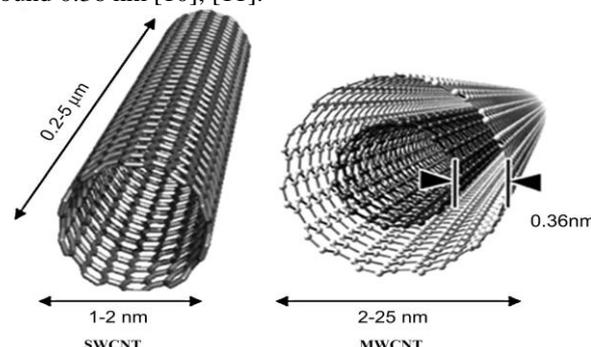


Fig. 2: Single and Multi-walled Structures of CNT

The CNTs having three alternatives depend on the chiral vector and chiral angle ( $\theta$ ). A CNT is called zigzag, if  $m = n$  and  $\theta = 0^\circ$  and known as armchair, if  $m = 0$  and  $\theta = 30^\circ$ .

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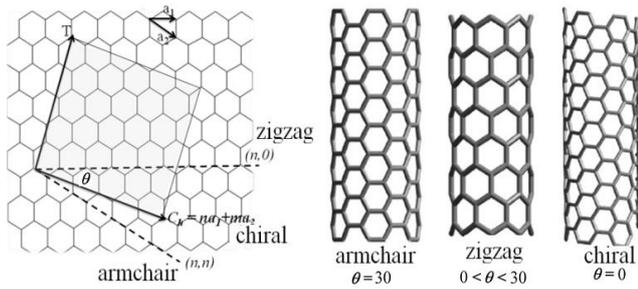
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Further, as chiral vector  $m \neq n$  and chiral angle lies between 0 and 30°, CNT is known chiral, as illustrated in Figure 3.



**Fig. 3: Types of Carbon Nanotubes**

The circuits based on CNTs possess fewer leakages current and improved switching. The construction of a CNFET is alike to MOS transistor excluding the SWNTs play as the device channel region. The metal contacts fabricated on either end of the SWNTs work for the source and drain. CNFET shows merits over conventional MOSFET, such as decrease in carrier tunneling and short-channel effects improved current density, greater carrier velocity and decreased leakage currents. Moreover, the drain current of transistor is shown by (1) and it is contingent upon charge mobile densities ( $\xi_S$  &  $\xi_D$ ) which are represented in (2) and (3).

$$I_D = \frac{4qkT}{h} [\ln(1 + \exp(\xi_S)) \ln(1 + \exp(\xi_D))] \quad (1)$$

$$\xi_S = \frac{(\Phi_S - \delta_1)}{V_T} \quad (2)$$

$$\xi_D = \frac{(\Phi_S - \delta_1 - V_{DS})}{V_T} \quad (3)$$

Further, the mobile charge densities of CNFET are connected to surface potential ( $\Phi_S$ ) and thermal voltage ( $V_T$ ) as illustrated in (4). Additionally, the CNT diameter ( $d$ ), thickness of oxide ( $t_{OX}$ ), and capacitance of oxide ( $C_{OX}$ ) of CNFET are related by (6) with some constants parameters [12]. The relation of threshold voltage is given in (6). Moreover,  $\delta_1$  is known as equilibrium sub-band minima of first sub-band ( $E_G = 2$ ). The terms  $q$ ,  $k$ ,  $T$  and  $h$  represent

electron charge, Boltzmann's constant, absolute temperature and Planck's constant accordingly [13].

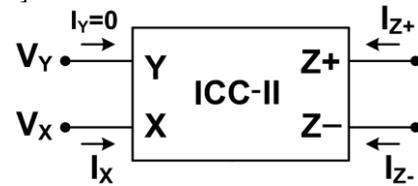
$$\Phi_S = \frac{V_{GS} - qN_{mobile}}{C_{OX}} \quad (4)$$

$$C_{OX} = \frac{2\pi \epsilon_0 \epsilon_{OX}}{\ln(2t_{OX} / d) + 1} \quad (5)$$

$$V_T = \frac{kT}{q} \quad (6)$$

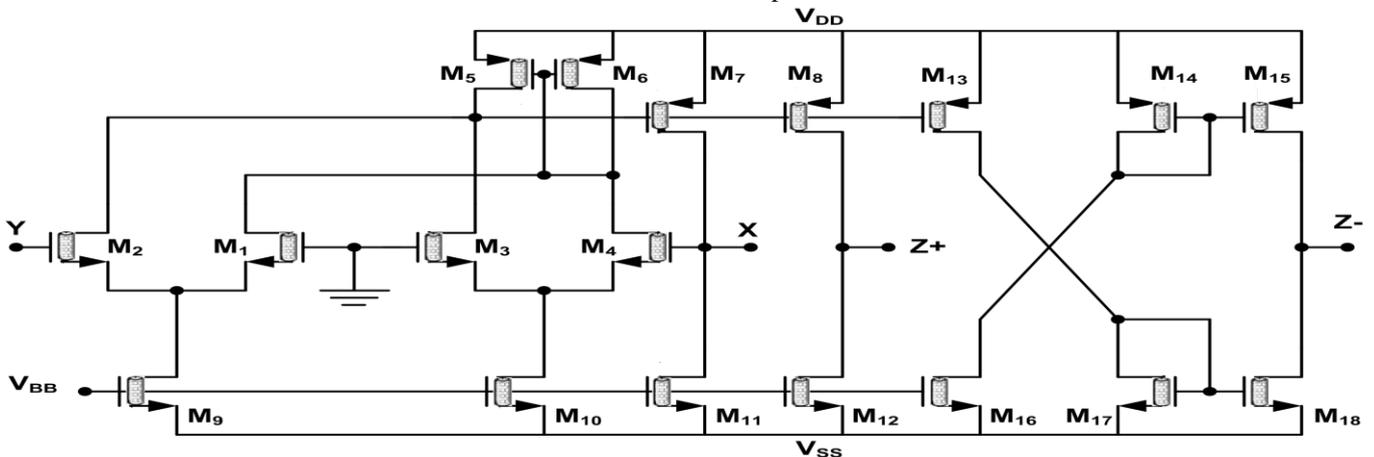
### III. CNFET-BASED INVERTING CURRENT CONVEYOR-II

The circuits with current-mode (CM) approach have gained noteworthy consideration because of their aids weighed against voltage-mode (VM) circuits in terms of wider bandwidth, higher linearity, enhanced dynamic range and reduced power consumption [14-17]. Further, CM circuits are appropriate for integration with CMOS process technology [17], [18]. The ICC-II was presented by Soliman et.al, to implement the CM circuits from the VM circuits [19], [20]. The block diagram of ICC-II is given in Figure 4. The port equations of inverting current conveyor are shown in (7). This is very versatile active device and also implemented with CNFET [24].



**Fig. 4: Symbol of ICC-II**

The CMOS technology has many performance concerns which can be answered by recently emerging CNFET technology [5], [12], [13]. The CMOS realization of ICC-II has been presented in the literature [23], [25]. Transistor level implementation of Current Conveyor based on CNFET is presented in Figure 5. The design uses HSPICE 32 nm parameters, developed by Stanford [21]. The important model parameters are illustrated in Table 1.



**Fig. 5: Implementation of ICC-II with one Z+ and one Z- output [15]**

In subsequent section, the effects of diameter alteration on the performance of device have been tested taking some other parameters in the design. The results would discover the various favorable effects for the CNT-based circuit design in coming future.

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (7)$$

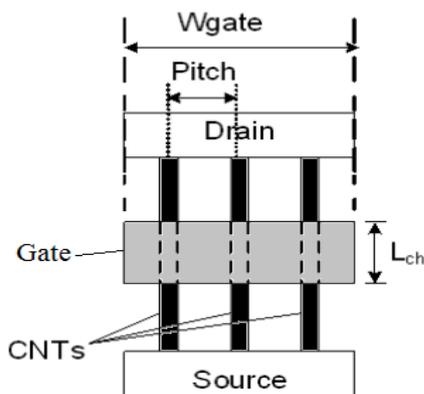


Fig. 6: Schematic of a CNFET

TABLE 1: CNFET DESIGN PARAMETERS

S.N.	Parameters	Value
1	Oxide Thickness ( $T_{OX}$ )	4 nm
2	Dielectric Constant ( $K_{OX}$ )	16
3	Power Supply	$\pm 0.9$ V
4	CNT's Chirality (n, m)	19, 0
5	Physical channel length ( $L_{ch}$ )	32 nm
6	No. of tubes in the device	6
7	Pitch (S)	14 nm

#### IV. OPTIMIZATION OF CNT DIAMETER

The CNT parameters like diameter ( $D_{CNT}$ ), threshold voltage ( $V_{th}$ ) etc. have been measured in the design of CNFET-based devices. The useful relations are illustrated in equations (8), (9).

$$D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \quad (8)$$

$$\sum g = \frac{0.84eV}{D_{CNT}} \quad (9)$$

$$V_{th} = \frac{aV_{\pi}}{qD_{CNT}\sqrt{3}} \quad (10)$$

Also, CNFET's width (W), number tubes (N), pitch (S) are given in (11) and presented in Figure 6. The n and m are the indices's of Graphene lattice and  $a = 2.49 \text{ \AA}$  (constant). Additionally, electronic charge is represented by q and  $V = 3.033 \text{ eV}$ , is the Carbon's  $\pi$ -  $\pi$  bond energy.

$$W = (N - 1) * S + D_{CNT} \quad (11)$$

The diameter of the carbon nanotube is a physical property that closely depends on the indices of Graphene lattice (n, m) given in (8). The single-walled CNT is obtained from the Graphene layer and its diameter has the great impact on the threshold voltage and band gap of the device as shown in (9) and (10). It is important to know that the modification of band gap in MOS transistor is critical but in CNFET, it can be easily controlled by diameter of the nanotube. The width of transistor also depends on the diameter of CNT [22]. The extensive simulations have been carried out to test the properties of current conveyor block.

#### (i) Variation in the Number of Tubes

The diameter of CNT affects various parameters of CNFET, and it is considered further the effect of the change in the diameter of CNT on the performance of CNFET-based inverting current conveyor. Results show that frequency response of the device is improved by increasing the diameter as illustrated in Figure 7. It is also attempted to see the effect of variation in the number of tubes with the 3-dB bandwidth of the device.

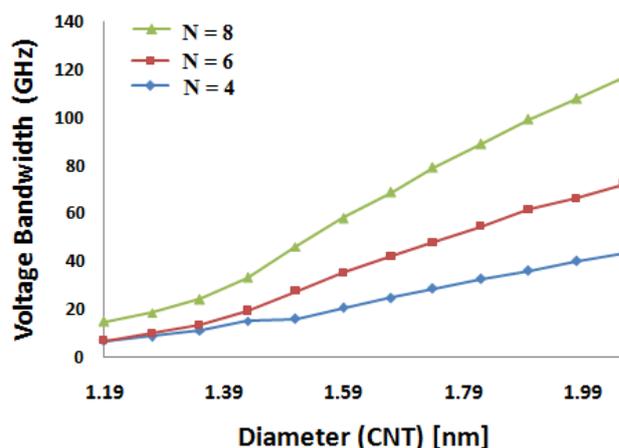


Fig. 7: CNT Diameter versus 3-dB Voltage Bandwidth with the Number of CNT

Figure 7 presents that 3-dB voltage bandwidth drastically improved with the increase in the number of tubes. The number of tubes in the channel controls the current supply for the load [23], [24]. A transistor with single-CNT could not provide sufficient current to meet the desired performance. Moreover, current-mode circuits have comparatively higher bandwidth than voltage-mode circuits. Figure 8 gives the effect of the number of tubes variation on the 3-dB current bandwidth of building block. The power requirement is an important issue in modern low power circuit design. Figure 9 illustrates the effect of diameter variation versus average power dissipation with the number of tubes as an additional parameter in the picture. For this particular analysis, the other design parameters except for diameter ( $D_{CNT}$ ) and number of CNT (N) are kept as given in Table 1.

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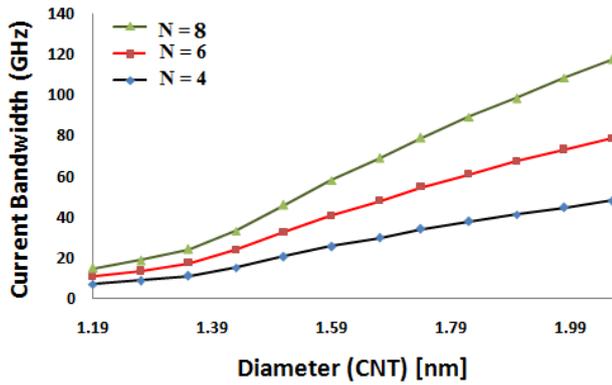


Fig. 8: CNT Diameter versus 3-dB Current Bandwidth with the Number of CNT

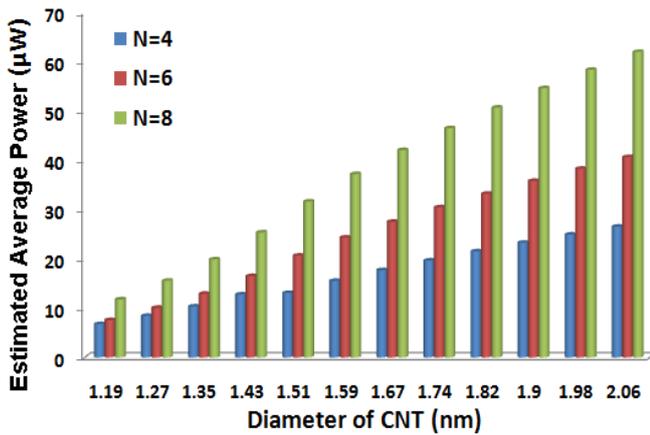


Fig. 9: CNT Diameter versus Average Power with the Number of CNT

### (ii) Variation in Power Supply

An attractive feature of CNFET that it can operate at much scaled power supply voltages. The effect of power supply variation in the performance of ICC-II is explored in the proposed work. The scaled supply voltages have more effect of parasitics and so on the performance [25].

Figure 10 depicts that 3-dB voltage bandwidth reducing with scaled power supply voltages. Although, the scaled voltages have the pessimistic effect on frequency response yet it reduces the average power of the device that is needed for present low power circuit design. The similar effort has been repeated for current-mode design.

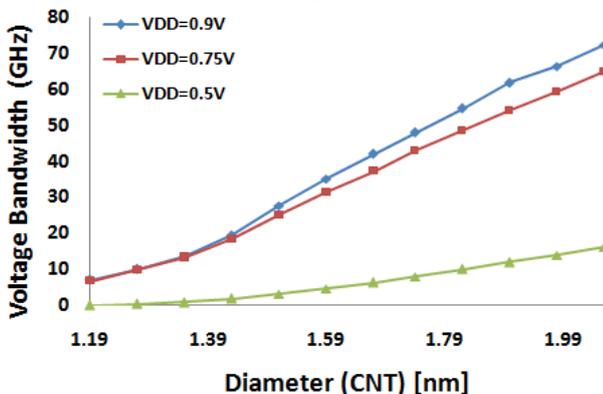


Fig. 10: CNT Diameter versus 3-dB Voltage Bandwidth

Figure 11 shows the variation in 3-dB current bandwidth with supply voltage, and it reflects that scaling of supply voltage limits the current bandwidth also. Thus it is a trade-off

between bandwidth and power requirements for the designers to choose the optimum values for futuristic applications [26].

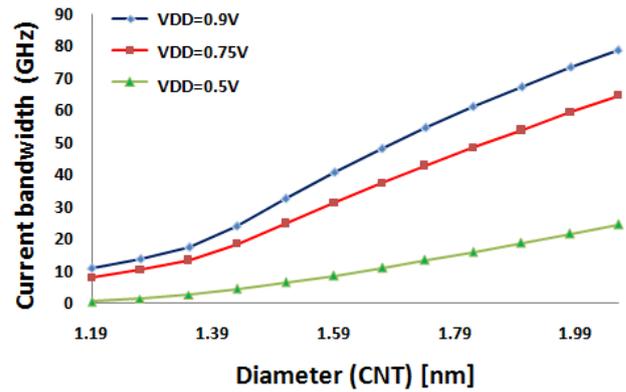


Fig. 11: CNT Diameter versus 3-dB Current Bandwidth

Figure 12 represents the effect of power supply scaling on the average power requirement of the device (CNFET). The other design parameters like inter-CNT pitch (S), number of CNT (N), oxide thickness ( $T_{OX}$ ), dielectric constant ( $K_{OX}$ ) have been referred from Table 1. Finally, it is important to discuss the advantages of current-mode circuits over voltage-mode counterparts. They have inherently wide bandwidth, greater linearity, wide dynamic range and simple circuitry.

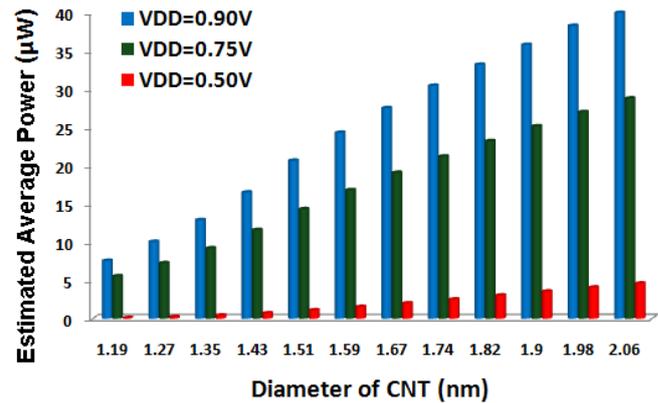


Fig. 12: CNT Diameter versus Average Power

## V. CONCLUDING REMARKS

In this paper, the advantages of carbon nanotube and transistor based on CNT have been discussed. This work investigated the effect of CNT diameter variation in the performance of analog building block. The bandwidth of above 100 GHz is achieved with the CNFET-based design which is far away from CMOS design. In this paper optimization of the number of tubes and power supply voltages express a wide significance for the CNFET-based low power circuit design which can solve the challenges of current nano-electronics. In addition to this, features of CM circuits are emphasized over VM circuits in the design. The results included in the paper are expected to act as guidelines for practicing electronics designers to decide the most optimum value of the diameter of CNTs for a particular design. The performance depicts that CNFET can be a suitable alternate option for present MOSFET technology.



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