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V/C Digital Controlled DC-DC Converter

R.Sravani, P.Deepak Reddy

Abstract: ***In this paper, the switching of dc-dc converter using voltage/current digital control is proposed. It is the combination of existed digital average voltage and digital average current controls. The stability analysis of V/C digital controlled dc-dc converter is derived by using sampled data model. The transient analysis of V/C digital controlled dc-dc converter is also derived by using z-domain small signal model. The proposed V/C digital controlled dc-dc converter has over current protection, fast load transient response, no sub-harmonic oscillations at any value of duty cycle, and wider stability range. The proposed system is analysed with a simple buck converter. The output voltage and inductor current weighting factors influence the stability boundary and transient performances of V/C digital controlled dc-dc converter. The stability analysis and transient analysis is investigated and verified by circuit simulations.***

Keywords: sampled data modelling, stability analysis, transfer function, transient analysis, z-domain small signal modelling.

I. INTRODUCTION

As electronic technology develops, the electronic appliances power supply performance requirements are increasing. They should have faster load transient response, higher output voltage accuracy, wider stability range and over current protection. The performance of switching dc-dc converter is affected by control technique[1]-[4]. The stability and transient performances can effectively improved by enhancing the control technique of switching dc-dc converter [5]. The basic voltage control is easy but low input and load transient responses [6]. Therefore, the requirements of the power supply for advanced electronic appliances cannot satisfy with voltage control.

In V^2 control the inner loop utilizes the output voltage wavelet as control signal based on voltage control. It exhibits rapid load transient response but has less anti-interference ability. It is because of having insufficient amplitude of the inner-loop voltage wavelet. It is eliminated by placing a capacitor having large equivalent series resistance (ESR) at the output, with this it can operate in stable state and does not manifest over current protection [5],[7]-[9]. In current control the inner loop control signal is the switch current or inductor current. It gives rapid input response and dynamic anti-interference ability. Current control has over current protection but the load transient performance is objectionable [5],[10]-[12]. In V^2C control the inner loop control signal is the combination of the inductor current and the output voltage. Accordingly it combines both advantages of voltage and current mode controls [5] i.e., over current protection in current control and rapid load transient performance of V^2 control additionally it has dynamic anti-interference ability [13],[14]. The disadvantage of V^2C control circuit has obstacles in designing and working and when the duty cycle is above 0.5 it generates sub-harmonic oscillations, as it is a peak- ripple based control method [14],[15].

Now a day's digital technology is improving day by day as it is advantageous than analog technology. They are increment of processing capabilities and low cost. The digital control is also more and more feasible for low to medium power switching and high frequency converters [16]-[26]. From the research it is known that the digital control deals with some modulations, such as triangle, trailing and leading-edge. They get rid of sub-harmonic oscillations [18]-[20]. A digital average voltage proposed by Liu et al [21] has rapid load response and no sub- harmonic oscillations but it can operate only with high valued capacitor ESR at the output. It doesn't provide over current protection. Digital peak control has been proposed by G. Zhou [23] has no sub-harmonic oscillations and the duty cycle exceeds 0.5 but the controlling of inner loop signal peak value to be enhanced when current wavelet and voltage wavelet is high. To get most advantageous performance for dc-dc converters capacitor charge balance [24] is proposed but its control algorithm is very complex. A talented control scheme to manage power converter has been introduced in the field of power electronics i.e., model predictive control [26]. The contribution of this paper is as follows. A V/C digital controlled dc-dc converter is propose to eliminate the above discussed drawbacks which manifests with wider stability, fast load transient response, less sub-harmonic oscillation at any value of duty cycle, over current protection and high output voltage accuracy. To study the influence of inductor current and output voltage weighting factors on load transient performance and stability the z-domain small-signal modeling and sampled-data modeling have been used, respectively. Including that the robustness of V/C digital controlled buck converter is analyzed. The paper is systematized as follows. In session–II working principle and control algorithm of V/C digital control and the robustness of V/C digital control are analyzed with the help of buck converter. In session-III the load transient performances and stability are analyzed by using the z-domain small-signal modeling and sampled-data modeling, respectively, and stability boundary is obtained. On the load transient response and stability the effect of the output voltage and inductor current weighting factors are analyzed. MATLAB Simulation results are shown in session-IV. Finally, the paper is concluded in session-V.

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II. ANALYSIS OF V/C DIGITAL CONTROLLED DC-DC CONVERTER

A. Principle of V/C Digital Control

The circuit diagram of V/C digital controlled buck converter is shown in Fig-1. The V/C digital controlled buck converter circuit has input voltage V_{IN}, capacitor C_O, MOSFET M, inductor L_O, free-wheeling diode D and output capacitor equivalent series resistance R_{ESR}, load resistor R_O, digital pulse width modulation (DPWM), digital proportional-integral-differential compensator (D-PID) and analog to digital converter (ADC). Some physical quantities are represented as, capacitor voltage as V_{CO}, capacitor current as I_{CO}, inductor current as I_{LO}, inductor voltage as V_{LO}, output current as I_O, and output voltage as V_O, while sampling value of V_O as V_{OS}, sampling value of I_L as I_{LS}, and control signal as V_C, ADC sampling clock signal as V_{CK}, digital reference voltage as V_{REF}, gate signal as V_G, switching period as T, rising slope of V_S as S_1, falling slope of V_S as S_2, duty cycle of n^{th} cycle is as D_N and duty cycle of $n+1^{th}$ cycle as D_{N+1}.

The operating waveforms of sampling signal V_S and V_G is shown in Fig-2, where V_S is the sum of I_{LS} and V_{OS}. The steady state operating waveforms are represented in solid lines and the transient waveform with perturbation signal V_P is represented in dashed lines. The V_S can be obtained by S_1, S_2 and T.

When perturbation occurred V/C digital control forces $V_S(n)$ to made equal to V_C by controlling the duty cycle. The operating principle of V/C digital controlled dc-dc converter is as follows. At the beginning of the nth cycle V_G is high and mosfet M is switched ON. At that time the clock pulse V_{CK} enables the ADC to sample the I_{LO} and V_O and the I_{LS} and V_{OS} is obtained to form V_S. At the same time $(n+D_N/2)T$ the V_G is low and M is switched OFF again at the time $(n+1-D_N/2)T$ is switched ON and remains ON until the end of the n^{th} cycle. DPWM gives duty cycle D_N based on V_C, T, V_S and D-PID calculates V_C based on V_{OS} and V_{REF}. .

B. Algorithm Implementation of V/C Digital Control

At the beginning of each cycle, ADC samples the V_O and I_{LO} and is hold during that cycle. The V_S is obtained as

$$V_S(n) = W_1 I_{LS}(n) + W_2 V_{OS}(n) \qquad (1)$$

Where W_1 and W_2 are the output voltage and inductor current weighting factors, respectively. When W_1=0, the V/C digital control act as DAV control and when W_2=0, the V/C digital control act as DAC control. So these are the two special cases of V/C control.

Now the sampling signal $V_S(n)$ can be expressed as

$$V_S(n+1) = V_S(n) + \frac{S_1 D_N T}{2} - S_2 D_N' T + \frac{S_1 D_N T}{2} \qquad (2)$$

Where S_1 and S_2 can be expressed as

$$S_1 = (W_1 + W_2 R_{ESR})\frac{V_{IN} - V_O}{L_O},$$
$$S_2 = (W_1 + W_2 R_{ESR})\frac{V_O}{L_O} \qquad (3)$$

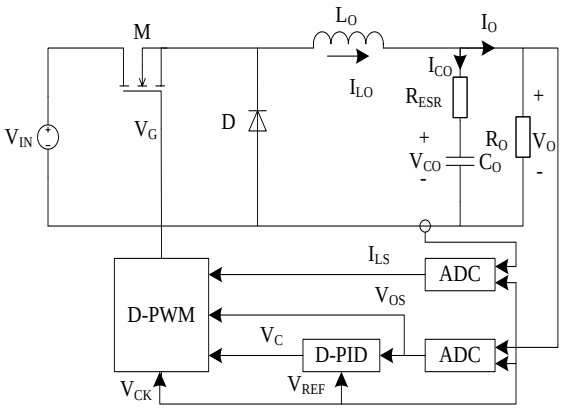

Fig-1- Circuit diagram of V/C digital controlled buck converter

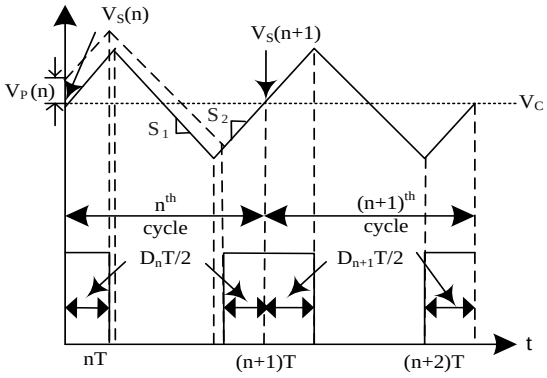

Fig-2 - V/C digital Controlled Buck Converter Operating Waveforms

D-PID calculates the control signal $V_C(n)$ and it can be express as

$$V_C(n) = K_P E(n) + K_I \sum_{I=0}^{N} E(I) + K_D[E(n) - E(n-1)] \qquad (4)$$

Where K_p, K_I and K_D are proportional, integral and differential coefficients, respectively and $E(n)=V_{REF}-V_{OS}(n)$. The aim of V/C digital controlled dc-dc converter is to force V_S to follow $V_C(n)$ at the end of present switching cycle. Substitute $V_S(n-1)$ by $V_C(n)$,

$$V_C(n) = V_S(n) + \frac{S_1 D_N T}{2} - S_2 D_N' T + \frac{S_1 D_N T}{2} \qquad (5)$$

By simplifying the above equation we can get algorithm of V/C digital controlled dc-dc converter.

$$D_N = \frac{V_C(n) - V_S(n)}{(S_1 + S_2)T} + \frac{S_1}{S_1 + S_2} \qquad (6)$$

Digital implementation of the V/C digital controlled dc-dc converter is shown in Fig-3. Counter based DPWM generates the digital ramp V_R. It counts 0 to V_M continuously. By comparing $D_N V_M/2$ and $(1-D_N/2)V_M$ with V_R the gate signal V_G is obtained which are changed with D_N. V_G is low level when $D_N V_M/2 \geq V_R \geq (1-D_N/2)V_M$ otherwise high level. The counter is reset when V_G has reached V_M and a new cycle begins.

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C. Robustness Analysis of V/C Control Algorithm

From the derived algorithm of V/C digital control it is seen that the control relies upon on the assumptions that the input voltage, the output voltage, the switching period and the inductance are known. The DSP system's clock decides the switching period and practically its variation can be neglected. However, the working conditions or aging, change in temperature will affect the value of the inductor. It may also have considerable tolerances and the output voltage and input voltage are the same. The results exhibit that the control has good robustness and the deviation of the inductance and output voltage does no longer have an impact on the stability of algorithm [18]. The robustness analysis L_O and V_{IN} of V/C digital controlled buck converter are discussed in this section. The error between the practical value and the designed value of inductor is represented as ΔL. Consider that at the beginning of first cycle the converter is stable, then at the beginning of (n-1)th cycle a voltage disturbance $\Delta V_S(n-1)$ is inserted, the new slopes can be obtained by

$$S_1' = (W_1 + W_2 R_{ESR}) \frac{V_{IN} - V_O}{L_O + \Delta L_O}$$
$$S_2' = (W_1 + W_2 R_{ESR}) \frac{V_O}{L_O + \Delta L_O} \quad (7)$$

Where S_1' is new rising slope and S_2' is new falling slope of V_S. Then, at the beginning of the nth cycle the disturbance of V_S can be obtained as

$$\Delta V_S(n) = V_C(n-1) - [V_S(n-1) + \frac{S_1' D_{N-1} T}{2} - S_2' D_{N-1}' T + \frac{S_1' D_{N-1} T}{2}]$$
$$= D_{N-1} T(S_1 - S_1') + D_{N-1}' T(S_2' - S_2)$$
$$= -\frac{\Delta L_O}{L_O + \Delta L_O} \Delta V_S(n-1) \quad (8)$$

Similarly, with practical input voltage V_{IN}+ ΔV_{IN} at the beginning of the nth cycle the disturbance of V_S can be expressed as

$$\Delta V_S(n) = \frac{\Delta V_{IN}}{V_{IN}} \Delta V_S(n-1) - \frac{\Delta V_{IN}}{V_{IN}} \frac{R_{ESR} T V_O}{L_O} \quad (9)$$

From this it is clear that as long as $\Delta L_O << L_O$ and $\Delta V_{IN} << V_{IN}$, the inductor tolerance and input tolerance not effects the control performance, in practical applications it is difficult to meet. Finally we can justify that even though the circuit parameters have small variation the V/C digital control is robust and can maintain converter in stable state.

III. STABILITY AND TRANSIENT ANALYSIS OF V/C CONTROLLED BUCK CONVERTER

The V_S is linear when the output capacitor ESR is large as in the above analysis. In some cases the ESR is small when for output filtering multiple paralleled ceramic capacitors are utilizes, so the effect of the nonlinearity of V_S on the stability of V/C digital control is considerable. So we have to analyze the stability boundary for V/C digital control related to ESR. It is done by using sampled data modeling. The DAV and DAC are the two individual cases of V/C digital control. The two controls have two different load transient performances. The V/C digital control load transient performance is affected by and the output voltage and inductor current weighting factors. The transient analysis is done by z-domain small signal modeling.

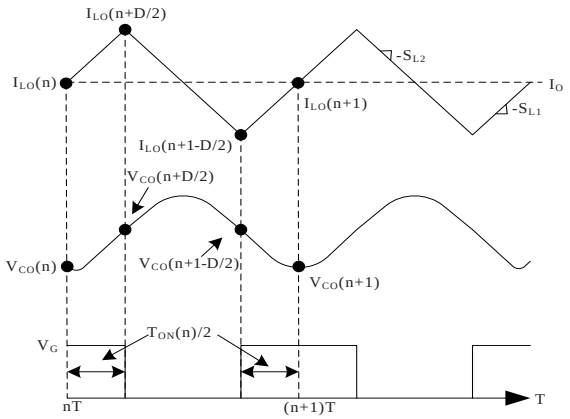

Fig-4 – V/C digital controlled buck converter Inductor Current, Capacitor Voltage and Driver signal Waveforms

A. Stability Analysis Using Sampling Data Modeling

The sampled data modeling is performed to obtain the V/C digital controlled buck converter stability boundary. The capacitor voltage, inductor current and driver signal waveforms are shown in Fig-4. Inductor current rising slope and falling slope are represented as S_{L1} and S_{L2}, respectively. The on time of nth switching cycle is $T_{ON}(n)$. the inductor current rising slope and falling slope can be expressed as

$$S_{L1} = \frac{V_{IN} - V_O}{L_O}, S_{L2} = \frac{V_O}{L_O} \quad (10)$$

$V_{CO}(n)$ and $I_{LO}(n)$ denotes the capacitor voltage and inductor current. At T=n+D/2 the diode D is forward biased when the mosfet M is switched off. At T=n+D/2 the capacitor voltage $V_{CO}(n+D/2)$ and inductor current $I_{LO}(n+D/2)$ can be expressed as

$$I_{LO}\left(n + \frac{D}{2}\right) = I_{LO}(n) - S_{L1} \frac{T_{ON}(n)}{2}$$
$$V_{CO}\left(n + \frac{D}{2}\right) = V_{CO}(n) - \frac{1}{C_O} \int_0^{\frac{T_{ON}(n)}{2}} I_{CO}\, dt$$
$$= V_{CO}(n) + \frac{I_{LO}(n) - I_O}{2C_O} T_{ON}(n) + \frac{S_{L1} T_{ON}^2(n)}{8C_O} \quad (11)$$

At T=n+1-D/2 the diode D is reverse biased when the mostet M is switched on. At T=n+1-D/2 the capacitor voltage $V_{CO}(n+1-D/2)$ and inductor current $I_{LO}(n+1-D/2)$ can be expressed as

$$I_{LO}\left(n + 1 - \frac{D}{2}\right) = I_{LO}\left(n + \frac{D}{2}\right) - S_{L2} T_{OFF}(n)$$
$$V_{CO}\left(n + 1 - \frac{D}{2}\right) = V_{CO}\left(n + \frac{D}{2}\right) + \frac{1}{C_O} \int_0^{T_{OFF}(n)} I_{CO}\, dt$$
$$= V_{CO}\left(n + \frac{D}{2}\right) + \frac{I_{LO}(n) - I_O}{C_O} T_{OFF}(n) + \frac{S_{L1} T_{ON}(n) T_{OFF}(n) - S_{L2} T_{OFF}^2(n)}{2C_O} \quad (12)$$

At T=n+1 again the diode D is forward biased when mosfet M is switched off. At T=n+1 the capacitor voltage $V_{CO}(n+1)$ and inductor current $I_{LO}(n+1)$ can be expressed as

$$I_{LO}(n+1) = I_{LO}\left(n+1-\frac{D}{2}\right) + S_{L1}\frac{T_{ON}(n)}{2}$$

$$V_{CO}(n+1) = V_{CO}\left(n+1-\frac{D}{2}\right) + \frac{1}{C_O}\int_0^{\frac{T_{ON}(n)}{2}} I_{CO}\,dt$$

$$= V_{CO}\left(n+1-\frac{D}{2}\right) + \frac{I_{LO}(n)-I_O}{C_O}T_{ON}(n)$$

$$-\frac{S_{L2}T_{ON}(n)T_{OFF}(n)}{2C_O} + \frac{3S_{L1}T_{ON}^2(n)}{8C_O} \quad (13)$$

From equation (6), in nth cycle the T_{ON} of mosfet M can be obtained as

$$T_{ON} = \frac{V_C(n)-V_S(n)}{(S_1+S_2)} + \frac{S_1 T}{S_1+S_2} \quad (14)$$

The complete sampled-data model of the V/C digital controlled buck converter composed in equations (4.2)–(4.5). For stability analysis a jacobian matrix is derived in the steady-state point by linearsing the nonlinear functions $I_{LO}(n+1)$ and $V_{CO}(n+1)$ with respect to $I_{LO}(n)$ and $V_{CO}(n)$. The Jacobian matrix **J** is written as

$$J = \begin{bmatrix} J_{11} & J_{12} \\ J_{21} & J_{22} \end{bmatrix} \quad (15)$$

Where $I_{LO}(n)$ and $V_{CO}(n)$ steady-state values are denoted by I_{LO} and V_{CO}, respectively. From (3.3) and (4.1)–(4.5), J_{11}, J_{12}, J_{21}, and J_{22} can be obtained as

$$J_{11} = \frac{\partial I_{LO}(n+1)}{\partial I_{LO}(n)} = 0$$

$$J_{12} = \frac{\partial I_{LO}(n+1)}{\partial V_{CO}(n)} = -\frac{W_2}{W_1+W_2R_{ESR}}$$

$$J_{21} = \frac{\partial V_{CO}(n+1)}{\partial I_{LO}(n)} = \frac{T}{2C_O}$$

$$J_{22} = \frac{\partial V_{CO}(n+1)}{\partial V_{CO}(n)}$$

$$= 1 - \frac{W_2 T}{2C_O(W_1+W_2R_{ESR})} \quad (16)$$

Then, the two eigen values λ_1 and λ_2 of J are derived as

$$= \frac{(J_{11}+J_{22}) \pm \sqrt{(J_{11}+J_{22})^2 - 4(J_{11}J_{22}-J_{12}J_{21})}}{2} \quad (17)$$

The stability of the V/C digital controlled buck converter needs that the two eigen values should be inside the unit circle. Therefore, the eigen values are $|\lambda_{1,2}|<1$ if

$$R_{ESR} > R_{CRITI} = \frac{T}{2C_O} - \frac{W_1}{W_2} \quad (18)$$

Where R_{CRIT} is the minimum value of ESR where the system work steadily. Equation (18) represents V/C digital controlled buck converter stability boundary condition, From equation(18), we can say that the duty cycle doesn't affect the stability of V/C digital controlled buck converter, it can be found by output capacitor, switching period and inductor current and output voltage weighting factors. In full range of the duty cycle When ESR is larger than R_{CRIT} the system can work stably. The system is unstable when the ESR of output capacitor is smaller than R_{CRIT}, but by raising the W_1/W_2 ratio the system can be made stable.

B. Load Transient Performance Analysis using z-domain Small Signal Modeling

From the theoretical view, in order to research the transient performance of V/C digital controlled buck converter, the z-domain small-signal modeling is executed. The open loop transfer functions of buck converter from V_G to I_{LO}, V_G to V_O are Figd out and output impedance are denoted by $G_{ID}(s)$, $G_{VD}(s)$, and $Z_{OUT}(s)$, respectively [28], and they can be expressed as

$$G_{VD}(s) = \frac{V_{IN}R_O(C_OR_{ESR}s+1)}{L_OC_O(R_O+R_{ESR})s^2+(C_OR_OR_{ESR}+L_O)s+R_O}$$

$$G_{ID}(s) = \frac{V_{IN}(C_O(R_O+R_{ESR})s+1)}{L_OC_O(R_O+R_{ESR})s^2+(C_OR_OR_{ESR}+L_O)s+R_O}$$

$$Z_{OUT}(s) = \frac{C_OR_OR_{ESR}L_Os^2+R_OL_Os}{L_OC_O(R_O+R_{ESR})s^2+(C_OR_OR_{ESR}+L_O)s+R_O} \quad (19)$$

Here, the transfer function from I_O to I_{LO} of buck converter denoted by $A_I(s)$, which is

$$A_I(s) = \frac{R_OR_{ESR}}{(R_O+R_{ESR})L_O}\frac{s+\omega_z}{s^2+2\xi\omega_0 s+\omega_0^2} \quad (20)$$

Where,

$$\xi = \left(C_OR_OR_{ESR}+L_O\right)/\left(2(L_OC_OR_O(R_O+R_{ESR}))\right)^{1/2},$$

$$\omega_0 = \left((R_O/(L_OC_O(R_O+R_{ESR})))\right)^{1/2}$$

The z-domain transfer functions can be obtained from s-domain form by applying the Tustin approximation [28], which can be expressed as

$$G_{VD}(z) = \frac{V_{IN}T[(2C_OR_{ESR}+T)z^2+2Tz+T-2C_OR_{ESR}]}{L_OC_O(\propto_2 z^2+\propto_1 z+\propto_0)}$$

$$G_{ID}(z) = \frac{V_{IN}T[(2C_O(R_O+R_{ESR})+T)z^2+2Tz+T-2C_O(R_O+R_{ESR})]}{L_OC_O(\propto_2 z^2+\propto_1 z+\propto_0)}$$

$$Z_{OUT}(z) = \frac{2(2C_OR_{ESR}+T)z^2-8C_OTz-2T+4C_OR_{ESR}}{C_O(\propto_2 z^2+\propto_1 z+\propto_0)}$$

$$A_I(z) = \frac{(2C_OR_{ESR}+T)z^2+2Tz+T-2C_OR_{ESR}}{\left(\frac{\rho}{T}+T+\rho\omega_z\xi\right)z^2-2\left(\frac{\rho}{T}-T\right)z+\frac{\rho}{T}+T-\rho\omega_z\xi} \quad (21)$$

Where

$$\propto_0 = 4\left(1+\frac{R_{ESR}}{R_O}\right)+\frac{T^2}{L_OC_O}-2T\left(\frac{R_{ESR}}{L_O}+\frac{1}{C_OR_O}\right)$$

$$\alpha_1 = \frac{2T^2}{L_O C_O} - 8\left(1 + \frac{R_{ESR}}{R_O}\right)$$

$$\alpha_2 = 4\left(1 + \frac{R_{ESR}}{R_O}\right) + \frac{T^2}{L_O C_O} - 2T\left(\frac{R_{ESR}}{L_O} + \frac{1}{C_O R_O}\right)$$

$$\rho = \frac{4L_O C_O (R_O + R_{ESR})}{R_O}$$

As in Fig-2, each variable is the combination of an ac component and dc component which replicate the response to this disturbance as indicated in

$$V_S(n) = V_S + \bar{V}_S(n)$$
$$V_C(n) = V_C + \bar{V}_C(n)$$
$$D(n) = D + \bar{D}(n) \quad (22)$$

Where V_C, V_S, and D are the dc components, and $\bar{V}_C(n)$, $\bar{V}_S(n)$, and $\bar{D}(n)$ are the ac components. Neglecting the nonlinear ac terms and substitute (22) into (4), the ac small-signal equation and dc equation can be obtained as

$$V_C = V_S + (S_1 + S_2)DT - S_2 T$$

$$\bar{V}_C(n) = \bar{V}_S(n) + (S_1 + S_2)T\bar{D}(n) \quad (23)$$

The ac small-signal equation can be rephrase as

$$\bar{D}(n) = \frac{L_O}{(W_1 + W_2 R_{ESR})V_{IN} T}\left[\bar{V}_C(n) - \bar{V}_S(n)\right] \quad (24)$$

By converting equation (24) to the z-domain, the D(z) can be obtained as

$$D(z) = F[V_C(z) - V_S(z)] \quad (25)$$

Where $F = L/(W_1 + W_2 R_{ESR})V_{IN} T)$

By ignoring the delays and quantization errors of ADC, the transfer function of ADC can be stated as

$$G_{ADC} = \frac{2^N}{V_{REF}} \quad (26)$$

Where V_{REF} is the reference voltage of ADC and N is the number of bits of ADC.Based upon D-PID algorithm as (4) the compensator is designed. The related D-PID z-domain representation can be stated as

$$G_c(z) = K_P + K_I \frac{z}{z-1} + K_D \frac{z-1}{z} \quad (27)$$

The V/C digital controlled buck converter z-domain small-signal diagram is achieved based on (21)–(27) and is shown in Fig-5. By using Mason's law the closed-loop output impedance transfer function can be derived, and it is expressed as

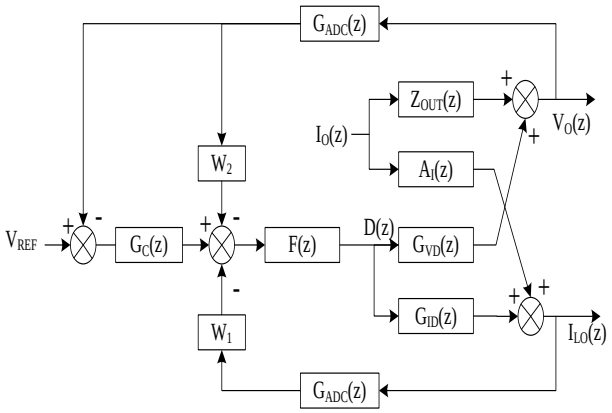

Fig-5 - V/C digital Controlled Buck Converter z-domain small signal diagram

The V/C digital controlled buck converter z-domain small-signal diagram is achieved based on (21)–(27) and is shown in Fig-5. By using Mason's law the closed-loop output impedance transfer function can be derived, and it is expressed as

$$Z_{C-OUT}(z) = \frac{Z_{OUT}(z) + W_1 G_{ADC}(z)F(z)[G_{ID}(z)Z_{OUT}(z) - G_{VD}(z)A_I(z)]}{1 + G_{ADC}(z)F(z)[W_2 G_{VD}(z) + G_C(z)G_{VD}(z) + W_1 G_{ID}(z)]} \quad (28)$$

Based on the z-domain small signal modeling and above analysis, the simulation of V/C digital controlled buck converter is done by using MATLAB by selecting the circuit parameters as required. The closed loop output impedance magnitude is increased by keeping W_2 constant and increasing W_1 which gives slower load transient response speed. The closed loop output impedance magnitude is decreased by keeping W_1 constant and increasing W_2 which gives the faster load transient response speed.Therefore, it can be finalized that the output voltage and inductor current weighting factors influence the load transient performance of the system. The system has inferior load transient response when the ratio of W_1/W_2 increases and the system has superior load transient response when the ratio of W_1/W_2 decreases

Table-I - V/C digital controlled buck converter components and its significance

Component	significance
Input voltage(V_{IN})	100V
Switching period(T)	0.02s
Output inductor(L)	0.5H
Output Capacitor(C)	20 μF
ESR of output capacitor(R_{ESR})	500 Ω
Load resistance(R)	10 Ω

Based on the earlier transient performance and stability analyses, it can be finalized that when the ratio of W_1/W_2 is huge, the load transient response of the system becomes narrow but the range of system stability becomes broad. Therefore, the choice of W_1 and W_2 is the tradeoff between the load transient responses stability of the system.

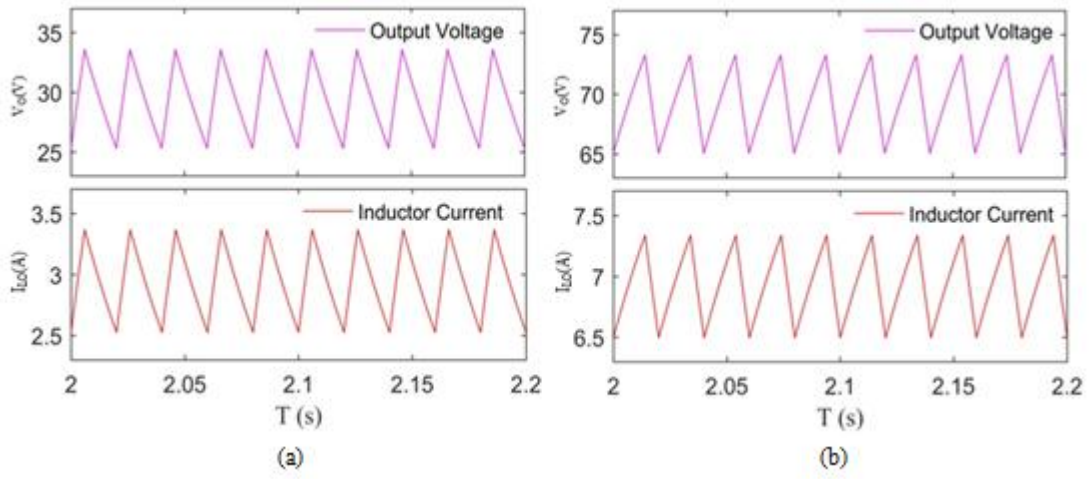

Fig-7 - Output voltage and inductor current simulation waveforms of V/C digital controlled buck converter. (a) V_O = 30 V and D < 0.5. (b) V_O =70 V and D > 0.5

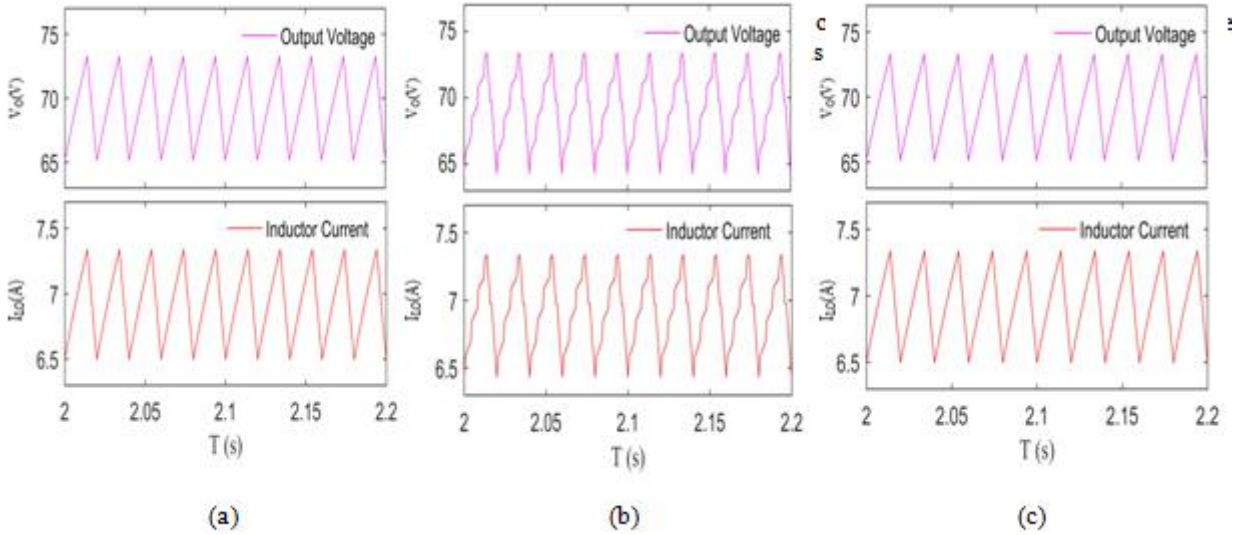

Fig-8 - Output voltage and inductor current simulation waveforms with different W_1, W_2 and R_{ESR}. (a) W_1 = 2, W_2 = 0.006, and R_{ESR} = 200Ω. (b) W_1=2, W_2=0.006, and R_{ESR} =300Ω. (c) W_1 =2, W_2 =0.008, and R_{ESR} =300Ω.

Table-II - Load transient performance simulation results of V/C digital controlled buck converter in three cases

Weighting Factors	Load steps from 10A to 20A		Load steps from 20A to 10A	
	Undershoot voltage/V	Setting time/S	Overshoot voltage/V	Setting time/S
W_1=1,W_2=0	50	1.3	140	0.5
W_1=0.5,W_2=0.5	30	0.5	80	0.4
W_1=0,W_2=1	20	0.2	50	0.2

IV. SIMULATION RESULTS OF V/C DIGITAL CONTROLLED BUCK CONVERTER

To verify the transient performance and stability analysis of proposed control, simulation of V/C digital controlled buck converter is carried out by using MATLAB. The parameters used in simulation as the same as in table-I.

A. Stability performance verification

To verify the stability boundary condition of V/C digital controlled buck converter, on the system stability the influence output voltage and inductor current weighting factors and duty cycle are examined by simulation. Taking W_1=0.5 and W_2=0.5, V/C digital

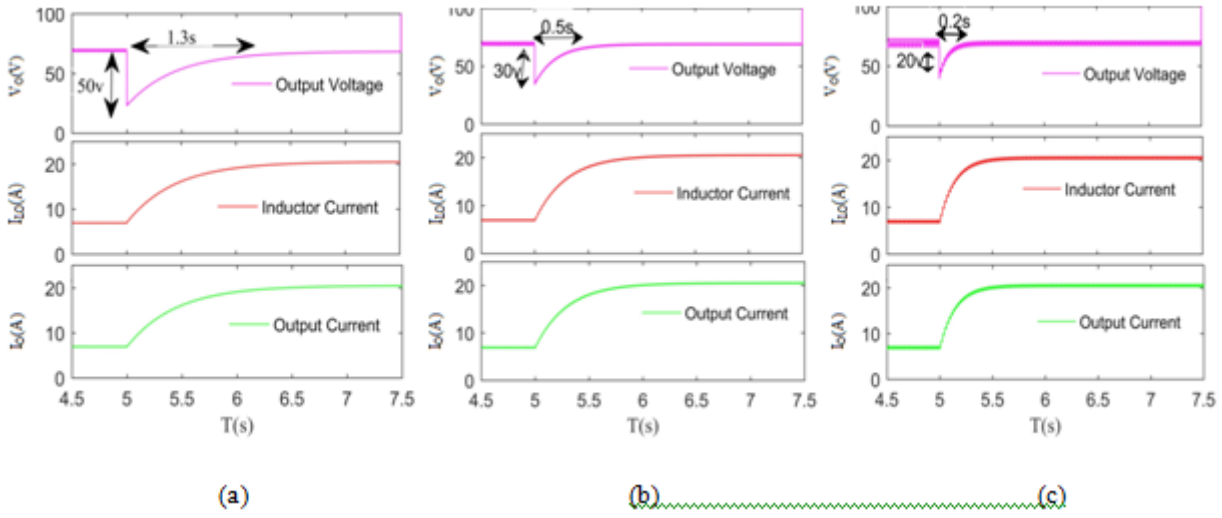

Fig-9 - Transient analysis simulation waveforms with load steps from 8A to 20A.(a) W_1 = 1, W_2=0 (b) W_1=0.5, W_2=0.5(c) W_1 =0, W_2 =1.

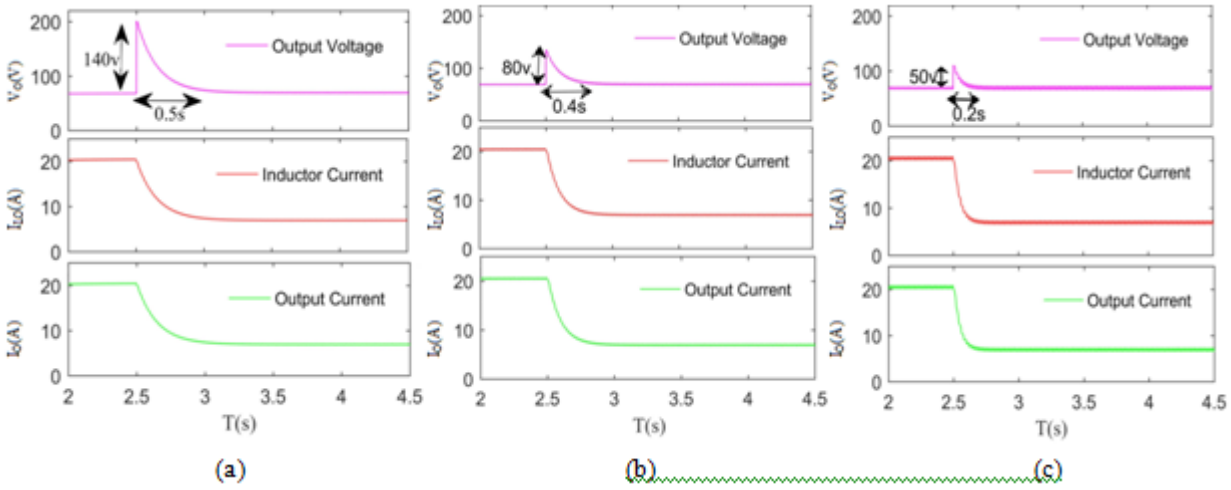

Fig-10 - Transient analysis simulation waveforms with load steps from 20A to 8A. .(a) W_1 = 1, W_2=0 (b) W_1=0.5, W_2=0.5(c) W_1 =0, W_2 =1.

controlled buck converter is simulated and waveforms of inductor current and output voltage are shown in Fig-6 representing the situation D > 0.5 and D < 0.5. As shown in Fig-6, the system is stable ether D < 0.5 or D > 0.5 and the sub-harmonic oscillation are eliminated in the system. Therefore, it can prove that at any value of duty cycle the V/C digital controlled buck converter is stable when the ESR of output capacitor satisfies the stability boundary condition, and the system has good output voltage accuracy.

The simulation waveforms of V/C digital controlled buck converter are shown in Fig-8 with different W_1, W_2 and R_{ESR}. The weighting factors are chosen as W_1=2, W_2=0.006 in Fig-8(a) and (b). The R_{CRIT} is obtained as 170Ω by (18). When R_{ESR} =200Ω, the ripple is small and the output voltage is stable and it is shown in shown in Fig-8(a) and (b). When R_{ESR} = 300Ω, the ripple becomes large as the low-frequency oscillation occurs. According to (18), keeping W_1 is as constant i.e., 2, increasing W_2 from 0.006 to 0.008, R_{CRIT} becomes 250Ω. In Fig-8(c) the simulation waveform with R_{ESR}=300Ω are shown. From Fig-8(c), it can be observed that the low-frequency oscillations are eliminated and the output

In the above simulation waveforms the stability boundary of V/C digital controlled buck converter is accurate. At any value of duty cycle V/C digital controlled buck converter has output voltage accuracy and it is stable. By regulating the ratio of W_1/W_2 the stability range can be extended.

B. Load Transient Performance Verification

In this section, three cases are assumed to verify the load transient response of V/C digital controlled buck converter simulation output waveforms. They are 1) W_1 and W_2 are 1 and 0 respectively; 2) W_1 and W_2 both 0.5; 3) W_1 and W_2 are 0 and 1 respectively. Fig-9 and 10 shows the transient analysis simulation waveforms of input current and output voltage. In Fig-9 the load steps from 8A to 20A. In Fig-10 load steps from 20A to 8A. To compare three cases, the overshoot and undershoot voltages and settling times of output voltage have been viewed in Table-II.

When the ratio of W_1/W_2 is small the output voltage overshoots or undershoots is reduced and the load transient response is sooner. When the ration of W_1/W_2 is high the output voltage overshoots or undershoots is increased and the load transient response goes slow down.

From this we can justify the by adjusting the inductor current and output voltage weighting factors of V/C digital control can attain rapid load transient performance.

The simulation results show that the inductor current and output voltage weighting factors of V/C digital control influence the load transient performance and the stability of the system. When the ratio of W_1/W_2 increases the stability range of V/C digital controlled buck converter becomes wider but the load transient response becomes inferior, when the ratio of W_1/W_2 decreases the narrow stability range of V/C digital controlled buck converter becomes, but the load transient response becomes superior. Therefore, the value of W_1 and W_2 is tradeoff between the load transient responses and the stability of the system.

The advantages of the V/C digital control are mentioned below. It has over current protection, perfect power management, and over voltage protection. It has good stability at any value of duty cycle, good robustness to the system parameters and strong anti-interference ability. Additionally, its dependence on ESR of output capacitor can be adjusted by changing the ratio of the output voltage and inductor current weighting factors. The V/C digital control has fast load transient performance, and can be adjusted by changing the ratio of the output voltage and inductor current weighting factors.

V. CONCLUSION

In this paper, the circuit and operating principle of V/C digital controlled buck converter is discussed. Sampled data modeling has been analyzed to obtain the stability boundary condition of V/C digital controlled buck converter, which shows that V/C digital control can work stably at any value of duty cycle and does not suffer the ESR limitation by adjusting the ratio of the output voltage and inductor current weighting factors. The V/C digital control technique has tough parameter tolerance. It is shown by robustness analysis. In addition, the z-domain small signal model has been analyzed to obtain the load transient response of V/C digital controlled buck converter which shows that the load transient performance of V/C digital control can be improved by adjusting the ratio of the output voltage and inductor current weighting factors. Finally, it is proven by simulation that the proposed V/C digital control has high voltage regulation accuracy, wide range of stability, and fast load transient response, good robustness and can achieve over current protection.

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