International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-9 Issue-3 September 2020

FPGA Implementation of Memory Bists using Single Interface

P. Ramakrishna, T. Vamshika, M. Swathi

Abstract: ***The development of IC integration technologies leads to an extensive use of memories and buffers in different memory intensive applications. Therefore, probability of occurrence of fault in every single read and writes operation is increased in Memory BIST (MBIST). There were many testing approaches that were developed for efficient testing and diagnosis of fault. However, all algorithms are not strengthened enough to detect all possible faults that may be present due to fabrication errors or environmental disturbance. Keeping this in mind and taking the possibility of development of efficient algorithm a hybrid memory testing algorithm is presented. To overcome those drawbacks, pipelining based MBIST designed to detect the all the types of memory faults by utilizing March-C testing algorithm. By introducing the Pipelining approach, majorly path delays are reducing. The proposed architecture designed and verified using Xilinx ISE environment under various testing methods with respect to the different category of memories. The simulation and synthesis results shows that the proposed method shows the enhanced performance with the hardware resource utilization and delay consumption compared to the conventional approaches.***

Keywords: DFT, MBIST, PRPG, RAM, SOC, VLSI

I. INTRODUCTION

With the continuous growth in semiconductor memory design and testing, the test time and its coverage become major problem and challenges for the industries and research groups [1]. The introduction of system chips has raised new problems for researchers at every stage of integration. Memory density and area are increasing day by day in embedded memory cores and SOCs. Thus on-chip memory yield defines the major portion of chip yield which can be improved with memory diagnosis and failure analysis (FA) methodologies [2]. The March tests are very convenient and efficient for testing RAM and are normally used with small test sizes [3]. The operation of each memory element/cell is set by the simulation test engine by fetching test-inputs. The cells that cannot give expected read output assume as faulty and its information is described in fault descriptor. Every fault descriptor has predefined conditions from which fault coverage can be calculated The integration problem increases with the advancement in submicron technologies that has different modules which contain high density memory cores and millions of gates but have pad limitations, switches to SOCs having embedded memories [4]. The market share of embedded memories is increasing day by day, so is the testing problems. In embedded memories. The challenges like performance, reliability and quality with the cost trade-off requires more attention of research and industrial community, including the problem of merging and integration of memory with logic [5]. The embedded memory is hard to test than an individual memory product due to accessibility problem of external tester [6]. Proper eorts using Design for Testability (DFT) are required for managing tradeoff between number of factors affecting area, power, speed, reliability; the choice of external tester suffers from availability and high cost issues [7]. So, in order to reduce the additional cost in terms of external tester an extra circuitry is embedded in the memory itself, called Memory-BIST (MBIST). In this paper MBIST developed based on proposed Pipelined March-c approach which provides a suitable framework for testing of memories, which is embedded in System on Chip (SOCs) and Memory cores. Thus, the major contributions of this paper as follows

- Designed and implemented the new architectures for Soc interface, test control, pipeline multiplexer with horizontal and vertical memory modules and Pipeline Multiplexer modules.
- Developed the new March-C algorithm with pipelining concept in MBIST.
- Developed the MBIST model with enhanced fault coverage model by controlling the multiple numbers of faults.
- Introducing the different Faults to generated in RAM and developed the fault detection and correction mechanism using pipelined March-C approach.

Rest of the paper as follows: section 2 discuss about the detailed analysis of various related works and its problems. Section 3 deals about the Developed of new March-C algorithm with pipelining concept in MBIST Developed the new March-C algorithm with pipelining concept. Section 4 discusses about the detailed analysis of experimental results of area, power and delay properties and compared to the state of art approaches. Section 5 discuss about the conclusion and future work.

Revised Manuscript Received on August 05, 2020.
***** Correspondence Author
P. Ramakrishna, Associate professor, Department of Electronics and Communication Engineering, Anurag University, Hyderabad, India. E-mail: ramakrishnaece@cvsr.ac.in
T. Vamshika, P.G. Scholar, Department of Electronics and Communication Engineering, Anurag University, Hyderabad, India. E-mail: tvamshika11@gmail.com
M. Swathi, Assistant professor, Department of Electronics and Communication Engineering, Vignana Bharathi Institute of Technology, Hyderabad, India. E-mail: msrk910@gmail.com

II. LITERATURE SURVEY

In [8-9] authors have used Iddq testing for fault detection, Iddq testing or Idd (quiescent) was useful for detecting bridging and gate oxide defects but could't detect an open defect.

Partitioned a large system core into two cores and proposed greedy heuristic and a genetic algorithm that were applied on 14-core SOC and found that the genetic algorithm yields near-optimal results In [10-11] authors have used applied current test on Static RAM using Power-Gating technique that could be applied in Nanotechnologies. For this a modified decoder was proposed that can generate test patterns using check-board logic test and power-gating current test. The current resolution was also retrieved upto 40 dB while simulated in a 0.13 micro meter technology. In [12-13] authors have proposed settling aspects related to IDDQ testing that can be used as a standard in the measurement of timing and quality. With the use of Load board based module (LBM) , thousands of IDDQ measurements were obtained which enables the high fault coverage for IDDQ. In [14] authors have proposed a model for digital circuits operating at March-C approach utilized MBIST to evaluate their performance. The proposed technique minimized the energy by reducing VDD, keeping same delay and yield proles. The author achieved more and more percent of power reduction and its leakage under reduced bias of various voltages applied on SRAM test chip.

III. PROPOSED MBIST ARCHITECTURE WITH PIPELINING

This section recapitulates the concepts, salient features, structures and functionalities of MBIST. ertain and some unpredictable changes in manufacturing and semiconductor industries cause VLSI circuits to face various challenges during designing, assembling, screening and testing phase. Conventional Automatic Test Pattern Generators (ATPG) with software support can't give high fault coverage due to their hardware dependency and operating limitation and available at quite high cost. With this functionality, MBIST is capable to generate test patterns specific for the design. These test responses matched with the correct responses using analysis through the Output Response Analyzer (ORA) of corresponding Memory under Test. The mismatching found in responses then chip is declared as faulty chip. The MBIST classification is categorized in two broad categories Online & Offline- MBIST. Once the checking is completed and the comparator output confirms that the output of memory and data in Memory under Test is same then memory is good for use. Otherwise corresponding address is being stored in the fault dictionary for doing repairing actions according to redundancy analysis algorithms. A MBIST hardware structure is developed using the proposed Pipelined March-c approach algorithm with suitable hardware description, the top-level module entity is as shown in Figure 1. The general simulation problem and circuit module is same as that of only the MBIST Controller module is changed which is based on Pipelined March-c approach. The presented MBIST hardware structure has major main units: Soc interface, Test control, memory interface module based on Pipelined March-c approach and BIST Controller to generate the necessary control signal for the working of MBIST.

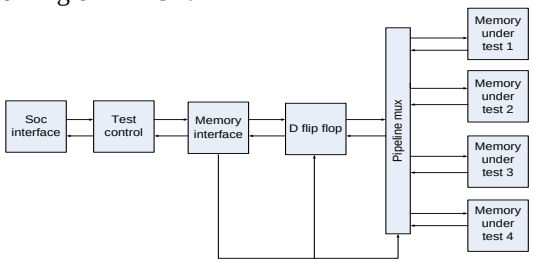

Figure 1. Pipeline architecture

For the testing of proposed Pipelined March-C algorithm a MBIST hardware structure for RAM is developed, that consist of a Test controller to control the ordering of marching, marching element state sequences and even, odd trace of loop through memory interface. The Pipeline multiplexer module that work is to check the output response according to mismatching of data output and the data available in the output response analyzer. If data matching is different, then the concerned location is stored in the fault dictionary. The fault dictionaries have the details of addresses in terms of row and column of RAM. This information is useful for further repairing solutions of the memory available in the fault dictionary. The working modes on fault dictionary as follows:

Normal Mode: No testing operation is being done and memory does its basic operations. In order to include fault tolerant feature and to ensure the correct operation in RAM the input data is placed in Pipelined Multiplexer, if the read data from memory cell is different than data in Memory under test. it indicate that there is a fault in that location, the input data is then made available in the backup buffer in spite of occurring fault in that location.

Testing Mode: In testing mode, whole RAM is tested using proposed hybrid Pipelined March-c approach testing algorithm and if fault occurs a fault dictionary containing row and column wise address detail of address index will be created that will help for further repair actions. The presented algorithm takes best suitable procedures from both conventional algorithms and provides a suitable framework for fault detection and diagnosis. The proposed MBIST contains Soc interface for analyzing its performance and fault coverage against injected fault covering stuck open faults, stuck at faults, transition faults and coupling faults and implemented using Test control to analyze its hardware related parameters like area, delay and power for all operations. The transition faults and coupling faults are injected keeping assumption that only two cells exhibit this nature. The proposed algorithm also proves better as compared conventional pipeline free March-C algorithm in terms of better fault coverage however still having some power related issues. It depends on hybrid marching technique to test SRAM. As in the Pipelined March-C algorithm, the pattern `0' or `1' is filled in memory with even and odd locations in pipelining manner. In March C- algorithms according to March element Memory under tests from M1 to M4 the patterns are successive pipelined read and write operations are performed.

The proposed algorithm combines Memory under tests elements by pipelining reading and writing on even and odd locations according to marching patterns in D flip flops. The main benefit of marching at even and odd locations is that three fault profiles i.e. transition faults, coupling faults and bridging faults can easily covered as compared to conventional pipeline free March-C algorithm.

The proposed MBIST mechanism can be able to solve the various types of faults; they are

1. Stuck at fault (SAF): By this fault the data stored in the memory are stick to fixed logical value either 1 or 0.
2. Stuck open Fault (SOF): this fault generated due to path broken and read, write memory interrupts.
3. Transition fault (TF): This fault occurred due to sudden change in the data due to parallel occurrence of read, write operations in the same address of memory. So the data in the address changed from one logical level (0/1) to another logical level (1/0).
4. Coupling fault (CF): By this fault data in the one memory address is affected by its nearest address while performing the read, write operations.
5. Neighborhood pattern sensitive fault (NPSF): this fault is same as the CF, but due to this fault same data can be stored in multiple addresses while performing write operation.
6. Address fault (ADF): due to this fault, memory cells and corresponding address locations will not useful to store the data. The data stored in that address is permanently losses.

The proposed method can be effectively detects and corrects all these type of faults and detailed comparison of various algorithm is presented in table 1. From the table it is observed that the proposed methodology effectively detects and corrects the faults compared to conventional alogrithums.

Table 1: Fault model detection

Algorithm	FAULTS						Complexity
	SAF	SOF	TF	CF	ADF	NPSF	
Checkerboard	DC	-	-	-	-	-	4N
GALPAT	DC	DC	DC	DC	-	-	4N*N
BUTTERFLY	DC	DC	-	-	-	-	5N log N
MATS	DC	-	-	-	-	-	4N
MATS+	DC	DC	-	-	-		5N
Marching 1/0	DC	DC	DC	-	DC	-	14N
MATS++	DC	DC	DC	DC	-	DC	6N
March X	DC	DC	DC	-	DC	-	6N
March C (conventional)	DC	DC	DC	DC	DC	-	11N
March C (Pipelining)	DC	DC	DC	DC	DC	DC	8N

Here in the above table, 'DC' means fault Detection and correction; '-' fault detection and correction not possible; 'N denotes the complexity of fault detection and correction.

IV. EXPERIMENTAL RESULTS

All the proposed designs have been programmed and designed using Xilinx ISE software this software tool provides the two categories of outputs named as simulation and synthesis. The simulation results give the detailed analysis of proposed design with respect to inputs, output byte level combinations. Through simulation analysis of accuracy of the addition, multiplication process estimated easily by applying the different combination inputs and by monitoring various outputs. Through the synthesis results the utilization of area with respect to the programmable logic blocks (PLBs), look up tables (LUT) will be achieved. And also time summary with respect to various path delays will be obtained and power summary generated using the static and dynamic power consumed.

Table 2: comparison table

parameter	BIST [8]	MBIST [11]	LBIST [9]	March-c[14] (conventional)	March-c Pipelined
Time delay	8.28 ns	7.24 ns	6.13 ns	4.858ns	2.674ns
Frequency	124.56	189.39	230.92	204.846MHz	373.986MHz
Power utilized	2.364 uw	2.49 uw	2.593 uw	1.293uw	0.143 uw
LUT	120	92	93	70	53
Slice Reg	112	90	83	49	29

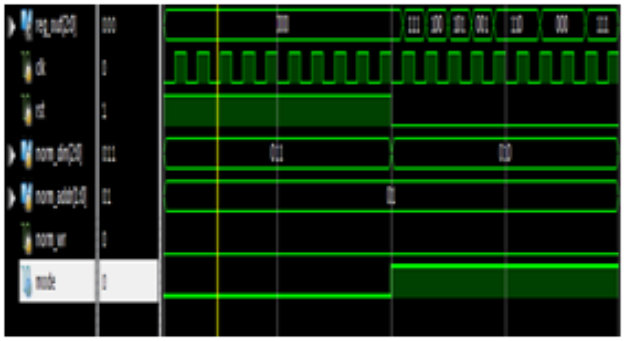

Figure 2: Simulation output

From figure 2, it is observed that if mode selection is one the proposed Pipelined March-C algorithm on RAM consumes less clock cycles for fault detection and correction compared to the conventional March-C algorithm with corresponding normalized din with respect to the address stored of RAM. If mode selection is zero there is no fault occurred and din will be transferred to the reg_out without any delay and fault respectively.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	29	408000	0%
Number of Slice LUTs	53	204000	0%
Number of fully used LUT-FF pairs	29	53	54%
Number of bonded IOBs	12	600	2%
Number of BUFG/BUFGCTRL/BUFHCEs	1	200	0%

Figure 3: Design summary

The Figure 3 represents the synthesis implementation by using the Xilinx ISE software. From the table, it is observed that only 53 look up tables are used out of available 20400 and 29 slice registers are used out of available 408000. It indicates less area was used for the proposed design compared to the conventional approaches.

From the table 2, it is observed that the proposed method consumes very less area, power and delay and shows faster fault detection as well as correction compared to the conventional approaches such as BIST [8],MBIST [11],LBIST [9] and March-c[14] conventional) respectively.

V. CONCLUSION

MBIST is an emerging and promising future in memory intensive applications of SOC designs and is expected to play a vital role in high reliable and accurate system design. There is a significant research work which has been carried out in context of MBIST designs and its architectures but comparatively less effort were put in for fault detection and correction. As an outcome, this research empirically proves that March C-pipelined test algorithm performs the best as compared to other types of memory testing algorithm in terms of fault coverage, complexity and percentage of resource utilization**.** The work can be extended to Parallel and Serial Architecture helps to testing the available memories in soc using March c in an efficient way. Repairing algorithms are used in further to repair the faulty memories. Fast testing helps in fast repair there by reduces the throughput and latency of memories being tested.

REFERENCES

1. Ogasahara, Yasuhiro, et al. "Implementation of pseudo-linear feedback shift register-based physical unclonable functions on silicon and sufficient Challenge–Response pair acquisition using Built-In Self-Test before shipping." Integration 71 (2020): 144-153.
2. LIANG, Huaguo, et al. "A novel BIST scheme for circuit aging measurement of aerospace chips." *Chinese Journal of Aeronautics* 31.7 (2018): 1594-1601.
3. DeMara, R. F., N. Imran, and R. A. Ashraf. "Emerging Resilience Techniques for Embedded Devices." *Rugged Embedded Systems: Computing in Harsh Environments, Elsevier Publishing*.
4. Jamal, K., K. Manjunatha Chari, and P. Srihari. "Test pattern generation using thermometer code counter in TPC technique for BIST implementation." *Microprocessors and Microsystems* 71 (2019): 102890.
5. Kumar, Mahesh. "An Efficient Fault Detection of FPGA and Memory Using Built-in Self Test [BIST]." *American Journal of Electrical and Computer Engineering* 3.1 (2019): 38-45.
6. Harutyunyan, Gurgen, Samvel Shoukourian, and Yervant Zorian. "Fault Awareness for Memory BIST Architecture Shaped by Multidimensional Prediction Mechanism." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 38.3 (2018): 562-575.
7. Lee, Kuen-Jong, Bo-Ren Chen, and Michael Andreas Kochte. "On-chip self-test methodology with all deterministic compressed test patterns recorded in scan chains." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 38.2 (2018): 309-321.
8. Lee, Sanghoon, et al. "A built-in self-test andin situanalog circuit optimization platform." IEEE Transactions on Circuits and Systems I: Regular Papers 65.10 (2018): 3445-3458.
9. Moghaddam, Elham, et al. "Logic BIST with capture-per-clock hybrid test points." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 38.6 (2018): 1028-1041.
10. Efanov, Dmitry V., et al. "Synthesis of Built-in Self-Test Control Circuits Based on the Method of Boolean Complement to Constant-Weight 1-out-of-n Codes." *Automatic Control and Computer Sciences* 53.6 (2019): 481-491.
11. Balaji, G. Naveen, and S. Chenthur Pandian. "Design of test pattern generator (TPG) by an optimized low power design for testability (DFT) for scan BIST circuits using transmission gates." *Cluster Computing* 22.6 (2019): 15231-15244.
12. Moghaddam, Elham, et al. "Logic BIST with capture-per-clock hybrid test points." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 38.6 (2018): 1028-1041.
13. Cui, Xiaole, et al. "Design and Test of the In-Array Build-In Self-Test Scheme for the Embedded RRAM Array." *IEEE Journal of the Electron Devices Society* 7 (2019): 1007-1012.
14. Silveira, Reinaldo, Qadeer Qureshi, and Rodrigo Zeli. "Flexible architecture of memory BISTs." *2018 IEE 19th Latin-American Test Symposium.* IEEE, 2018.

AUTHOR PROFILE

P. Ramakrishna, born in East Godavari district, Andhra Pradesh. He received his B. Tech degree in Electronics and communications engineering from NIT Warangal, India. M. Tech degree in VLSI System Design from CVR College of Engineering JNT University Hyderabad India. He had 13 years of teaching and research experience. Presently he is pursuing Ph. D at K.L.E.F (Deemed to be University), Guntur, Andhra Pradesh, India. And Associate Professor Anurag University Hyderabad, Telangana. He has published 25 International Journals, and two patents. His research interests include VLSI System Design, Digital Signal Processing and Image processing, Deep Learning, Device modeling.

T. Vamshika, born in Nirmal, Telangana. She received her B. Tech degree in Electronics and Communications Engineering from AVNIET, JNT University, Hyderabad, India. M. Tech degree in VLSI System Design from Anurag University, Hyderabad, Telangana, India.

M. Swathi, born in Hyderabad, Telangana. She received her B. Tech degree in Electronics and Communications Engineering from MIST, JNT University, Hyderabad, India. M. Tech degree in VLSI System Design from CVR College of Engineering JNT University Hyderabad, India. She had 8 years of teaching and research experience. Presently working as an Assistant Professor at Vignana Bharathi Institute of Technology (Autonomous) Hyderabad, Telangana. She has published 5 International Journals, her research interests include VLSI System Design, Digital Signal Processing and Deep Learning.