Performance Measures of Different Gate Oxide Materials in Gate All Around Fet

S. Ahmad Saidulu, R.Sai Vineeth, Y.Tanmayee, B.Meenakshi

Abstract: ***The classical planar Metal Oxide Semiconductor Field Effect Transistors (MOSFET) is fabricated by oxidation of a semiconductor namely Silicon. In this generation, an advanced technique called 3D system architecture FETs, are introduced for high performance and low power quality of devices. Based on the limitations of Short Channel Effect (SCE), Silicon (Si) FET cannot be scaled under 10nm. Hence various performing measures like methods, principles, and geometrics are done to upscale the semiconductor. CMOS using alternate channel materials like GE and III-Vs on substrates is a highly anticipated technique for developing nanowire structures. By considering these issues, in this paper, we developed a simulation model that provides accurate results basing on Gate layout and multi-gate NW FET's so that the scaling can be increased few nanometers long and performance limits gradually increases. The model developed is SILVACO that tests the action of FET with different gate oxide materials.***

Keywords: Gaafet's; Gate Materials; Short Channel Effect (Sce); Sensitivity

I. INTRODUCTION

GAA is similar to FinFETs in some way except that the conducting channel is enclosed by a gate all around. So we get better channel controllability over the gate. When we push into nano-scale technology, the density of the transistors is growing. This deterioration is due to short channel effects such as subthreshold current, lowering of the barrier caused by the drain, etc. MOSFETs are replaced by a double gate or tri-gate transistors. Unlike multi-gate FETs, Gate All Around structures showed the advantage of strong channel-by-gate control. It has the best electric properties and conductivity.
The growth of nanowire transistors increases gradually by developing many technologies like 3D Nanowire (NW) and the combined characteristics of new materials and potential nature called CMOS. From the past 15 years, MOSFET's are channeled by Ge and III-V's on Si platform for the reduction of VDD. It is applicable for high and low-performance logics. If there is low effective mass, then there is a chance of high velocity so that CMOS reduces Gate oxides (Vg-Vth) which results in low VDD at those channels. An increase in channel width states that NW CMOS is more reliable than Fin FET's. Due to the wide range of channels integration advanced CMOS platform has not been implemented yet.

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II. SOFTWARE INTRODUCTION

The most efficient software tool for analog/mixed signals, power IC and memory design is Silvaco an EDA supplier. Since its establishment in 1984, Silvaco has developed to turn into the biggest secretly held EDA organization and keeps on developing reliably on the quality of its fantastic items, backing, and administration. The organization has been a brilliant illustration of the creative valley culture and endeavors to proceed with this heritage. Silvaco's strategy is to enable its clients to quicken the pace of mechanical advancement and their opportunity to showcase while diminishing their expenses in building up the cutting edge chips.

III. METHODOLOGY

The theoretical studies have been examined on the limitations of downscaling transistors with sub-10 nm nodes. There are many challenges to be faced concerning replacing silicon as MOSFET. Nanowire manufacturing is a technique that is developed based on its structure and its characteristics limited to the field of electronics. Every study states about the performance and efficiency of the materials, thus nanowire transistors are also making sure of implementing optimized techniques to improve the quality of the materials. Final results are performed based on downscaling MOSFET's in sub-10nm by the process of the sensitivity of silicon nanowire in the view of FET's.Gate oxide materials in All-Around FET had been thrived for a mimic Si-NW-GAA-FET by performing comparative analysis on silicon and III-V NW-GAA-FET which constitutes of distinct gate oxides. And, the results state that III-V transistors provide better performance when compared to silicon. For developing a simulation model different readings are taken and a simulated curve with this experiment data is generated. Calibration is performed using drain current as of its function and values of gate voltage as the axis in the curve. So, based on the generated simulation curves and experiment data there is a chance of concluding that the model is adjustable concerning distinct semiconductor channels and oxide materials. Hence, we can observe the improvement in the performance of III-V transistors when the silicon channel is replaced by the other oxide elements. Eventhough silicon is an abundant semiconductor on earth, its replacement can bring many salient features in the development of a transistor.

IV. RESULTS AND DISCUSSION

In this paper, we mainly concentrated on the different gate oxide materials for GAAFET through which the characteristics will be calculated from the graphs we obtained after the simulation in SILVACO software, and hence we can identify the Vd, Id, Rd from those graphs for different gate oxide materials. The materials we used are Hfo2, Sno2, Zno, Sio2.

The simulation results were attached below.

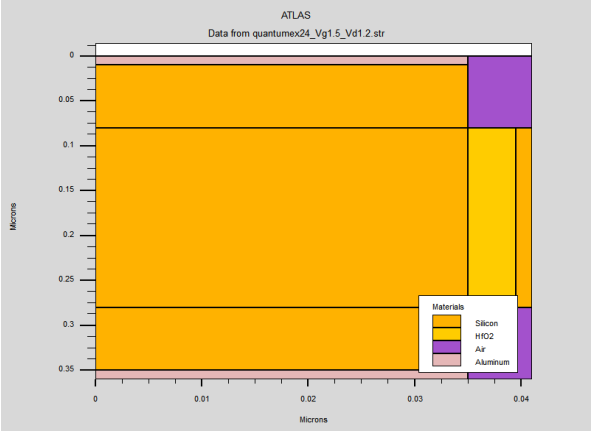

Fig 1:structure of the gate all around fet with hfo_2 as gate oxide material.

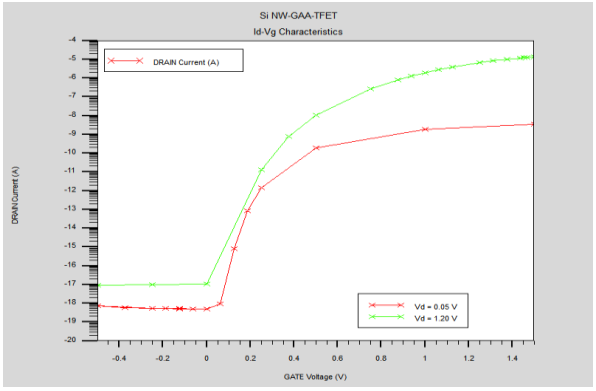

Fig 2:characteristics of the gate all around fet with hfo_2 as gate oxide material. for the applied vd of 1.20v and 0.05v ΔR obtained is 0.206Ω and 0.285Ω respectively.

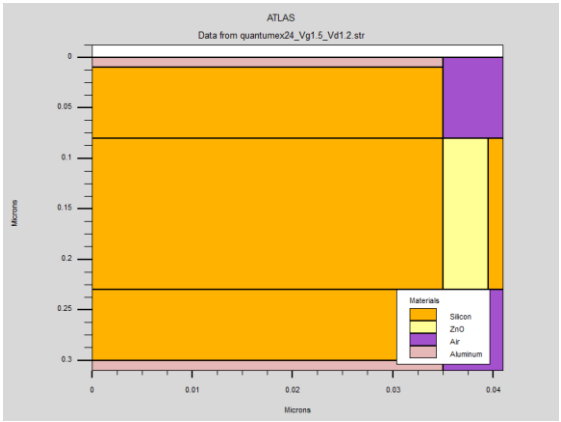

Fig 3:structure of the gate all around fet with ZnO as gate oxide material.

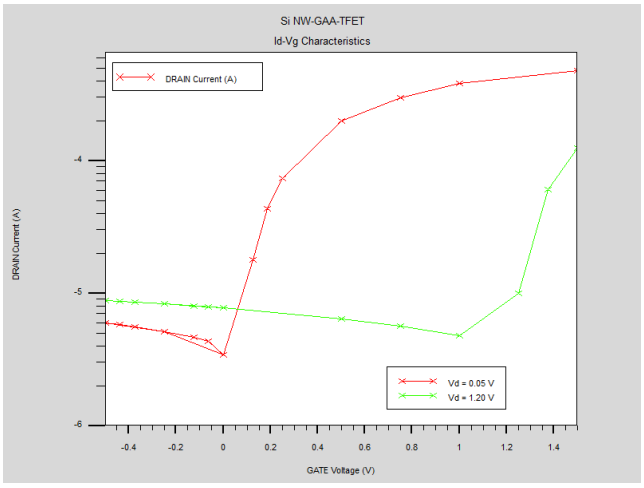

Fig 4:characteristics of the gate all around fet with ZnO as gate oxide material. for the applied vd of 1.20v and 0.05v ΔR obtained is -4Ω and 1.5Ω respectively.

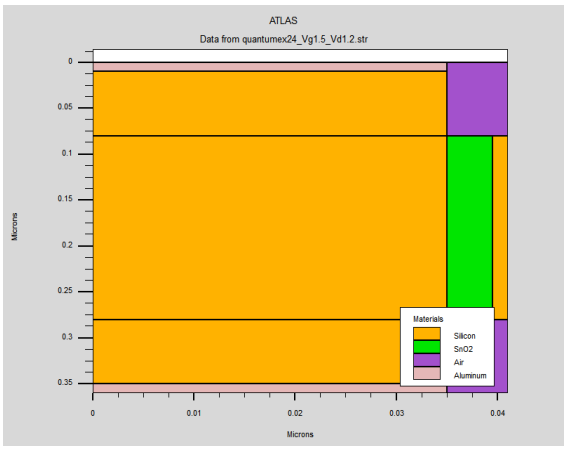

Fig 5:structure of the gate all around fet with sno_2 as gate oxide material.

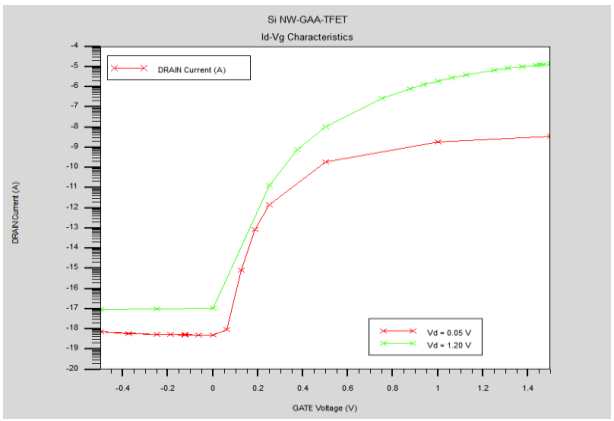

Fig 6:characteristics of the gate all around fet with sno_2 as gate oxide material. for the applied vd of 1.20v and 0.05v ΔR obtained is 0.125Ω and 0.146Ω respectively.

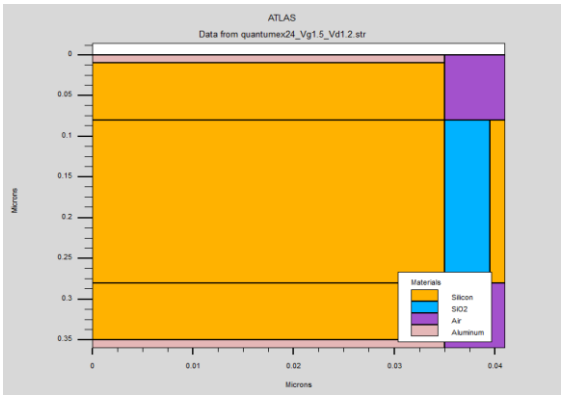

Fig 7:structure of the gate all around fet with sioo$_2$ as a gate oxide material

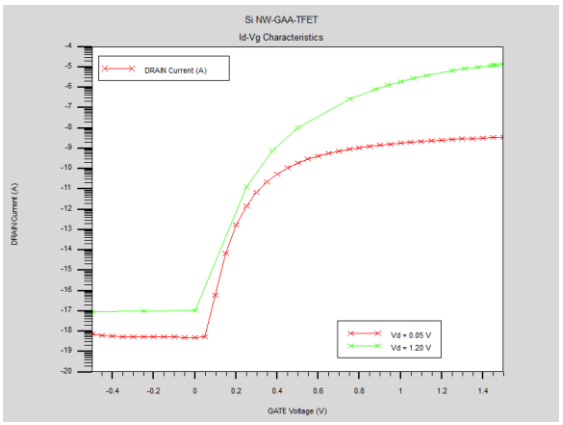

Fig 8:characteristics of the gate all around fet with sio$_2$ as gate oxide material. for the applied vd of 1.20v and 0.05v ΔR obtained is 0.181Ω and 0.375Ω respectively.

Table- I: V_d ,ΔV,ΔI,ΔR values for different gate oxide materials in Ground-all-around FET

Materials	V_d	ΔV	ΔI	ΔR
Sio_2	0.05	0.6	1.6	0.375
	1.20	0.6	3.3	0.181
Zno	0.05	0.6	0.7	1.5
	1.20	0.6	-0.15	-4
Hfo_2	0.05	0.6	2.1	0.285
	1.20	0.6	2.9	0.206
Sno_2	0.05	0.6	4.1	0.146
	1.20	0.6	4.8	0.125

V. CONCLUSION

From the resistance values obtained from the graphs, we observe that GAAFET with SnO2 as gate oxide material has less resistance and more current through which we can say that the performance of the GAAFET is more efficient when compared to the other gate oxide materials we've used.

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