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Harmonic Reduction using Three-Phase IGBT Based Detuned Filter in Grid connected PV System

K.Bharathi, M.Sasikumar

Abstract*: As the energy consumption is steeply increasing globally, alternate methods must be adopted to meet the demands. Also to preserve the conventional resources, energy production by renewable sources such as solar, wind, geothermal, tidal, etc is the need of the hour. Energy generation through solar cells can be largely used. But, the harmonic content in the power generated from the solar panels are seemingly higher than the maximum allowable limits. Harmonics are the deviation in the output value from the actual value, caused due to various phenomenal factors. We have observed that the harmonics in the output power from the photo-voltaic cells is way to larger than the limited value. So, we have proposed a three-phase shunt connected IGBT based detuned filtering system to limit the harmonic levels within the desired values. To reduce the current THD value below the permissible limits as specified by the IEEE standards and also to maintain voltage regulation and power factor correction, as well as to improve the efficiency of the entire system.

***Keywords* : Detuned filter, Harmonics, Total Harmonic Distortion (THD).**

I. INTRODUCTION

We have observed that the system efficiency is greatly influenced by harmonics in output voltage and current.
The maximum allowable limits according to the IEEE 519 standards is as mentioned below:

- Current harmonics is 8%.
- Voltage harmonics is 5%.

Though both voltage and current harmonics are present in the system, the current harmonic levels have greater influence.

SOURCES OF HARMONICS:

- Transformer under saturated conditions
- Computer power supplies
- UPS, Switched Mode Power Supply (SMPS)
- Adjustable speed drives
- Electric Arc Furnace, Induction Furnace
- Resistance welding machines
- Arc discharge device
- DC drives, variable frequency drives and DC rectifiers

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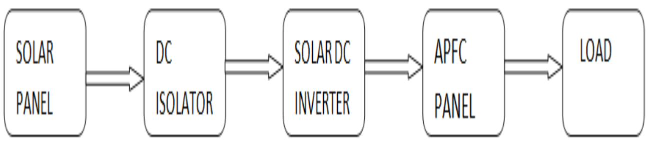
SOLUTION TO REDUCE HARMONICS

Current and Voltage output waveforms having more distortions can create undesirable effects in the power system to those electrical networks to which these systems been connected. Because of harmonic filtering so many advantages are there in power system .Reactive power control voltage flicker reduction are main advantages. For power factor correction and for proper voltage regulation, capacitor banks are necessary. But, the addition of capacitor bank increases the harmonic level in the system beyond the specified limit. Since, we cannot omit the capacitor banks in the circuit we must find alternative measures to reduce the harmonics. This can be done by connecting a filtering system to the existing system. A harmonic filter system basically injects required kVAr to the network to improve the power factor below the harmonic frequency and beyond the harmonic frequency

II. EXISTING SYSTEM

We have observed that the system without a filter has a major drawback. The harmonic content in the output power is deliberately high, due to which the total transmitting power gets reduced. Also, the efficiency of the entire system is considerably reduced, which implies that the losses in the system are significantly high. Though the system has an inbuilt filter in it, it is not significantly effective. Thus, we aimed at lowering the harmonic content with the help of a specially designed filter explicitly to reduce it to the allowable limits. In the existing system, we have only a combination of blocking reactors with a delta connected capacitor network. But, this system does not reduce the harmonic content properly. As a result, the harmonic levels are above the permissible limits. This leads to more power dissipation in the device. Thus, it gets hotter and the efficiency is reduced drastically. Also, the TNEB considers the 5th harmonic as a major concern and imposes penalty. A detuned filter is observed to reduce fifth order harmonics to a better extent.

III. BLOCK DIAGRAM OF CONVENTIONAL SYSTEM



OBSERVATIONS

The Total Harmonic Distortion (THD) of voltage harmonics is **2.74%** which is within the limits as specified by IEEE 519 standards.

The Total Harmonic Distortion (THD) of current harmonics is **20.85%** and reaching a maximum of **28.25%** which is outside the limits as specified by IEEE 519 standards. We can conclude that there are harmonic amplifications when the capacitor is switched on. Consequently, there is increase in both current and voltage THDs. Because of these harmonic currents flowing into the capacitors, there is degrading of the capacitor banks.

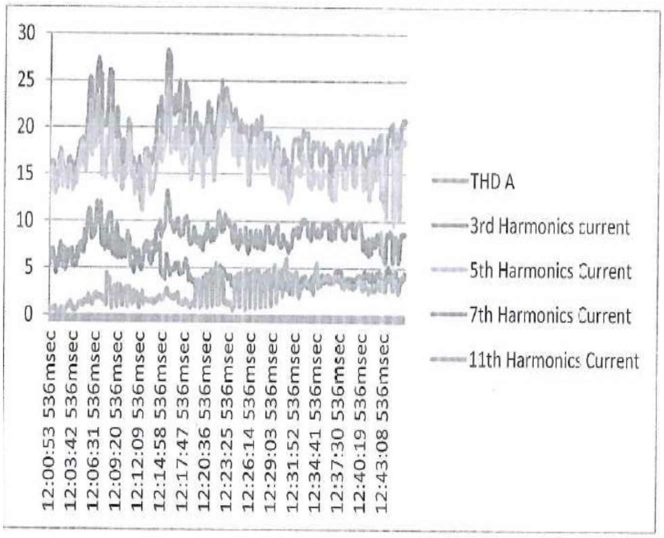
INTRODUCTION TO APFC

APFC or Automatic Power Factor Correction panels are used for power factor improvement. Power factor is a key factor in measuring electrical consumptions. Everyone knows electricity has become costlier now days. Therefore it becomes utmost important to reduce the electrical consumption for reducing expenditure.

PARAMETER READINGS UNDER NORMAL LOAD WITH APFC SWITCH ON CONDITION

Parameter	Values	R	Y	B	Units
Vrms	Max	415	415	415	Volts
Irms	Max	398	396	412	Amps
F	Max	50			Hz
PF disp	Max	0.96	0.99	0.99	
Vthd	Max	2.74	2.44	2.52	%
Ithd	Max	28.18	28.25	25.97	%
I Harmonic Spectrum	2nd	3.59	3.62	2.78	%
	3rd	12.01	6.35	4.38	%
	5th	24.37	24.03	22.18	%
	7th	10.83	13.13	12.17	%
	11th	6.00	5.38	3.59	%

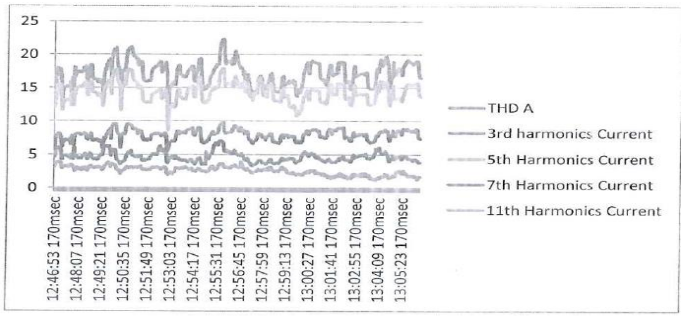
The below graph shows the current harmonics with capacitor ON condition



PARAMETER READINGS WITH NORMAL LOAD WITH APFC SWITCH OFF CONDITION

Parameter	Values	R	Y	B	Units
Vrms	Max	418	418	416	Volts
Irms	Max	416	412	416	Amps
F	Max	50			Hz
PF disp	Max	0.94	0.95	0.96	
Vthd	Max	2.52	2.65	2.83	%
Ithd	Max	20.85	22.29	21.27	%
I Harmonic Spectrum	2nd	2.98	3.56	3.53	%
	3rd	7.44	7.00	4.73	%
	5th	17.88	18.47	17.84	%
	7th	8.32	9.75	9.74	%
	11th	3.97	2.02	2.21	%

The below graph shows the current harmonics with capacitor OFF condition



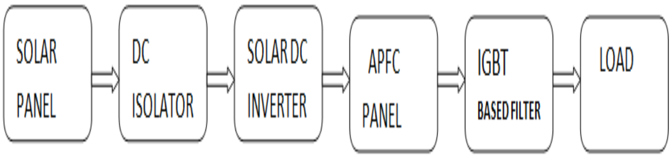
READINGS WITH TOTAL LOAD WITHOUT FILTER

Time	Current Avg	Power Factor Total Avg	THD A	3rd Harmonics current	5th harmonics current	7th harmonics current	11th harmonics current
12:15:29 536msec	215	0.96	26.01	4.84	22.08	11.41	2.24
12:15:30 536msec	211	0.96	26.6	4.89	22.61	11.71	2.26
12:15:31 536msec	211	0.96	26.76	4.96	23.07	11.86	2.29
12:15:32 536msec	225	0.95	26.17	4.91	22.9	11.85	2.3
12:15:33 536msec	206	0.95	25.53	5.01	22.4	11.66	2.32
12:15:34 536msec	220	0.94	26.05	5.23	22.7	11.82	2.35
12:15:35 536msec	208	0.94	26.12	5.53	22.5	11.94	2.4
12:15:36 536msec	208	0.95	27.24	6.24	23.31	12.52	2.56
12:15:37 536msec	200	0.96	27.96	6.42	24.21	12.9	2.66
12:15:38 536msec	207	0.96	28.08	6.4	24.2	12.96	2.68
12:15:39 536msec	205	0.95	28.13	6.35	24.07	12.91	2.73
12:15:40 536msec	198	0.95	27.81	6.07	23.85	12.81	2.79
12:15:41 536msec	195	0.96	28.09	6.02	24.16	12.92	2.83
12:15:42 536msec	195	0.96	28.25	6.03	24.37	13.04	1.38
12:15:43 536msec	243	0.89	19.23	6.01	16.04	8.35	1.41
12:15:44 536msec	253	0.86	18.74	5.82	15.52	8.25	1.55
12:15:45 536msec	253	0.86	18.47	5.61	15.18	8.27	1.65
12:15:46 536msec	245	0.88	18.44	5.44	15.14	8.34	1.73
12:15:47 536msec	239	0.89	18.84	5.42	15.52	8.49	1.73
12:15:48 536msec	251	0.87	18.79	5.36	15.47	8.34	1.69
12:15:49 536msec	253	0.86	18.42	5.26	15.11	8.28	1.66
12:15:50 536msec	250	0.86	18.23	5.17	14.96	8.34	1.72
12:15:51 536msec	243	0.88	18.43	5.16	15.2	8.4	1.75
12:15:52 536msec	236	0.89	18.73	5.14	15.55	8.37	1.66
12:15:53 536msec	236	0.87	18.96	5.21	15.87	8.45	1.65

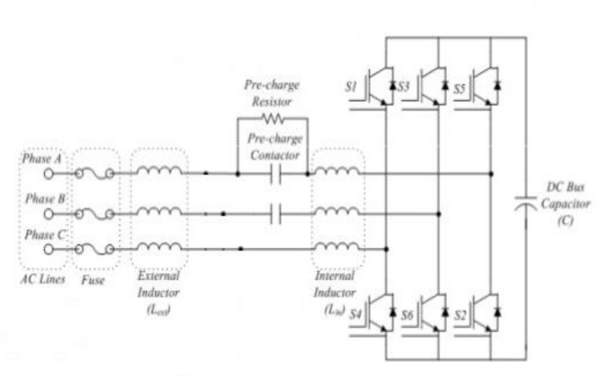
IV. PROPOSED SYSTEM

We have formulated a filtering system constructed using IGBT (Insulated Gate Bipolar Transistor) semiconductor device. This filter is connected in shunt with the load such that it consumes minimal current possible, so that the transmission losses are also negligible. Also, IGBT modules have high voltage and current handling capability which serves as the main purpose to be used in high voltage applications. The existing 300kVAr APFC (Automatic Power Factor Control) panels should be adopted with 14% detuned filter and rating of capacitors of 525V, so as to avoid resonance in the presence of AHF (Active Harmonic Filter). A 100A AHF should be connected at the incomer to care of mitigation of harmonics and to bring it to the recommended levels. Since the LT side voltage is in the range of 400-415V, we adopt a capacitor with a higher voltage rating of 525V, to protect the system in case of voltage surges. Before the adoption of filter the total current distortion was around 22%. So we use a 14% detuned filter to bring the total current distortion value to the standard limit of 8%. The power factor is also observed to increase to unity power factor.

BLOCK DIAGRAM OF PROPOSED SYSTEM



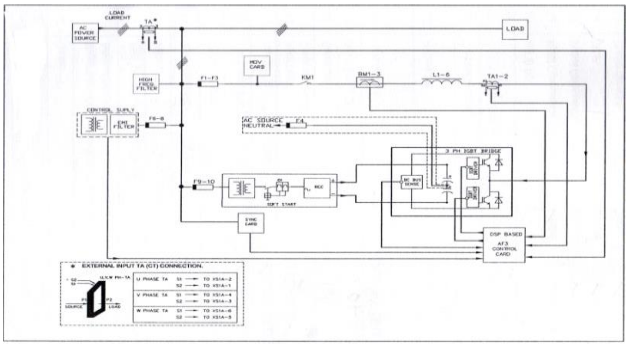
CIRCUIT DIAGRAM OF PROPOSED SYSTEM



READINGS WITH TOTAL LOAD WITH FILTER

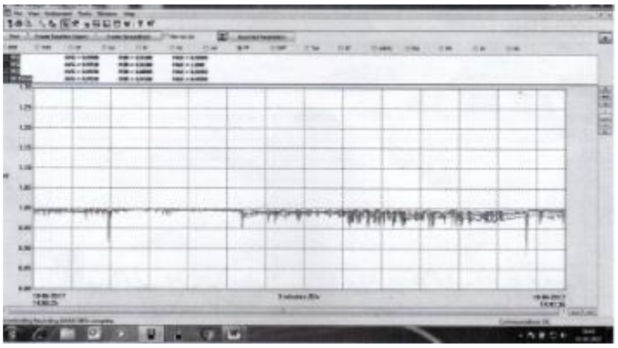
Time	Current Avg	Power Factor Total Avg	THD A	3rd Harmonics current	5th harmonics current	7th harmonics current	11th harmonics current
13:26:16 482msec	220	0.95	15.01	2.84	19.08	5.41	1.24
13:26:17 482msec	208	0.96	15.6	2.89	19.61	5.71	1.26
13:26:18 482msec	208	0.96	15.76	2.96	19.07	5.86	1.29
13:26:19 482msec	200	0.96	18.17	2.91	20.9	5.85	1.3
13:26:20 482msec	207	0.95	18.53	2.01	20.4	5.66	1.32
13:26:21 482msec	205	0.94	19.05	3.23	20.7	5.82	1.35
13:26:22 482msec	198	0.93	19.12	3.53	18.5	5.94	1.4
13:26:23 482msec	195	0.95	16.24	3.24	18.31	6.52	1.56
13:26:24 482msec	195	0.96	17.08	3.42	19.21	6.9	1.66
13:26:25 482msec	243	0.96	17.13	3.4	19.2	6.96	1.68
13:26:26 482msec	253	0.96	16.81	3.35	17.07	6.91	1.73
13:26:27 482msec	253	0.95	18.09	3.07	17.85	6.81	1.79
13:26:28 482msec	245	0.95	18.25	3.02	18.16	6.92	1.83
13:26:29 482msec	239	0.96	19.23	4.03	20.37	7.04	1.8
13:26:30 482msec	251	0.89	18.76	4.01	19.04	3.35	1.41
13:26:31 482msec	253	0.90	18.45	4.82	18.52	3.25	1.55
13:26:32 482msec	250	0.89	17.44	4.61	18.18	3.27	0.65
13:26:33 482msec	243	0.88	17.84	4.44	18.14	3.34	0.73
13:26:34 482msec	236	0.87	17.79	4.42	17.52	3.49	0.73
13:26:35 482msec	236	0.87	17.42	3.36	18.47	3.34	0.69
13:26:36 482msec	237	0.86	17.23	3.26	18.11	3.38	0.66
13:26:37 482msec	249	0.89	18.43	3.17	17.96	3.34	0.72
13:26:38 482msec	225	0.88	17.63	3.16	18.2	3.4	0.75
13:26:39 482msec	231	0.89	17.03	3.14	19.55	3.37	0.66
13:26:40 482msec	223	0.89	17.98	3.21	19.87	1.45	0.65

SIMULATION USING POWER ANALYSER

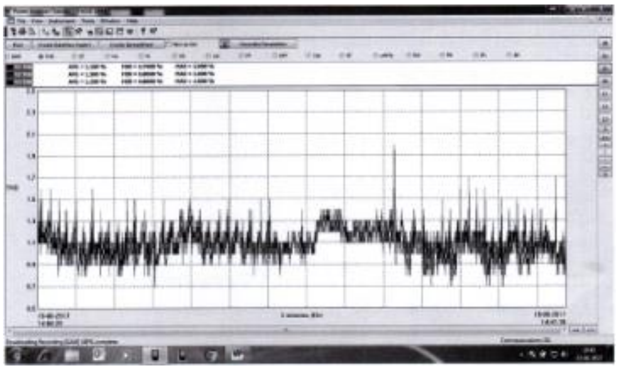


KVA

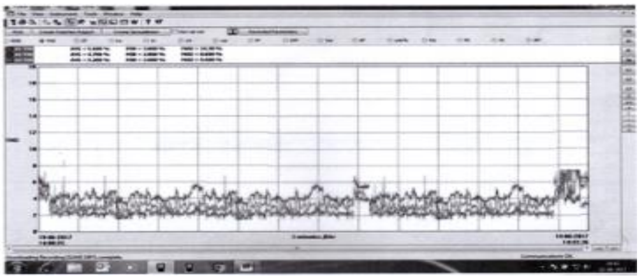
POWER FACTOR

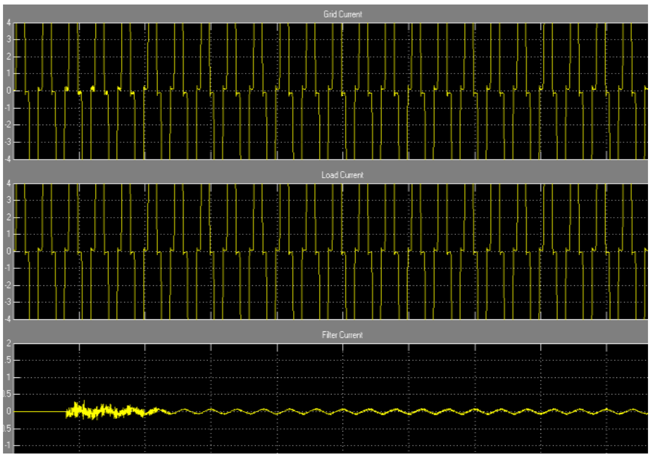


VOLTAGE THD

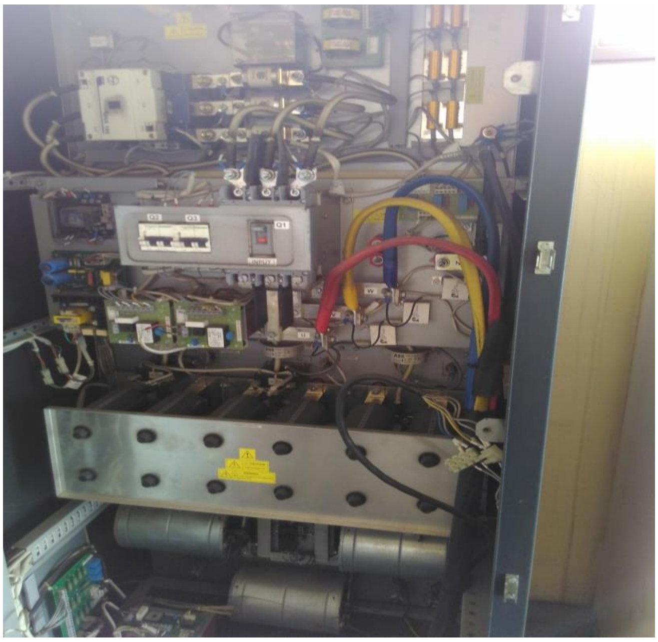


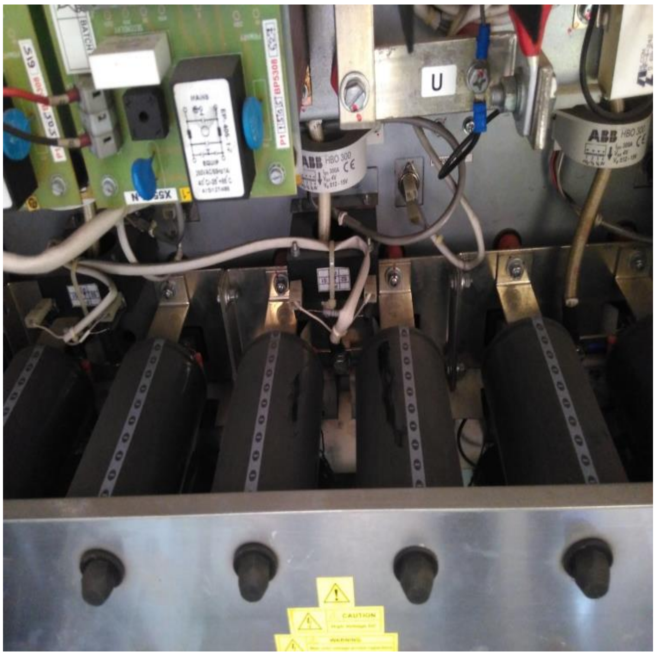
CURRENT THD





V. HARDWARE LAYOUT





HARDWARE COMPONENTS

- IGBT module
- DC capacitors
- Heat sink cooling fans
- Power resistor
- Semiconductor fuse
- Choke cooling fan
- Control card
- Display interface card
- Interface card

VI. RESULT AND DISCUSSION

The implementation of the proposed three-phase IGBT based shunt connected detuned filtering system have considerably reduced the harmonic levels to the permissible limits. Also, the voltage regulation and power factor correction is maintained, with reduced transmission losses.

The overall efficiency of the system is improved.

VII. CONCLUSION

The implementation of the proposed three-phase IGBT based shunt connected detuned filtering system have considerably reduced the harmonic levels to the permissible limits.

Also, the voltage regulation and power factor correction is maintained, with reduced transmission losses.

The overall efficiency of the system is improved.

The odd harmonics are reduced using the simulated filter. Since solar power generation is being adopted by various industries on a large scale, the reduction of harmonics in its output power will be a major concern in upcoming years. Also, it reduces the loss in the system and conserves the overall power.

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K.Bharathi, has received the Bachelor degree in Electrical and Electronics Engineering from Bharath Institute of Science and Technology, Madras University, India in 2002, and the M.E degree in High Voltage Engineering from CEG Campus, Anna University, in 2007. Currently she is pursuing her Ph.d degree in Sathyabama University, Chennai and working as a Assistant Professor in Jeppiaar Engineering College, Chennai, Tamilnadu, India.