International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-9 Issue-1, May 2020

Design and Implementation of Jtag Compatible 4-Bit Multiplier

A.Indira, B.Sumathi, S.Vigneshwari, A.Saravanaselvan

Abstract: ***The novel scan- based methodology was developed and resulted in system designers agreeing on it due to the rising complication of boards and also enhancement of technologies like multichip modules. It is called as boundary scan testing for the board level chips. This method was established by the Joint Test Access Group. It was named as JTAG. JTAG was developed for verifying designs and testing printed circuit boards after manufacture. A JTAG interface is a special interface added to a chip. Traditional test technologies require very large and expensive equipment. The most aim of this paper is to style and implement 4-bit multiplier using this standard. The designs were being verified and the circuit boards were being tested after the manufacture by using the industry standard JTAG. It is employed because of accessing sub-blocks of chips. It's a very important mechanism for debugging embedded systems. Boundary-scan cells created exploitation electronic device and latch circuits square measure hooked up to each pin on the device. These cells, embedded among the device, will capture knowledge from pin or core logic signals conjointly as force knowledge onto pins. Captured knowledge is serially shifted out through the JTAG take a look at Access Port (TAP) and will be compared to expected values to figure out a pass or fail result. Forced take a look at knowledge is serially shifted into the boundary-scan cells.***

Keywords : boundary scan testing, JTAG, JTAG interface, 4 bit multiplier

I. INTRODUCTION

The Institute Of Electrical and Electronic Engineers defined Joint Test Action Group as IEEE 1149.1.It is also referred to as boundary scan architecture and it's the integrated method wont to check the connectivity between the integrated circuits placed on the computer circuit Board.Nowadays PCB's are grown far more complex where the standard test methods like testing with probes are impossible. Physical access to the nodes are complex due to the space constraints. it'll not yield accurate results.Thus JTAG is evolved in 1990 which has become more popular and is adopted by all as it is easy to detect faults and the results were also accurate. JTAG also helps to obtain Design For Testability as the designs are made suitable for testing. The main advantage of JTAG is that the boundary scan cells can be accessed in two modes , that is normal mode and functional mode. In normal mode, the device can perform its own function and in test mode , it is allowed to test the connectivity in the device.

II. LITERATURE SURVEY

Distributed Reconfigurable Hardware Systems can be tested in two steps by proposing a brand new extension of the IEEE Std. 1149.1 . the primary step introduces associate degree extension of the boundary scan design by ever-changing the same old boundary scan register (BSR) into a reconfigurable BSR. The second extends the JTAG key directions that cowl reconfigurable internal check and reconfigurable external check. For a coherent testing of various subsystems, a world DRHS check formula is planned. the fundamental plan behind coherent testing is to alter testing of dependent circuits and their interconnections per the coordination and interconnection matrices. Finally, so as parenthetically the effectiveness of the planned formula, we've conducted experiments on combinable and asynchronous ordered DRHS [1]1. JTAG is primarily used for IC producing check, however conjointly for in-field debugging and failure analysis since it provides access to internal subsystems of the IC. as a result of the JTAG has to be left intact and operational when fabrication, it inevitably provides a "backdoor" that may be exploited outside its supposed use. For these problems ,there is machine learning-based approaches to discover illegitimate use of the JTAG [2]2. There is a unique protection method for fine-grained access management in complex reconfigurable scan networks supported a challenge-response authentication protocol. The target scan network is extended with along with the instrument and secure segment insertion bits that together control the accessibility of individual instruments . Usually the primary fine-grained access management scheme that scales well with the amount of protected instruments and offers a high level of security. In comparison to the recent state-of-the-art techniques, this scheme is more favorable with regard to implementation cost, performance overhead, and provided security level [3]3. Chip function is not necessary for board test(shorted/open nets). Test generation is fully automated; Simple 'In-Circuit Library' models(BSDL) are vendor-supplied or EDA-generated [4]4.

Manuscript received on April 02, 2020.
Revised Manuscript received on April 21, 2020.
Manuscript published on May 30, 2020.
* Correspondence Author
A.Indria*, in ECE department,National Engineering College ,kovilpatti, thoothukudi, Tamilnadu ,India Email: indirarumugam99@gmail.com
B.Sumathi in ECE department,National Engineering College ,kovilpatti, thoothukudi, Tamilnadu ,India Email: bsumathi1998@gmail.com
S.Vigneshwari in ECE department,National Engineering College ,kovilpatti, thoothukudi, Tamilnadu ,India Email:vickysundar26@gmail.com
A.Saravanaselven department,National Engineering College ,kovilpatti, thoothukudi, Tamilnadu ,India Email: asselvan1981@gmail.com

Each and every electronic test problem are most apparent at the level of IC. Any electronic circuit testing requires test signals that propagate the circuit and effects due to these signals are monitored. When circuits collected from discrete components and low-complexity standard IC. This presented some serious problems because the inner workings of the circuit are ready to access [5]5.

III. PROBLEM DESCRIPTION

- BGA packaging is a technique that is used for increasing number of devices. Each BGA devices on a board have extreme limitations on testing process which includes, bed of nails and flying probe machines.
- The cost of building NRE test fixtures are often considered as excessively high.
- Each processor can interact via the peripherals with other processor in different ways. These traditional function test requires costly custom development for every board..
- Large and costly equipments are used for these conventional test technologies.

IV. METHODOLOGY

A. JTAG Architecture

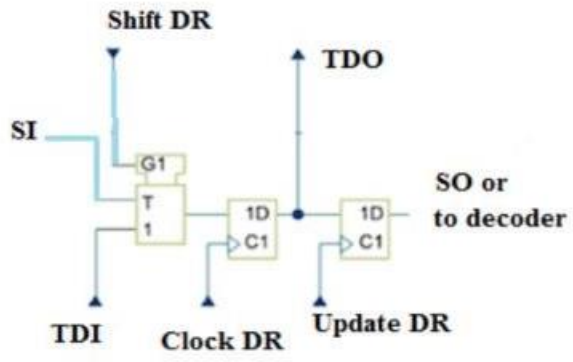
The JTAG architecture is developed in the way to test interconnections without using physical test probes on a chips arranged in a printed circuit board. Boundary-scan cells were created by flip flop circuits and multiplexers. These scan cells were inserted in the device and connected to the boundary of the each and every pin. These cells, will capture data from input pin or core logic, further force data onto output pins for testing. These test data input are shifted into the scan cells serially. These captured data will be named as test data input (TDI) .The test data input is serially shifted out through the JTAG Test Access Port (TAP) controller and should be compared with the data from the output pins to check whether it is a pass or fail result. The above process would be controlled by the scan path or scan chain from serial information path. JTAG required only tens or many test vectors to perform the task instead of thousands vectors. Lower capital equipment cost, higher test coverage, shorter test times and increased diagnostic capability will be permitted by boundary –scan.

B. JTAG TAP Controller

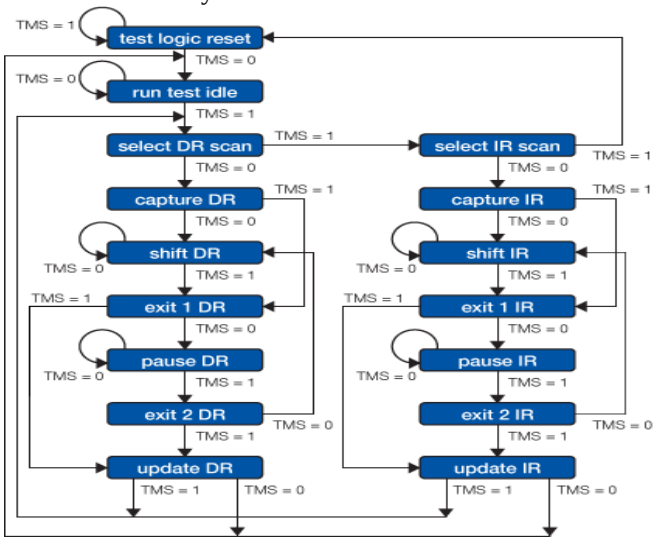
TAP controller could be a finite state machine. The state of the TAP controller will vary according to the TMS and TCK signals of the faucet controller and it controls the operations that should be performed by the circuit. It'll also control the scanning of information into registers of the JTAG architecture. For scanning the TDI signal, there are 2 transition paths at input pin, one for shifting to the instruction register and one for shifting into data register. The state diagram is shown in figure below. At the rising fringe of clock-TCK all state transitions of the faucet controller will happen with the support of TMS. Actions of the test logic will occur either in the rising TCK or within the falling fringe of TCK in each state.

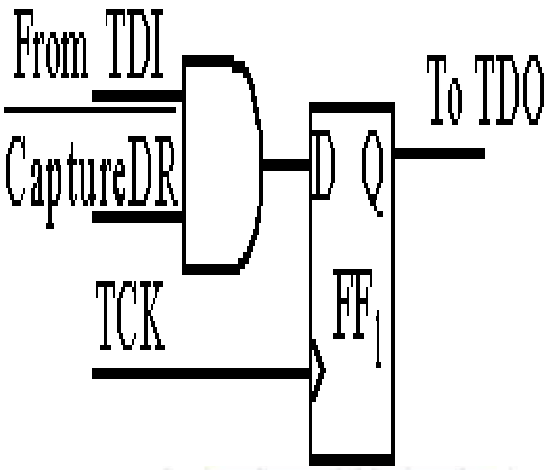
Starting state at power-up is Test-Logic-Reset .It stays here as long as TMS is high (CUT normal mode).Note that it may be reached from any other state by holding TMS high and clocking at least 5 times. With TMS at zero, Run-Test-Idle is active on ensuing TCK. Here BIST may be initiated or the TAP idles between scan operations. To begin testing, the instruction needs to be loaded into IR. TMS command high and TCK clocked (Select-IR-Scan).This connects TDI and TDO to Instruction Register.With TMS at zero,Capture-IR state becomes active and then Shift-IR, that permits the instruction to be scanned in, to the IR.Two clocks with TMS at one causes instruction transfer to output latches.

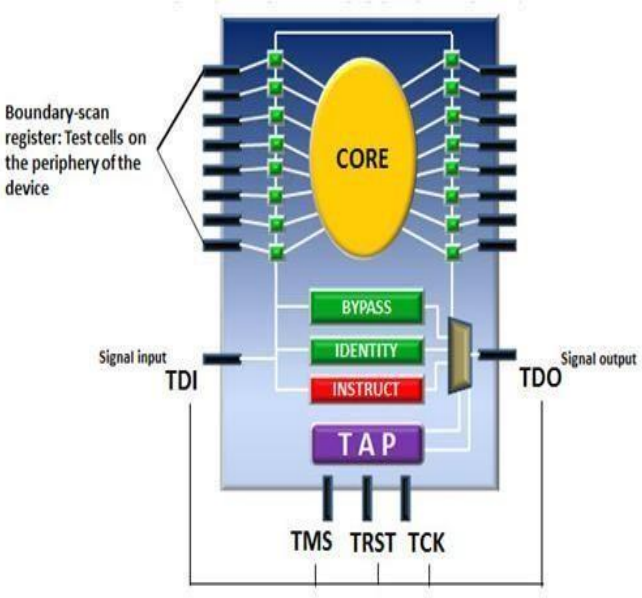
B. Boundary Scan Chain



.Boundary scan chain consists of boundary scan cells connected serially to every other. The information is captured and shifted to test the results externally via TDO and therefore the TDI is serially shifted into the scan cells which are connected to the boundary of each pin on the device. This operation is controlled by scan path or scan chain. because it can directly accessed to any or all the nodes , the test vectors required is additionally less compared to other non – JTAG compatible devices. By this, the test time is additionally reduced. Using this boundary scan chain, the fault is additionally identified with more accuracy.







D. JTAG Registers

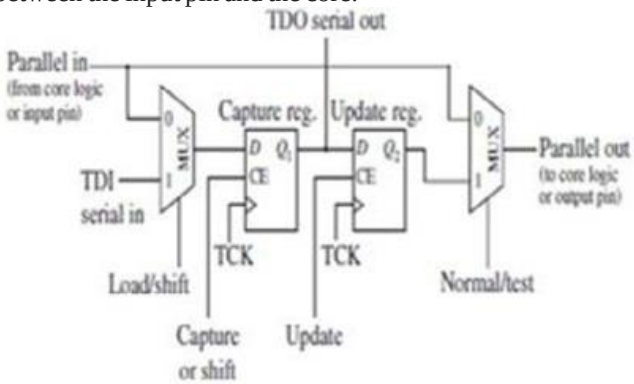
JTAG registers has two types of registers namely data registers and instruction registers.

a. Data Registers

There are 3 data registers. They're boundary Scan Register , bypass register and ID code or identity register.

1. Boundary Scan Register

Boundary scan cells are positioned in the input side and output side of the chip. In the input side , the cells are placed between the input pin and the core.



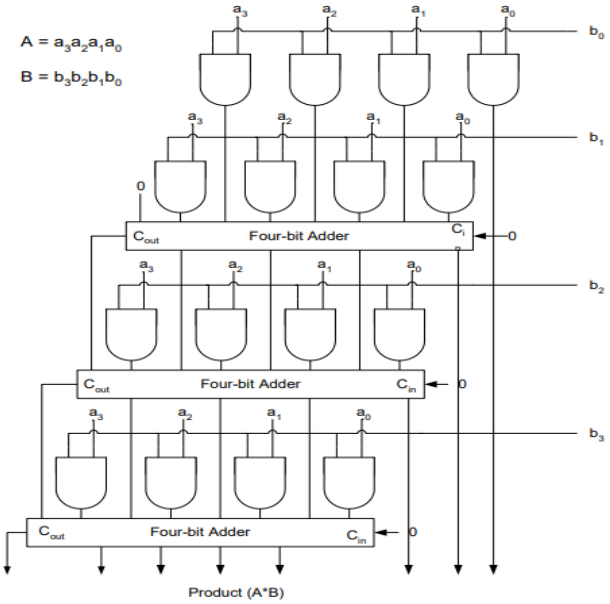
In the output side , the cells are placed between the output and the core functional pin. In normal mode , the cells just pass the data into and out of the core. In test mode , it can pass the data serially via TDI to TD0. They are used to check the pin to pad connectivity and identify where the fault occurs.

2. Bypass Register

Bypass instruction is exclusively there to bypass the boundary scan chain and it allows the data to pass through this register. By using this instruction , specific device can be allowed to be tested without passing through other boundary scan register. This reduces the test time effectively and also specific device can be tested.

3. Identity Register

ID code register contains the ID code and revision



number for the device. This ID code and revision number permits the device to joined to its Boundary Scan Description Language (BSDL) file. The file contains information of the full description of the Boundary Scan functionality configuration for the device.

b. Instruction Register

This register holds the current instruction. Using this instruction , tap controller decides whether the data should be passed through bypass register or the boundary scan register. The size of this register is 2 bit long. There are some basic instructions.

i. BYPASS

The data is captured, shifted and updated through the bypass register. During this operation, the device will be allowed to perform its function without any interpretation.

ii. SAMPLE

During this instruction, taking a sample of the data entering through its inputs i.e. capture the data through the boundary scan register and leaving the chip through its outputs i.e. shift data through the boundary scan register. In the update phase, it doesn't drive data on inputs or outputs.

iii. PRELOAD

In this instruction we can fixing a value within the scan cells for further use by shifting the data through the boundary scan register.

In the capture phase, it doesn't get the previous value into the cell and thus the update phase doesn't drive data against inputs or outputs.

iv. EXTEST

It is used to test the connectivity between the multiple chips. It is used to identify the short or open between the chips. The short between the two pins acts as wired AND and open in the pin acts as stuct at 1 fault.

v. INTEST

It is used to check the connectivity within the core logic. During this test, TDI and TD0 lines are connected to the boundary scan cell, so that the functionality of the core can be tested

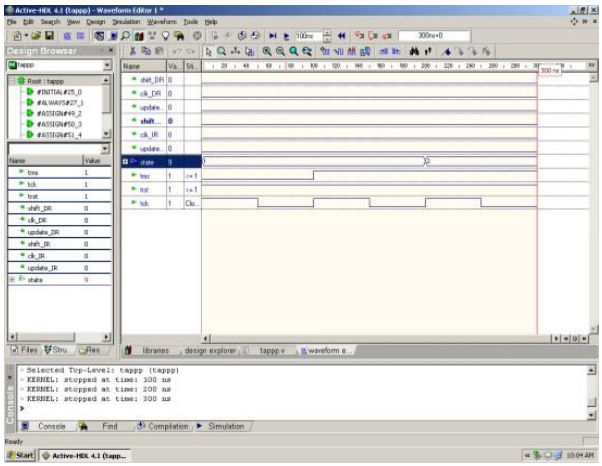
E. JTAG Compatible 4 Bit Multiplier

a. 4 Bit Multiplier

Array multiplier is popular thanks to its structure. Multiplier circuit is depends on add and shift algorithms. Every partial product value is formed by the multiplication of the multiplicand with one multiplier bit. The partial product are kept shifted with their bit orders and so added.The process of addition is distributed with carry propagate adder. If N is the multiplier length, then N-1 adders are needed.In this, the partial products can be produced using AND gates and the Full Adders and Half Adders perfomed the aggregation of partial products. In an M x M array multiplier, the partial products may be computed by M x M of AND gates and also the M x (M-2) full adders and M half adders may be produced the addition of partial products. The speed performance will be degraded for wide fan-in multipliers due to the worst case delay of the bit array multiplier is proportional to the width of the multiplier. Since the 4-bit array multiplier uses a pipelined architecture, it is simple to design.

V. RESULTS

With reference to the JTAG architecture, the core logic 4 bit multiplier has been implemented. The output of the core logic is given below.



VI. CONCLUSION

Usually for testing an IC we use ATE which test the IC with the help of test head,prober / handler and DIB . As technology is being developed , the size of the IC is extremely small. Hence the testing has become more complex nowdays . To reduce the complexity we are using JTAG to achieve the DFT (Design For Testability). To attain DFT 5 JTAG pins are required. They are TDI,TDO,TMS,TRST,TCLK. Using TAP controller, Boundary Scan Cell, Instruction Register, Bypass Register, the pins are enabled. In our paper, the logic blocks of JTAG compatible 4-bit multiplier are verified using Active HDL.

REFERENCES

1 Ahmed, A. B., Mosbahi, O., Khalgui, M., & Li, Z. (2019). Boundary Scan Extension for Testing Distributed Reconfigurable Hardware Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 66(7), 2699-2708..

2 Baranowski, R., Kochte, M. A., & Wunderlich, H. J. (2015). Fine-grained access management in reconfigurable scan networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 34(6), 937-946.

3 Maunder, C. (1986). JTAG, the joint test action group. In IEE Colloquium on New Ideas in Testing (p. 6).

4 Dettmer, R. (1989). JTAG-setting the standard for boundary-scan testing. IEE Review, 35(2), 49-52..

5 Peterka, P., & Medvinsky, A. (2012). U.S. Patent No. 8,214,630. Washington, DC: U.S. Patent and Trademark Office.

6 Khu, A. H., Shokouhi, F., & Theron, C. A. (2006). U.S. Patent No. 7,047,467. Washington, DC: U.S. Patent and Trademark Office.

7 Khu, A. H., Shokouhi, F., & Theron, C. A. (2006). *U.S. Patent No. 7,047,467*. Washington, DC: U.S. Patent and Trademark Office.

8 JTAG Interface, DanStorakers , Patent no : US 7,747,916 B2 , Jun. 29, 2010.

9 IEEE Transaction On Computer-Aided Design Of Integrated Circuits And Systems- IC Protection Against JTAG-Based Attacks ,38 & 1 , 2019, XuanleRen,Francisco Pimentel Torres.

AUTHORS PROFILE

A.Indira is an undergraduate student in the stream of Electronics and communication Engineering at National Engineering College, Tamil Nadu, India. Her research interest includes VLSI and JTAG Standard.

B.Sumathi is an undergraduate student in the stream of Electronics and communication Engineering at National Engineering College, Tamil Nadu, India. Her research interest includes VLSI and JTAG Standard.

S.Vigneshwari is an undergraduate student in department of Electronics and communication Engineering at National Engineering College, Tamil Nadu, India. Her research interest includes VLSI and JTAG Standard.

A.Saravanaselvan is an Assistant Professor (SG) in the Department of Electronics and Communication Engineering at National Engineering College, Tamil Nadu, India. He received his B.E. Electronics and Communication Engineering degree from PGP College of Engg & Tech, Periyar University, Salem, Tamil Nadu in the year 2003. He completed her M.E. Applied Electronics from Anna University of Technology, Tirunelveli, Tamil Nadu in 2011. He is currently doing Ph.D. in Anna University, Chennai. He has 14 years of academic experience. He has presented six papers in the international conference . His research interest is about Sensor Network. His is a life member of IE society bodies.