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Design of Broadband 1.9 GHz Ga as MMIC Switching Power Amplifier for PCS Communication Services

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Abstract*: *The paper presents a broadband Monolithic microwave Switching Class–E Power amplifier using 0.5µm GaAs E-pHEMT technology for PCS communications systems operating at 1900MHz.Wider bandwidth is achieved by employing reactance compensation technique in load network of the switching power amplifier. The main Power amplifier is a single stage Class-E circuit with a driver stage driving it to achieve high gain and efficiency. The modified load network using reactance compensation network results in higher power added efficiency. The paper provides simulation results of designed two-stage Class-E Power amplifier circuit results with an power output of 20dBm, power added efficiency of 80% and gain of 26dB at the centre frequency of 1.9GHz compared with various Class-E designs of 1.9 GHz using different technologies. A high linear gain is reported in the design at the frequency range of 0.8GHz to 2.2GHz.The designed circuit achieves a wider bandwidth of 1.35GHz over a frequency range of 0.8-2.2GHz.The physical layout is drawn using GaAs foundry components and EM simulation is performed.

Keywords* : *Input Intercept point, Linearizer, Output at 1dB compression point, pHEMT, Power-added Efficiency (PAE).

I. INTRODUCTION

A higher demand for spectral efficiency in wireless communication makes various schemes of modulation such as QAM, QPSK to be more attractive. But there is always a trade-off between spectral and power efficiency in all digital modulation schemes. As the signal bandwidth is more limited, due to filtering or pulse shaping, Spectral regrowth can be prevented through linear power amplifiers. Spectral regrowth affects the transmitted bandwidth and distortion in the desired signal within the bandwidth. A high-efficiency class E power amplifier was first proposed by Sokal et al. Design equations for a wideband PA using broadband matching network was discussed in [1].A new circuit topology of power amplifier having a modified load network with a series-parallel resonant circuit as a compensation of shunt capacitor was introduced in [2]. A class E amplifier was designed in [3]using GaN HEMT to operate in L band at the frequency of 900 MHz- 1500 MHz and obtained with 1W output power and Power added efficiency of 81%. Microwave integrated circuit (MMIC) technology for frequency between1.8GHz to 3.5GHz.Reactance compensation technique is introduced which achieves wide bandwidth and high efficiency with an LDMOS transistor technology for 136-174 MHz FM radio applications [4]. The paper[5] discussed a stacked FET configuration using 0.18µm CMOS technology power amplifier which results with an efficiency of 38%.The author in [6],implemented the power amplifier at 1.9GHz with a higher output power of 38 dBm. Another implementation of Power amplifier using 0.35µm GaAs pHEMT technology which resulted in 70% PAE[7]. A Two-stage fully integrated, high efficiency and wide bandwidth using 0.5µm E/D pHEMT process for 1.5GHz to 3.8GHz was demonstrated in [8]. Grebennikov [9] implemented Two-stage class E power amplifiers using a BiCMOS process at 5-6 GHz. A higher power output of 19.7 dBm and 43.6% PAE is observed. An efficient load network for an MMIC class E amplifier operating at 22-25 GHz range results in power added efficiency of 42% , highest in Ka-band reported till today [10].Class-E PAs with balun integrated for matching is discussed by Riccardo Brama[11] et al. designed a Lumped element low loss balun and integrated balun with differential cascade topology. A four-stage class-E power amplifier of 1W operating at 935 MHz with a novel technique of resonance power-combining is studied in the paper [12] by Adam L. Martin and Amir Mortazawi. The authors in [13] presented the design and fabrication of Inverse switching power amplifier with drain efficiency of 65% at 2.26 GHz, and 20.4 dBm of output power is observed. Chi-Tsan proposed a concept of switching mode power amplifiers used in RF transceivers with an efficient load network design in which the amplitude and phase distortions are reduced for WCDMA/WiMAX systems [14].

II. DESIGN OF CLASS-E AMPLIFIER

In switching configuration, transistor works as a switch. A 180^{o} phase shift exists between the voltage and current output at the active device. The Switch operates between on and off states as result of which drain voltage waveform is obtained using transient response of load network during off state of switch.The load network of a class-E circuit having a high Q provides zero power dissipation at fundamental frequency, and acts as an open circuit at for other harmonic frequencies except fundamental frequency.Figure.1 shows the load circuit of Class- E power amplifier.

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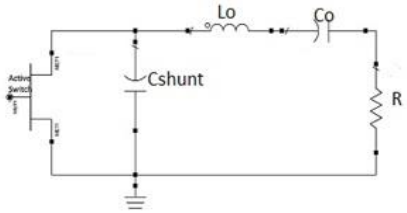

Fig.1.Load network design .of Power amplifier

By using standard design equations for better performance of amplifier, the load network's power output and resistance are obtained through the equations (1-2),

$$P_{out} = V_{dc} * I_{dc} \quad (1)$$

$$R = 1.365 * V_{dd}^{2}/P_{out} \quad (2)$$

The series resonant network is designed with the Q-factor of 2 with duty cycle of 50%. To realize wide band power amplifier, lower Q- value is chosen along with reactance compensation technique.

2.1 Reactance Compensation Technique

An equivalent load network, one with series resonant circuit L_oC_o and shunt resonant circuit L and C with a load resistance R_L is as shown in Fig.2. The reactances of the resonant circuits are tuned to the fundamental frequency. Near the resonant frequency ω, the reactance increases for series and decreases for parallel resonant circuit. By proper selection of shunt circuit components, the change in reactance with frequency is controlled exactly inverse to reactances of the series circuit, there by variation over a wide range of frequency is zero. For a wide operating bandwidth, load angle can be made constant by a suitable choice of Lo and Co component values.

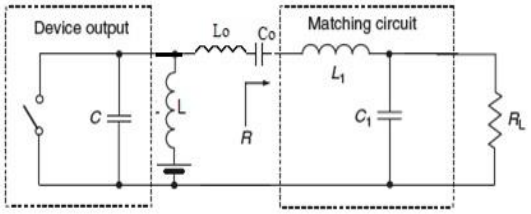

Fig.2. Equivalent circuit of Reactance compensation network

As the load network of the parallel circuit configuration is similar to reactance compensation network, the design equations (3-8) are used to calculate the values.

The input admittance of load network Yin is given by

$$Y_{in} = \left[j\omega C + \frac{1}{j\omega L_0} + \frac{1}{RL + j\omega' L_0} \right] \quad (3)$$

$$\omega' = \omega\left(1 - \omega^2{}_0 / \omega^2\right) \quad (4)$$

where, $\omega_0 = 1/\sqrt{L_0 C_0}$

The shunt inductance L_1 and capacitance C_1 can be obtained by,

$$C_1 = 0.685/\omega * R \quad (5)$$

$$L_1 = 0.732 \times R/\omega \quad (6)$$

The series capacitance Co and Lo are calculated using the following equations,

$$L_0 = \frac{Q \times R}{\omega} \quad (7)$$

$$C_0 = 1/\omega \times R \times Q \quad (8)$$

III. SIMULATED CIRCUIT

The two-stage Class-E PA is designed using 0.5µm (E-pHEMT) process technology. The power amplifier is designed with a drain voltage of 5V and power output of 0.082W.

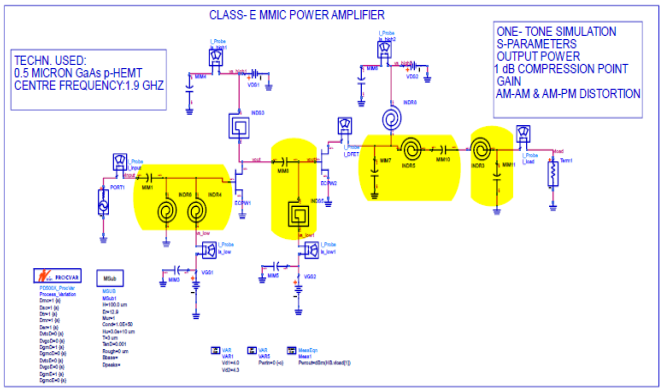

Fig.3. Schematic of Two-stage Class-E Power amplifier

The Fig.3.illustrates the schematic of two-stage class-E power amplifier operated at the centre frequency of 1.9GHz.The simulated Class-E results with the return losses of S(1,1) and S(2,2) as -13.71dB and -20.5 dB respectively. The power added efficiency obtained as 80% with the power output of 22dBm and Linear gain of 26.1dB at an input power of 0dBm as in Fig.4. The linear gain S(2,1) as illustrated in Fig.5 have a wider response from 0.8GHz to 2.4 GHz, with a maximum of 26.1 dB. Input power at 1dB compression point (IP@1dB) of -6dBm and output power (OP@1dB)of 19.9dBm is obtained as shown in Fig.6. The two-tone test performed with carrier frequencies of 1905.42 MHz and 1905.44 MHz which results in IMD3 suppression of 13.75 dBc.

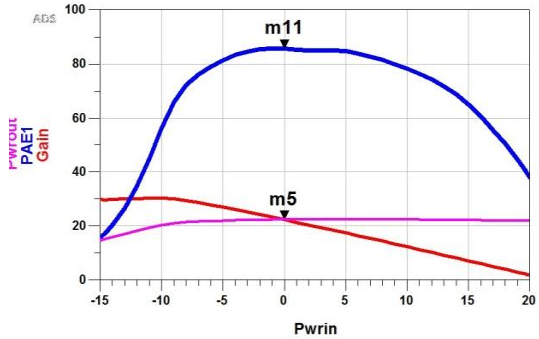

Fig.4. PAE, Gain and Output power plot versus input power

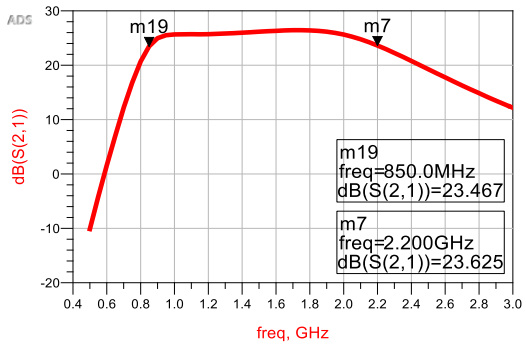

Fig.5. Small Signal gain S(2,1)

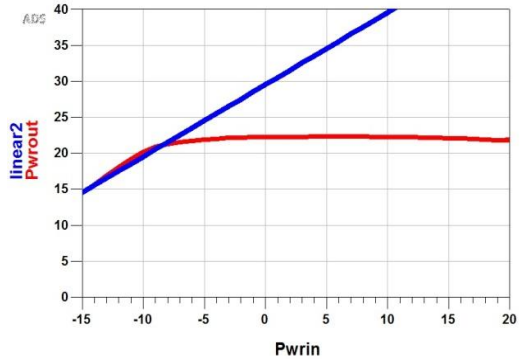

Fig.6. Linear gain and output power versus input power

The physical layout is drawn for the two stage Power amplifier with the WIN foundry components. The layout of the Class-E amplifier is illustrated as in Fig.7, has dimensions of 0.31mm x2.6mm.

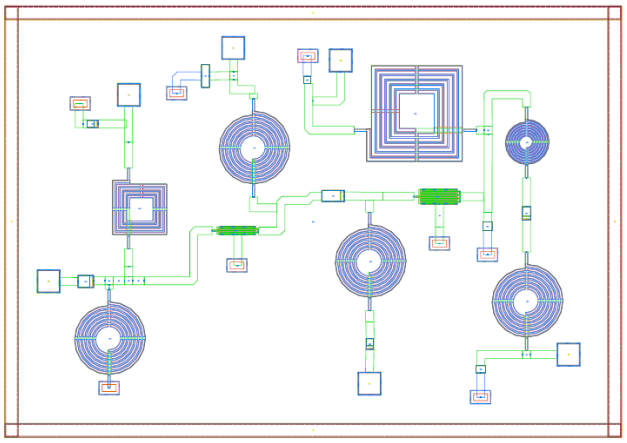

Fig.7. Physical layout of Class-E Power amplifier

Table-I Comparison of performance of Power amplifiers at 1.9GHz

Reference works @ Freq:1.9GHz	*Technology*	*Output power(dBm)*	*PAE (%)*
My work	0.5 µm GaAs pHEMT	22	80
[6]	0.35 µm GaAs pHEMT	27	70
[4]	0.18µm CMOS	23	38
[5]	GaN	38.7	50

The previous works of power amplifiers at 1.9 GHz with different technologies are compared. On comparison, the PAE arrived from this work is higher compared to other designs operating at 1.9GHz. Power added efficiency is improved compared to different designs implemented in various technologies. The bandwidth achieved is wider around 1.5GHz over the frequency range from 850MHz to 2.2GHz for the two-stage PA.

IV. CONCLUSION

A wide band class-E power amplifier is designed using 0.5µm E-pHEMT technology. A wider bandwidth of around 1.5 GHz and higher PAE of 80% is obtained at 1.9GHz. This is achieved by the load network modified using reactance compensation technique which results in wider bandwidth. Wider bandwidth and high efficiency is one of the present day requirements for 5G communications. Linearity by design can be implemented to reduce the intermodulation distortion which has to be addressed in designed PA.

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