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Power Quality Event Detection and Classifier Architecture on FPGA for Smart Meters

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Abstract*: Smart meters have been developed to capture PQ events, detect the event, compress events and characterize events. The events are stored in local memory of smart meter as well are transmitted over communication channel. The smart meter hardware that performs complex signals processing activity such as event detection, classification and compression need to be implemented on reconfigurable platforms. FPGAs are used in smart meters as they support reconfigurability and also has inbuilt memory modules, processor modules and additional features for interfacing. High speed low power area efficient architectures for computation of Dual Tree Complex Wavelet Transform (DTCWT).

***Keywords*: Dual Tree Complex Wavelet Transform, power quality disturbances, Smart meter,**

I. INTRODUCTION

Electric power quality (PQ) has become the concern of utilities, end users, manufacturers, and all other customers. Mainly economic losses occur due to the poor quality of power [1-3]. According to survey, power quality disturbances like voltage dip, interrupts, flickers, transients and other disturbances leads huge economical losses. Smart meters functions include automatic meter reading, outage detection, and information on power grid status to the customer, reducing potential outages, frequency & duration of outages and transmission of information between consumer and the power station unit. The smart meters that are located at various locations along the feeder system acquire information on quality of power at the location and the data logged information at that location is transmitted over power line to the base stations for timely action and monitoring [4].

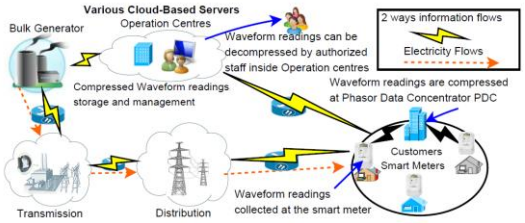

Fig1. Infrastructure of smart grid environment

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Smart Grid and Smart Meter initiatives seek out to enable energy providers and consumers to intelligently manage their energy needs through real-time monitoring, analysis, and control as shown in the fig 1[5]. FPGAs play a vital role in smart meters for data processing, data storage and data transmission. Reconfigurability is one of the major advantages of FPGA with vast hardware resources that can be utilized for implementing complex as well as time critical data processing units. The FPGA permits cost-effective power and monitoring of individual power consumption of every customer. This information from the FPGA can be used to manage the operation of power system. The analysis of Power quality disturbance (PQD) is usually measured by PQ analyzers, but still equipment is cannot be configured to achieve additional analysis of the signal. Smart energy meters, alternatively, can be integrating with several signal processing modules, such as field programmable gate arrays (FPGAs). The development of FPGA-based smart meters that provide a signal analysis intended to detect and quantify PQD from each customer end along with usual energy tariffs calculations [6].

II. PQ EVENT DETECTION AND CLASSIFICATION

PQ data detection is proposed based on DWT wavelet approach and compared with DTCWT transformation techniques [7]. An algorithm for PQ data detection and compression is proposed that uses Dual Tree Complex Wavelet Transform (DTCWT) for sub band computation. DTCWT bands are selected for encoding thus resulting in improvement in compression ratio and that indicate presence of PQ events [8-10]. The developed algorithm for Real Time applications design of suitable hardware architecture for the proposed algorithm will provide applications in smart meters. Figure 2 shows the top level block diagram of PQ feature detector and classifier. PQ signal captured by the data acquisition module is preprocessed prior to feature detection and classification. The preprocessed data is decomposed into multiple levels using DTCWT algorithm. From each of the real and imaginary sub bands the most significant sub bands are selected from which appropriate features are computed denoting the presence of PQ events. The selected features are further processed by the classification network to determine the presence of particular PQ event.

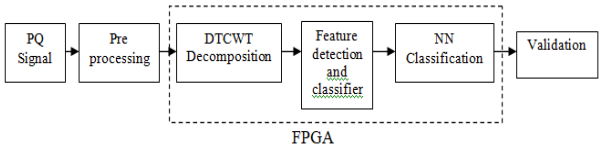

Fig 2. Top level block diagram of PQ feature detector and classifier.

With FPGA platform for smart meter design it is required to design feature detection and classification algorithm in accordance to the resources available on FPGA. Most of the FPGAs from Xilinx as well as Altera consist of LUTs forming the core of FPGA architectures. In addition to LUTs FPGAs comprises of multiplexers as basic elements, multipliers and memory modules as dedicated resources. DTCWT and FFNN are data processing modules and hence require multipliers, adders and memory elements for architecture design. Estimating the computation complexity of DTCWT and FFNN in terms of data path arithmetic units and propagation delay will lead to efficient architecture design.

In this paper, DTCWT architectures are designed that can operate at high frequencies and reduced computation complexity. Design of efficient DTCWT architectures are presented in next section.

III. DTCWT ARCHITECTURE

As the PQ signals are processed by 8-levels of DTCWT filter structure, each of the filter banks consists of four filters {LP and HP} for real and imaginary DTCWT sub band coefficient computation. Each of the filters requires 10 filter coefficients for data processing, and for every output sample to be computed it requires 10 multiplication and 9 addition operations per filter in order to reduce the number of arithmetic operations.

The responses of four filters denoted as $\{Y_{LR}, Y_{HR}, Y_{LI}, Y_{HI}\}$ for row processing are represented as in Equations (1) & (2), the responses are obtained by considering the similarities in filter coefficients, xi represents the input samples. From the output expression as represented in Equations (1) & (2), there are common output terms between $\{Y_{LR}, Y_{HR}\}$ such as $\{(x_{i+2} - x_{i+1}), (x_{i+3} + x_{i+4}), (x_{i+5} - x_{i+6})$ & $(x_{i+7} + x_{i+8})\}$ that are required to compute Y_{LR} and Y_{HR}. The reduced filter structure for computation of $\{Y_{LR}, Y_{HR}\}$ is shown in Figure 3.

$$Y_{LR} = h_1(X_{i+2} - X_{i+1}) + h_2(X_{i+3} + X_{i+4}) + h_1(X_{i+5} - X_{i+6}) + h_3(X_{i+7} + X_{i+8}) \quad (1)$$

$$Y_{HR} = h_3(X_{i+2} - X_{i+1}) + h_1(X_{i+3} + X_{i+4}) + h_2(X_{i+5} - X_{i+6}) - h_1(X_{i+7} + X_{i+8}) \quad (2)$$

The first group of 10 inputs represented by Xi is loaded into the register array. The terms ai = $x_{i+2} - x_{i+1}$, ai+1 = $x_{i+3} + x_{i+4}$, ai+2 = $x_{i+5} - x_{i+6}$ and ai+3 = $x_{i+7} + x_{i+8}$ are computed and stored in intermediate register array.

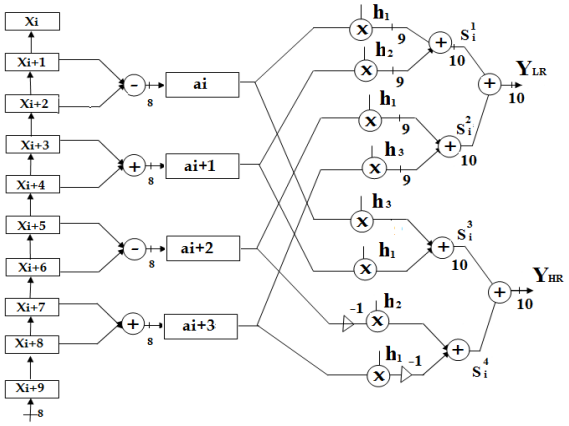

Fig 3. Reordered Pipeline filter architecture (Real)

Table-I: Comparison of hardware requirements

Parameter	1st Stage Processing	
	Modified architecture with pipeline	Generic DTCWT architecture
Multipliers	16	40
Adders	20	36
Throughput	1T	4T
Latency	14T	24T
Pipeline stage	4	Nil
Intermediate memory	32	20

IV. OPTIMUM ARCHITECTURE FOR DTCWT FILTER

From the discussions presented in the previous section, by considering similarity in DTCWT filter coefficients between high pass and low pass filters the common terms were simplified and a reduced order DTCWT architecture was designed using four stage pipelined structure that could simultaneously compute both Y_{LR} and Y_{HR}. Further observations on the common factors between DTCWT low pass filter and high pass filter of both real and also imaginary filters an optimum architecture is designed. The first stage of DTCWT processing have four filters in which the first pair representing real and second pair representing imaginary tree, the filter coefficients between real and imaginary structure are found to be common and later reducing the common terms . The expression representing the output terms of first stage four filters represented as Y_{LPR}, Y_{HPR}, Y_{LPI} and Y_{HPI} are realized using the optimum structure shown in Figure 4.

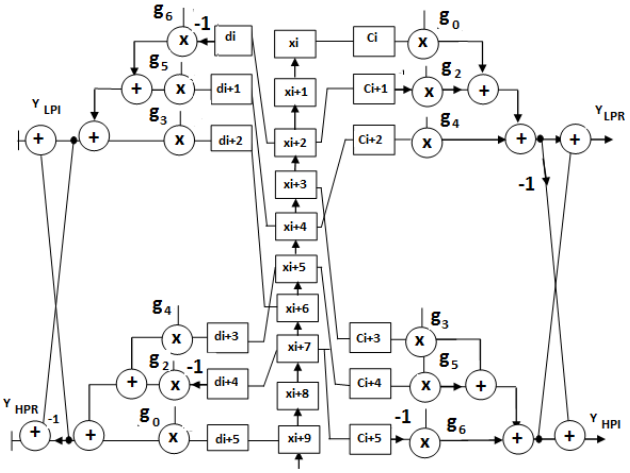

Fig 4. Optimal Pipelined Filter Architecture

The reduced architecture for level-1 processing comprises of 10 input registers, into which the input data is first loaded. The data path control unit reads corresponding elements into another register array represented by c and d. The contents of registers c and d are correspondingly multiplied by the filter coefficients and are build up in two stage adder array. A last stage accumulator unit designed as butterfly structure generates the real and imaginary components.
With four outputs being generated every clock cycle for four filters simultaneously the optimal structure is faster and also requires less number of arithmetic units for data processing. Table 2 summarizes the data path metrics of designed optimal DTCWT structure.

Table-II: Comparison of hardware requirements

Parameter	1st Stage Processing			
	Direct Structure	Reduced Order Structure	Optimal Structure	Improvement %
Multipliers	40	16	12	70
Adders	36	20	12	67
Throughput	4	1	1	75
Latency	24	14	15	37.5
Pipeline stage	Nil	4	4	-
Intermediate memory	20	32	32	37.5

One of the major advantages of the optimal structure is that the throughput in terms of number of output per clock cycle is estimated to be 4 which imply the proposed architecture is four times faster than direct structure implementation with additional cost in increase in number of intermediate registers by 37.5%. The designed optimal architecture for DTCWT computation is modeled in Verilog HDL and is implemented on FPGA platform using Xilinx ISE 14 version targeting Virtex-5 pro FPGA family.

V. RESULT AND DISSCTION

A. Simulation Results of DTCWT

The synthesized DTCWT processor is simulated to check for its logic correctness by simulation considering test vectors. The simulation results of level 1 and level-8 are captured and test results are shown in Figure 5. From the simulation results it is found that the 1D-DTCWT (One-dimensional Dual-Tree Complex Wavelet Transform) processor results are matching with as per the theoretical requirements. A known set of data input representing the PQ data signal is generated in the test bench and is used as test vector. The test data applied to the DTCWT processor computes the intermediate sub bands and the final sub band results. The final results are captured and are compared with MATLAB results for validations. Inverse DTCWT is carried out for validation of DTCWT and Inverse DTCWT processor.

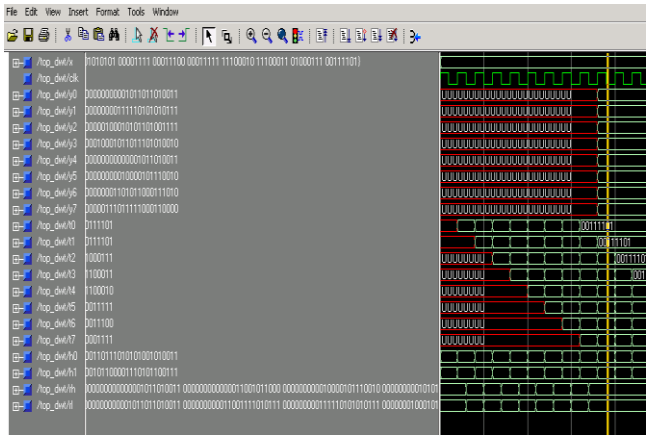

Figure 5. Results of 1D DTCWT processor using Modelsim

The eight levels DTCWT results presented in Figure 6 demonstrates the logic correctness of DTCWT logic developed in Verilog HDL

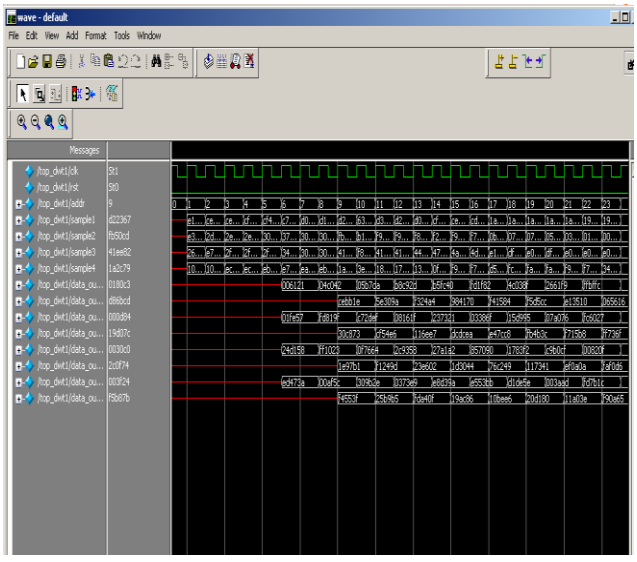

Fig 6. 1D DTCWT of frame1 Simulation results

The synthesized net list of top module 1D DTCWT is shown in the Figure 7(a). The top module netlist obtained demonstrates that the DTCWT processor computes eight levels of decomposition from the input data. Figure 7(b) shows the internal architecture of 1D DTCWT synthesized net list.

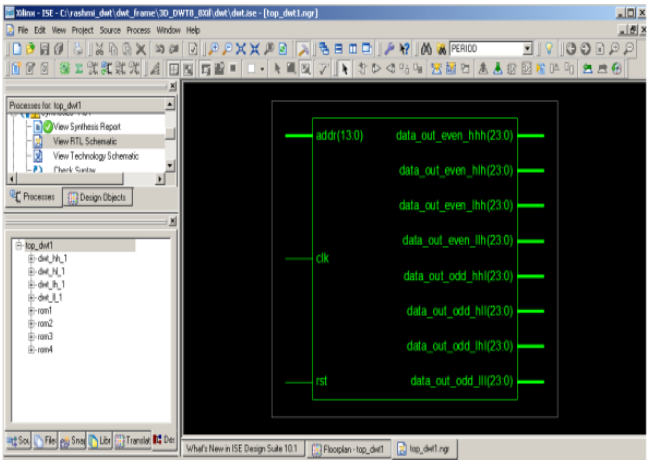

Fig7 (a). Top module 1D-DTCWT Synthesized net list

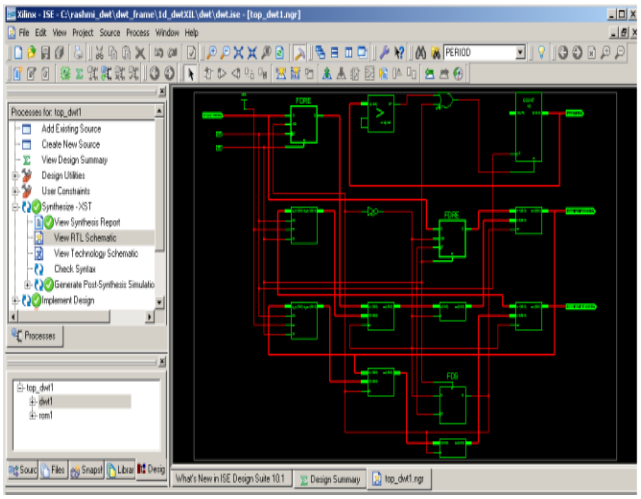

Fig7 (b). Internal architecture of 1D-DTCWT Synthesized net list

B. FPGA Implementation Results of DTCWT

The DTCWT architecture is synthesized in Xilinx tool, post place, map and route simulation also have been carried out. Power, area and timing are obtained by optimized design. FPGA implementation results of DTCWT and Inverse DTCWT are shown in Table 3.

Table-III: Implementation results of DTCWT

	Proposed DTCWT	**Ref [11]**	**Proposed Inverse DTCWT**	**Ref [11]**
Slice Logic utilization	Used	Used	Used	Used
Number of Slice Registers	3672	4112	6482	8734
Number of Slice LUTs	3173	4091	7224	9122
Total quiescent power	0.38010 (W)	0.40110 (W)	1.00016 (W)	1.00133 (W)
Total dynamic power	1.19011 (W)	1.31001 (W)	1.00191 (W)	1.10004 (W)
Total power	1.57021 (W)	1.71111 (W)	2.00207 (W)	2.10137 (W)

For DTCWT computations out of 69120 registers available less than 5% is the utilization of resources in terms of LUTs and Slices. The maximum operating frequency of the planned design on Virtex-5 pro FPGA is found to be 288 MHz for DTCWT and also 268 MHz for Inverse DTCWT processor. From the results obtained the proposed DTCWT processor can operate greater than 200 Msps speed which is more than what is expected that is 2ksps.

VI. CONCLUSION

Dual Tree Complex Wavelet Transform (DTCWT) based architectures are designed and implemented on FPGA Virtex-5 Platform to archive High speed low power area. The 8-level DTCWT filter bank structure with 10-tap filter coefficients is designed with 16 multipliers and 8 adders for each filter bank stage. The multiplexing scheme designed for the FFNN multiplier stage and adder stage reduces the arithmetic units by less than 20%. The designed DTCWT is configured on FPGA operate at a maximum frequency of 268 MHz. Together the area utilization is less than 8% and power dissipation is less than 2W. The designed modules are suitable for real time PQ analysis and can be used as IP cores in smart meters.

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Dr.Prathibha did her B.E during 2000 from Kuvempu University and M. Tech in VLSI Design & Embedded System during 2010 and Ph.D in 2018 in power quality from Viswesvaraya technological University, Karnataka. She is working in the Department of Electrical and Computer Engineering, Adama Science and Technology university, Adama, Ethiopia. Published 13 International and National journals, 28 International and National Conferences. Her Research areas of interest are power quality, Smart grid, and renewable energy. She is the life member of Indian society for technical education.

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