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Design of Low Power Adder Cell by XOR & XNOR Gate

Rahul Jadia, Sonali Joshi

Abstract: ***In under this research article, neoteric circuits for Exclusive OR gate and Exclusive NOR gate are designed. The designed logic is highly refined in terms of power consummation and speed, which are due to minimum CL at the output and low leakage power. We followed six novel hybrids, one bit one full-adder design based on the new Exclusive OR gate and Exclusive NOR (XOR-XNOR) gates. Many Relevant designed logics carries its advantages within aspect relevant to delay power, dissipation power, speed, as well as all that. Within validate the presentation of the introduced design, major SPICE as well as Tanner EDA simulations function as executed. This simulation outcomes, arrange at a 65-nanometer based on hybrid technique process, reveal for the introduced architecture have the best speed and power in contempt of different Full Adder architectures. The proposed design has a minimum power of 0.8 nw & delay of 9.4 ns, which is very optimized & efficient than the reference design. The previous design has 4.08-microwatt power. We customized the design with 22T and change the design methodology to make the results optimized.***

Keywords : ***Tanner EDA, Power, Delay, Digital Circuit Design, Power Optimization, CMOS, Pass Transistor, Full adder (FA), XOR-XNOR, Transistor (T), Hybrid Full Adder (HFA) [14], Sleepy-Gate Diffusion Input (S-GDI) [20], Complementary Pass Transistor Logic (CPTL) [20], Economized Pass Transistor Rationale (EEPL) [20], Differential Cascade Voltage (DCV) [20], Pass Transistor Logic (PTL) [20], Transmission Gate (TG), Complementary CMOS technique (CCT) [20].***

I. INTRODUCTION

Nowadays, electronic devices have a very vital role in everyone's day to day life. Systems like phones, tablets, and laptops have become necessary instruments in our day to day life. Customer prefers portable & battery-operated gadgets. In the '90s, the performance and speed were the most critical key to design any system but nowadays optimized computing, and wire-free communication and low power have become one of the critical factors in the continued progress of VLSI Design.

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In VLSI, power dissipation plays the primary role in circuit design. In a static CMOS design, we get a stable output and high fan-out with low power consumption static and dynamic power consumption. Inactive control utilization is due to spillage current, and energetic control utilization is due to the move of the capacitor, and third control utilization is due to a short circuit that occurs due to the transition of the pulse. For a long period getting high performance from design, high dense packaging, and low power to less, the transistor size scaling is required. There is a lot of design topology in the VLSI design to connect the NMOS & PMOS in a manner.
Initially we have worked with CMOS, The CMOS has a very stable output; that is why it has the highest fan-out ever in all logic design family. However, due to the static nature of CMOS, the number of transistors in CMOS. By using the hybrid topologies, we can reduce the number of transistors, the power estimation factor as well as delay.

II. LITERATURE SURVEY

"Design and Derivative of Low-Power FA using 65 nm Complementary Metal-oxide Semiconductor Technology." [16]

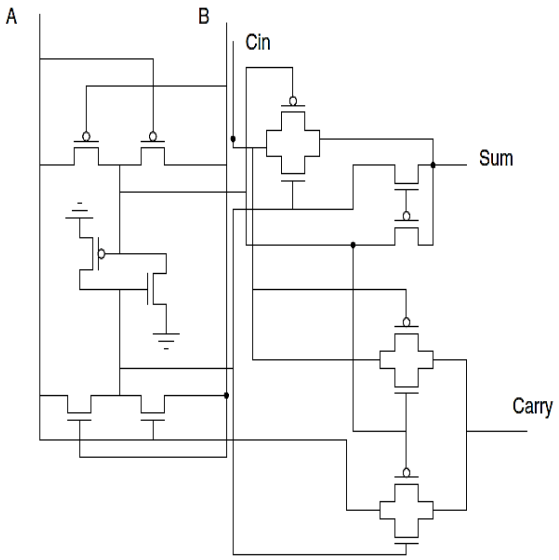

Fig.1 14 T full-adder [16]

This research proposes a low energy one-bit full adder utilizing 65nm 14T and Complementary Metal-oxide Semiconductor Technology by taking the merits of present full adders. The introduced one-bit full adder has the least power consummation. An analytical comparison of average power and maximum power was performed with one-bit FA.

The simulated design and corresponding results have been presented using the Tanner EDA tool.[16]

"Novel 11-T FA In 65NM Complementary Metal-oxide Semiconductor Technology." [18]

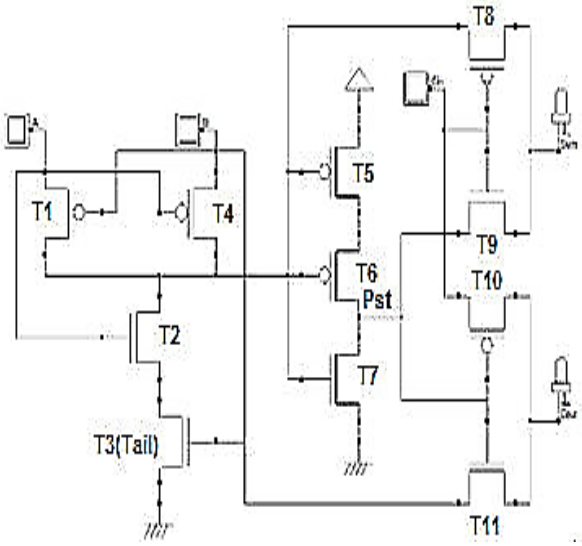

Fig.2 11 T full-adder [18]

This research proposes an improved 11T one-bit FA design for min power consummation. A replacement adder circuit is meant with a replacement proceed towards using the amount of 11-transistors, hence, referred to as an 11-transistors cell. After simulation of the circuit, a transparent view of the circuit performance is studied. The improve adder circuit is compared with reference cells and find it lower in power consummation. The new cell gives quicker for the carry outturn and can be used at greater temperature with least power depletion. The obstacle of the circuit is that it intrigues more region on the chip. [18]

"S-GDI —Splendid Low Power science for Digital Design." [20]

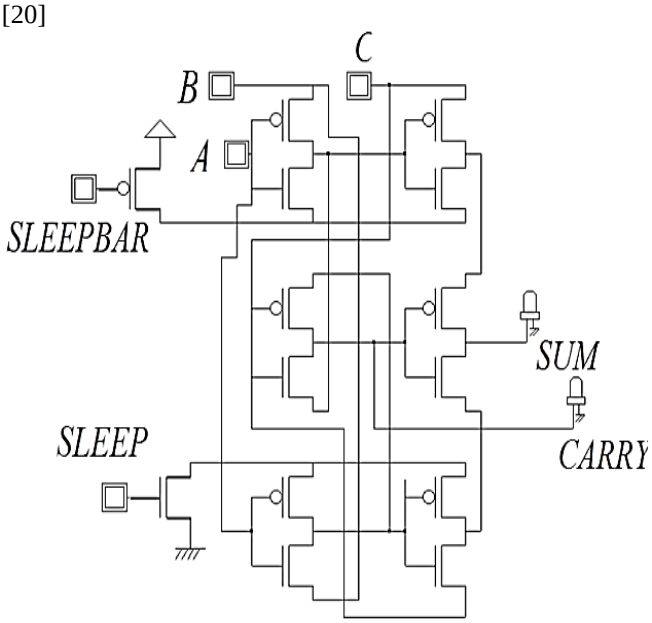

Figure 3: S-GDI ADDER 65nm [20]

In this research work, this proposed an energy-saving technology called S-GDI as can be drawn on for improved electronic architecture at low-power works. Towards concentration as well as power evaluation, ten former methods function as used into contemplation and occupied in effect Exclusive OR gate, one-bit comparator, one-bit adder, and four-bit up and down counter. Each technology parameters characterize and analysed in use 65-nanometer technique. That introduced sleepy gate diffusion input method has come to be checked power saving while CPTL, CCT, DCMOS, Vitality EEPL, DCV, Switch with Pass Entryway Rationale (DCVSPG), Incline Integration with Pass Transistors (LEAP), PTL, PPL, CMOS with TG and GDI. In comparison to S- Gate Diffusion Input acts as expos 96.20%, 93.65%, 97.88%, and 98.22% power measurements towards EOR, one-bit adder, one-bit comparator, as well as four-bit up-down counter successively. S-Gate Diffusion Input represents appearance region in sequence based on 17.16% as well as 28.1% towards EXOR, 41.26%, as well as 53.89% toward a one-bit adder, 7.6%, as well as 21.76% for one-bit comparator and 6.7% as well as 28% towards up-down counter over EEPL and DCMOS techniques progressively. As much as different methods, apart from EEPL as well as DCMOS, exist as region preserver even as analysed to the introduced technology, however such is next to an expenditure on greater thorough power dissolution. Thus, PDP consisting of measured technologies function as similarly determined done with 65 nano-meter process toward each SUM as well as CARRY outturns from the one-bit adder. Within each issue, the power delay solutions of S-Gate Diffusion Input methodology represent particularly reduced as respects toward each one different methodology. Consequent efficacy on Sleepy Gate Diffusion Input in respect of measured scale, certain method could be spontaneously put-upon toward low-power approaches. [20]

"1-Bit Sub Threshold FA in 65nm Complementary Metal-oxide Semiconductor Technology." [19]

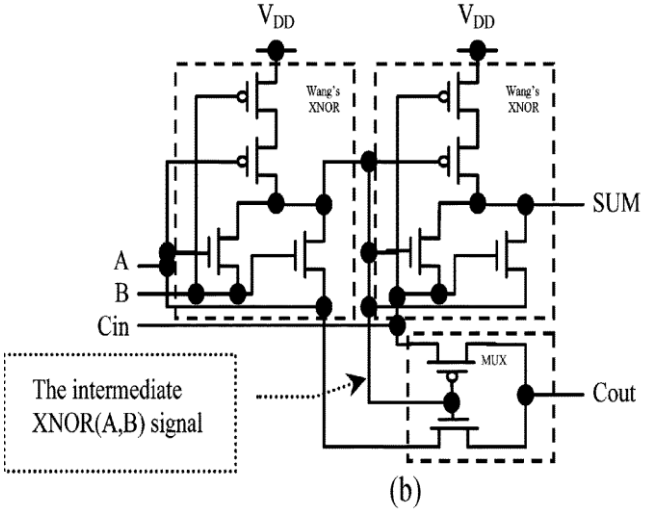

Fig.4 SERF 1-Bit Full Adder at 65nm [19]

In this research work, a new FA circuit improved for extreme-low power implementation. The circuit design used improved XOR gates driven in the sub-threshold region to decrease power consummation. Derivative consequences are equipped with 65nm standard Complementary Metal-oxide Semiconductor models. The simulated outcomes represent a 5%-20% for frequency 1 KHZ to 20 MHZ while supply voltages less than 0.3V. [19] "Low Power and High-Speed F-A on Analyzing Novel EOR and Exclusive NOR Gates." [14]

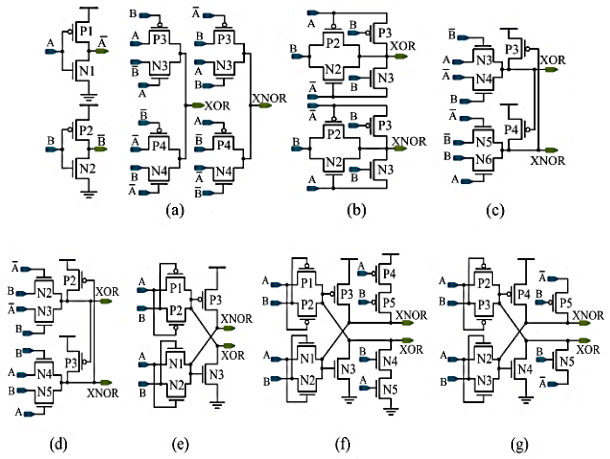

Figure 5: Low Power High-Speed FA Design of XOR & XNOR [14]

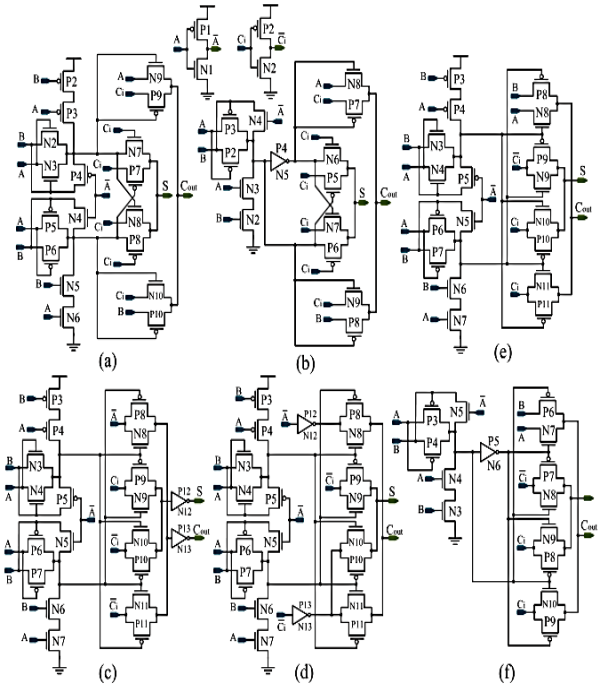

Figure 6: Proposed (HFA) Cell [14]

In this research work, inventive circuits for EOR/ Exclusive NOR and parallel EOR/Exclusive NOR functions are introduced. In the research, the author uses a novel design of XOR & XNOR and optimized the power & delay. Six transistors have used to make an XOR gate and XOR gate and implemented with the adder cell at 1.2V with the various frequency range. [14]

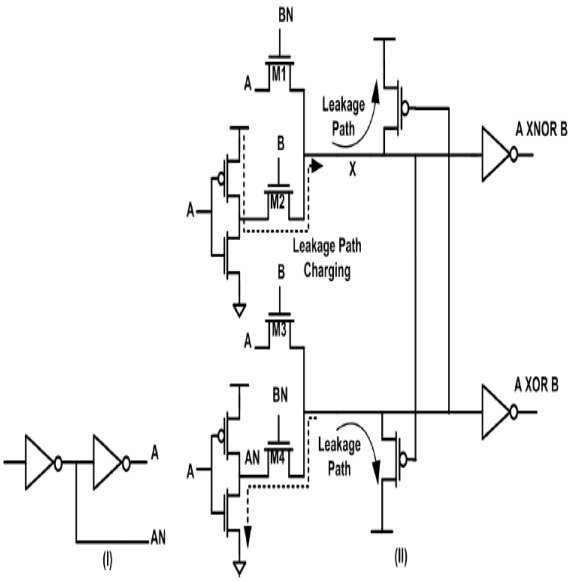

Fig.7 XOR-XNOR gate circuit at 65nm

III. Related Work & Design Methodologies

In the research, the author uses a novel design of XOR & XNOR and optimized the power & delay. Six transistors have used to make an XOR gate and XOR gate and implemented with the adder cell at 1.2V with the various frequency range. [14]

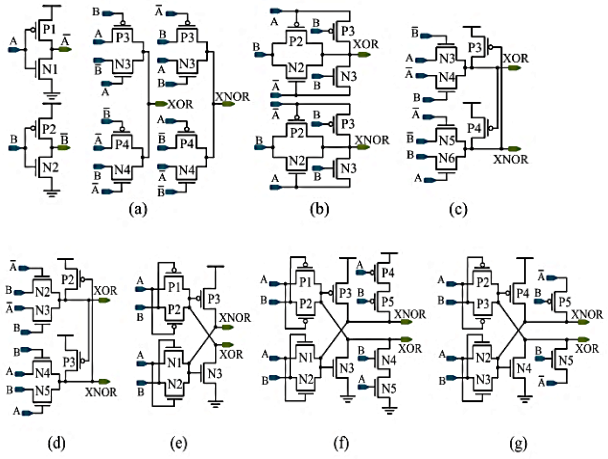

Figure 8: Reference Design of XOR & XNOR [14]

By using the above new XOR & XNOR author implemented the 6-type new low power adder cell and used a hybrid approach to design the adder cell with high fan-out.

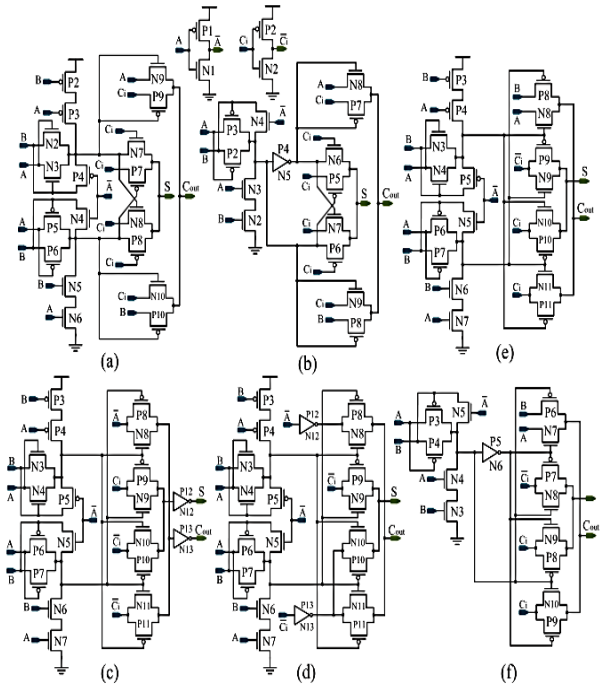

Figure 9: Reference Adder Cell [14]

IV. PROPOSED WORK (NEW ADDER CELL)

The proposed a new adder cell by using the reference methodologies. We found the avg. Power again, as shown in results. We used the tanner EDA 14.1 to implement the adder cell & helped to T-spice & W-edit for above the design has 22 transistors by using a hybrid approach. By using the help of reference new XOR & XNOR design to implement a new adder cell with low power in Nano watt & delay also. We found this design output very stable & with proper voltage levels.

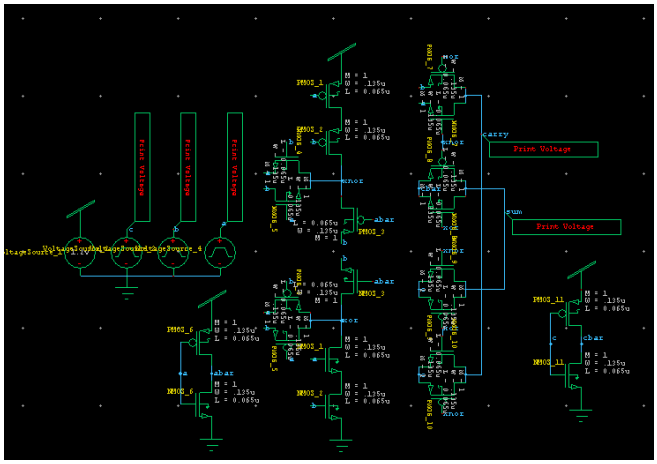

Figure 10: Proposed Adder Cell 22T 1.2 V Supply

Proposed Design Methodology

Hybrid Design

Total Transistor = 22

Modified Reference XOR & XNOR gate

The proposed design found the one-bit adder cell by using the arrangement of transistor above.

Voltage Supply – 1.2V.

Threshold Voltage – 0.2 ~ 0.3 V.

Tanner EDA

Avg. Power Consumption Command

. measure Tran delay trig V (a) Val=2.5 rise=1 + targ V(y) Val=2.5 rise=1

. measure Tran power avg P (vvoltageSource_1)

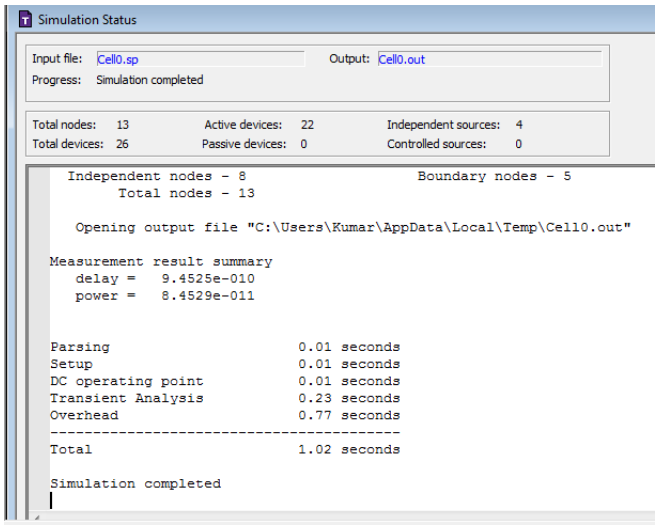

Figure 11: Proposed T-Spice Result of Adder Cell

V. SIMULATION RESULTS

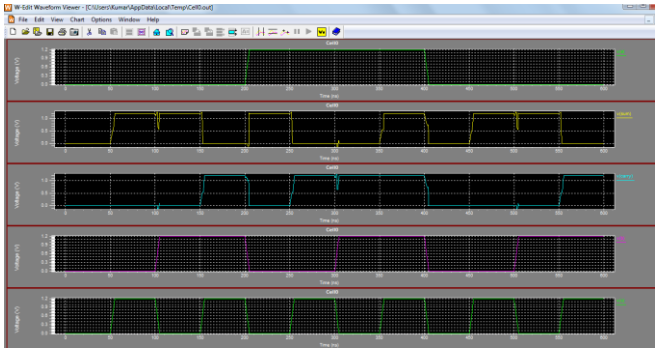

Figure 12: Proposed W-Edit Result of Adder Cell

Design	Avg. Power Dissipation	Delay
14T	2.975 uw	11.2ns
11T	0.321uw	10ns
Reference HFA -22T [14]	4.08 uw	21ns
S-GDI -14T	0.022uw	11ns
SERF 1-Bit Full Adder -10 T	0.0013 uw	10.5ns
Proposed HFA* - 22T	**0.8 nw**	**9.4 ns**

Proposed design * - 65nm 1.2 V Power Supply

Figure Table: Comparison b/w Reference & Proposed Results

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VI. CONCLUSION

In this research work, new circuit topology is used to cut down the power degradation of hybrid adder cells in digital circuits. After reviewing some paper at 65 nm, the proposed design is consuming very low power from the source an adder is a prime unit of ALU; if it works fast, then automatically the processing will get fast. In the future, we will design a multiplier cell from the designed new low power adder cell.

REFERENCES

1. N. S. Kim et al., "Leakage current: Moore's law meets static power, "Computer, vol. 36, no. 12, pp. 68–75, Dec. 2003.
2. N. H. E. Waste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2010.
3. S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-sub micrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large-Scale Integer. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.
4. H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power10-transistor full adders using novel XOR-XNOR gates," IEEE Trans.Circuits Syst. II, Analog Digit. Signal Process. vol. 49, no. 1, pp. 25–30, Jan. 2002.
5. S. Timarchi and K. Navi, "Arithmetic circuits of redundant SUT-RNS," IEEE Trans. Instrum. Meas., vol. 58, no. 9, pp. 2959–2968, Sep. 2009.
6. J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, vol. 2. Englewood Cliffs, NJ, USA: Prentice-Hall, 2002.
7. D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEEProc. -Circuits, Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.
8. K. Yano, A. Shimizu, T. Nishida, M. Saito, and K. Shimohigashi, "A 3.8-ns CMOS 16×16-b multiplier using complementary pass-transistor logic," IEEE J. Solid-State Circuit's vol 25, no. 2, pp. 388–395, Apr. 1990.
9. A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large-Scale Integer. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.
10. N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEEJ. Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.
11. N. Weste and K. Eshraghian, Principles of CMOS VLSI Design. New York, NY, USA: Addison-Wesley, 1985.
12. P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, and A. Dandapat, "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit," IEEE Trans. Very Large-Scale Integer. (VLSI) Syst., vol. 23, no. 10, pp. 2001–2008, Oct. 2015.
13. M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage-swing nodes," in Proc. IEEE Workshop Signal Process. Syst. (Sips), Oct. 1999, pp. 713–722.
14. H. Naseri and S. Timarchi, "Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 26, no. 8, pp. 1481-1493, Aug. 2018.
15. S. Wairya, R. K. Nagaria, and S. Tiwari, "New design methodologies for high-speed low-voltage 1-bit CMOS Full Adder circuits," Int. J. Compute. Technol. Appl., vol. 2, no. 2, pp. 190–198, 2011.
16. K. Paramasivam, Suresh Kumar N," Design and Analysis of Low Power Full Adder using 65nm CMOS Technology," International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-7 Issue-4S, November 2018.
17. S. Sunithamani*, V. Viswateja, S. Krishna Bharat, P. Lakshmi Prathyusha, K. Nikhil, "Area Optimization and Power Analysis of Hybrid 1-Bit Full Adder using Sleepy Keeper approach," International Conference on Instrumentation, Electrical and Electronics Engineering (ICIEEE'17) ISSN: 0974-2115 JCHPS Special Issue 9: June 2017.
18. C. M. R. Prabhu, Tan Wee Xin Wilson and Thangavel Bhuvaneswari, "NOVEL 11-T FULL ADDER IN 65NM CMOS TECHNOLOGY," ARPN Journal of Engineering and Applied Sciences, ISSN 1819-6608. VOL. 13, NO. 14, JULY 2018
19. Farshad Moradi, Dag T. Wisland, Tuan Vu Cao, Ali Peiravi, Hamid Mahmoodi, "1-Bit Sub Threshold Full Adders in 65nm CMOS Technology," 2008 International Conference on Microelectronics.
20. Anjali Sharma, Harsh Sohal, "Sleepy- Gate Diffusion Input (S-GDI) — Ultra Low Power Technique for Digital Design," International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-9 Issue-1, November 2019.

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Prof. Sonali Joshi has 12 years of teaching & research experience. She is member of IEEE & IETE technical societies. Presently she is working as Assistant Professor in Electronics Engineering Department of G H Raisoni College of Engineering, Nagpur. Her research area includes embedded systems, soft computing etc. She has published many research papers in nation & international journals of repute.