International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-9 Issue-1, May 2020

Design of Improved 8:1 Multiplexer using Quantum-dot Cellular Automata Technology

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Abstract*: *A much-required breakthrough in the field of VLSI took place with the birth of Quantum-dot cellular automata (QCA) technology, an impressive amalgamation of Quantum Physics and Nanotechnology and acted as a possible replacement to the age-old semiconductor transistor-based designs (CMOS) with Boolean paradigm. In this paper, we aim at implementing this technology to build a robust 8:1 multiplexer that can help in building and developing many more digital logic circuits, from an already proposed 2:1 multiplexer. It has excellent efficiency with respect to least cell count, latency, space and power dissipation.

Keywords:* *Quantum-dot cellular automata, VLSI, Nanotechnology, Multiplexer, Digital Logic circuits.

I. INTRODUCTION

Quantum-dot Cellular Automata (QCA) [1-3] is an emerging technique that has the potential to replace traditional and conventional CMOS technique. QCA offers a small size feature, low power consumption, very high switching speed, and high possibility of mass production of devices by the means of self-assembly. QCA consists of cells which are nanometer in size [4-5]. Logical circuits in QCA are built using these cells. Majority gate and inverters are the two building blocks of QCA using them, many researchers have developed various different logical gates and circuits. Multiplexer is very significant component in digital systems. It allows us to send one or more inputs over a single transmission line at different time or system. Multiplexer is designed so as to switch one of several input lines through to a single common output line by the application of a control signal. Using QCA, the design of multiplexer is optimized. QCADesigner is a design and simulation tool for Quantum- dot Cellular Automata developed in University of Calgary [3]. The remainder of the paper is divided into the following sections. Section II throws more light on the background of QCA. Section III talks about various implementation of 2:1 multiplexer. Section IV is about implementation of optimized 8:1 multiplexer and conclusions are drawn.

Manuscript received on April 02, 2020.
Revised Manuscript received on May 21, 2020.
Manuscript published on May 30, 2020.
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II. BACKGROUND OF QCA

A. History of QCA

Lent et al in 1993 introduced the concept of QCA. He created nano-scale devices by integrating the concepts of discrete nature of cellular automata and quantum mechanics. These devices were capable of performing at higher speed and consumed low power as compared to the traditional CMOS introduced by John von neumman.

B. Working of QCA

Generally, QCA consists of arrays of coupled quantum dots which can be used to implement different logic functions. In conventional method uses voltages or current to have a logical value however in QCA, electrons position determines the binary value. Each QCA cell consists of 4 points and two electrons that always occupy diagonally opposite position so as to obey the principle of coulomb repulsion. The cell polarization is determined on the electron position in the cell. The following figure shows us diagrammatically the logic 1 and logic 0 of a QCA cell.

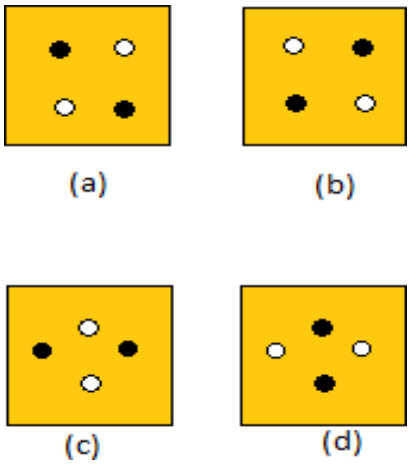

Figure 1. 90- degree QCA cell with two different polarization, Binary=0(a); Binary=1(b); and 45-degree QCA cell with two different polarization, Binary=1(c); Binary=0(d)

The clocking forms an essential part in the functioning of QCA technology as it permits the computation to take place in adjacent QCA cells. In a given circuit design, it synchronizes the data flow and controls the direction to reach the desired output. Hence, in QCA structures, following the clocking principle is very vital. It also acts as the power bank to the circuits; hence we need to keep the track of changes in clocks in long run. It primarily consists of four stages; Switch, Hold, Release and Relax, and functions in four different clock zones namely Clock 0, Clock 1, Clock 2 and Clock 3. The first stage, Switch makes a cell is vulnerable to change as it gradually increases the potential barrier and gets polarized according to the input given due to high potential difference. In the second stage, Hold, the cell contains and reserves its value for a given time. At this stage, the cell is immune to changes as the potential barrier becomes highly stable. In the third stage, Release, the potential barrier linearly decreases allowing the cell to lose its value and come back to its natural neutral state. Here, the information is already passed on to the adjacent cell following the clock zone principles. The fourth stage, which forms the last stage, Relax, has finally brought down the potential barrier of the cell and makes it non-polarized [6-15]. The information can be passed on only in a cycle from Clock 0 to Clock 1 to Clock 2 to Clock 3 to Clock 0 according to the graph given below.

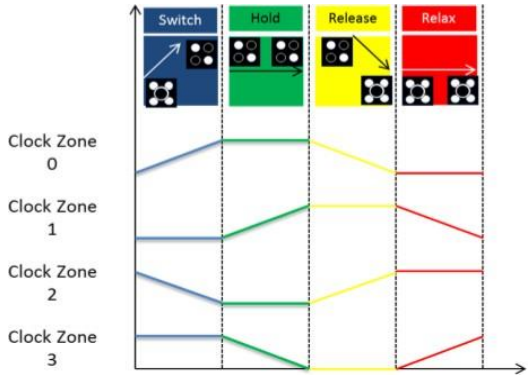

Figure 2. QCA clocking system.

III. 2:1 MULTIPLEXER

A multiplexer plays a very vital role in digital electronics world when it comes to handling many circuits or memory units, simultaneously, hence becoming a very important part in FPGA implementations. It usually has 2^n where input lines n select lines plugged in, through which one output is drawn. The 2:1 multiplexer is a digital logic circuit that is plugged in with two input and 1 select line which will be logic-set to determine the input line selected. The output drawn out of the given logic circuit hence depends on the select line. A basic 2:1 multiplexer design has two AND gates and an OR gate to satisfy the given logic:

$$OUTPUT = a.S'+b.S \quad (1)$$

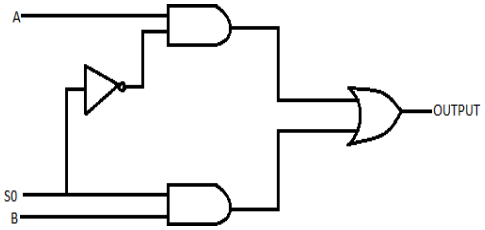

Figure 3. Multiplexer Digital Design

Using the QCA technology, we aim to optimize the runtime speed, space and make the circuit robust to high input frequencies on repetitive simulations. Therefore, the given generic design of the 2:1 multiplexer falls short for implementation in large circuit designs. The works of [5] in implementing 2:1 multiplexer has been taken into consideration to build the proposed 8:1 multiplexer as it has less cell count, is robust and efficient. It utilizes intrinsic nature of quantum technology for working and does not follow Boolean principles. The functioning of the design can be explained by splitting it into two symmetrical halves along S0 laterally. When the Boolean logic at S is 0 (QCA logic = -1), the upper half of the circuit gets activated, that is, input A gets selected and the output drawn out of the multiplexer becomes input A. Similarly, when the Boolean logic at S is 1 (QCA logic = +1), the lower half of the circuit gets activated, that is, input B gets selected and the output drawn out of the multiplexer becomes input B. As the area, latency and robustness of the design is excellent compared to other designs, the design has further been extended to design the proposed 8:1 multiplexer.

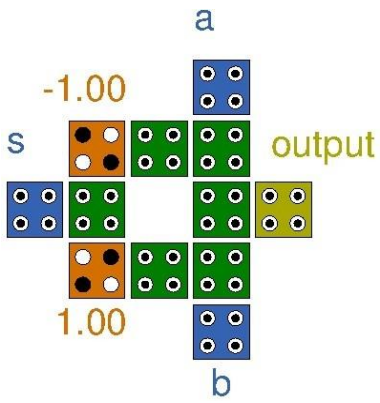

Figure 4. Chosen 2:1 Multiplexer design using QCA Technology.

IV. 8:1 MULTIPLEXER

The proposed 8:1 multiplexer consists of seven 2:1 multiplexer as shown in Fig 6, thereby containing 11 inputs, 1 output. There will be 2048 rows in the truth table which is very large. The following Table I interconnects the 8 inputs to 1 output using the 3 select lines S0, S1, S2.

Therefore, according to Table-I, when the values of S0, S1 and S2 collectively is 000 bit, the input A gets selected as the output. Similarly, the rest of the combination of select lines follows.

The proposed QCA layout of 8:1 multiplexer is shown below in Fig 8, which is constructed using 7 multiplexer gates. In this design; A, B, C, D, E, F, G, H are the 8 inputs and S0, S1, S2 are the 3 select lines and OUTPUT is the final output of the whole multiplexer.

The select lines selects A as output when the values of S0 S1 S2 is 000, selects B as output when S0 S1 S2 equals to 001, selects C as output when S0 S1 S2 equals to 010, selects D as output when S0 S1 S2 equals to 011, selects E when S0 S1 S2 equals to 100, selects F when S0 S1 S2 equals to 101, selects G when S0 S1 S2 equals to 110 and selects H when S0 S1 S2 equals to 111. The logic of the proposed QCA layout is given as:

$$OUTPUT = S0'.S1'.S2'.A + S0'.S1'.S2.B + S0'.S1.S2'.C + S0'S1\ S2\ D + S0\ S1'S2'\ E + S0\ S1'\ S2\ F + S0\ S1\ S2'\ G + S0\ S1\ S2\ H \quad (2)$$

Table- I: Truth table of given 8:1 Multiplexer

Inputs (Select Lines)			Output
S0	*S1*	*S2*	
0	0	0	A
0	0	1	E
0	1	0	C
0	1	1	G
1	0	0	B
1	0	1	F
1	1	0	D
1	1	1	H

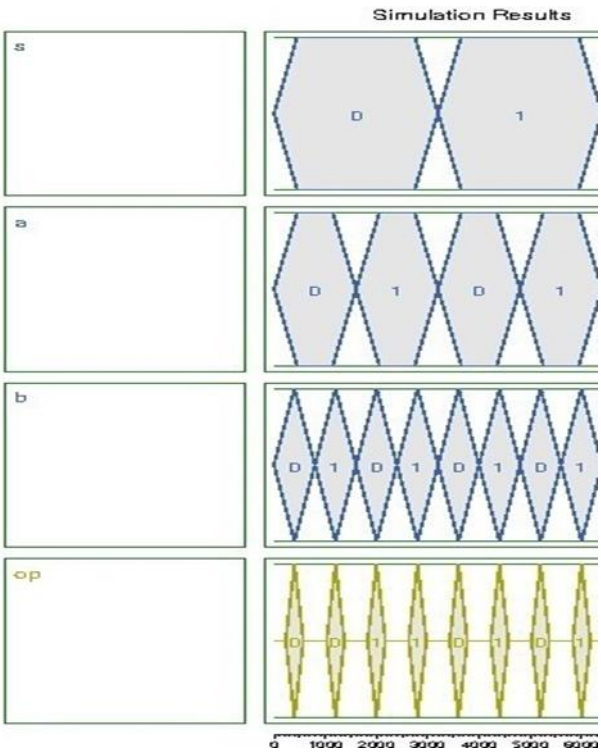

Figure 5. Chosen 2:1 Multiplexer design simulation results using QCA Technology

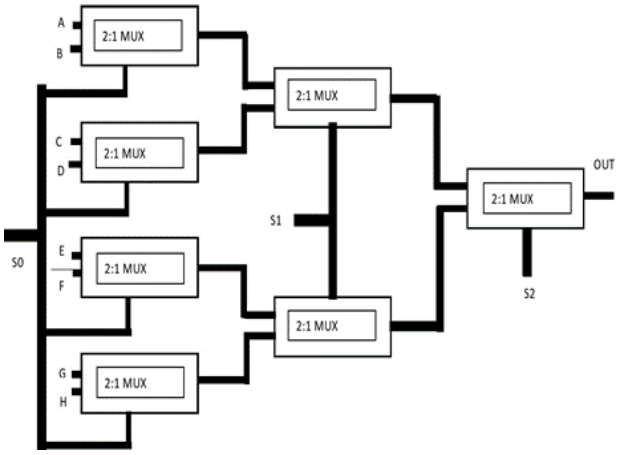

Figure 6. Implementation of 8:1 Multiplexer using 2:1 Multiplexer

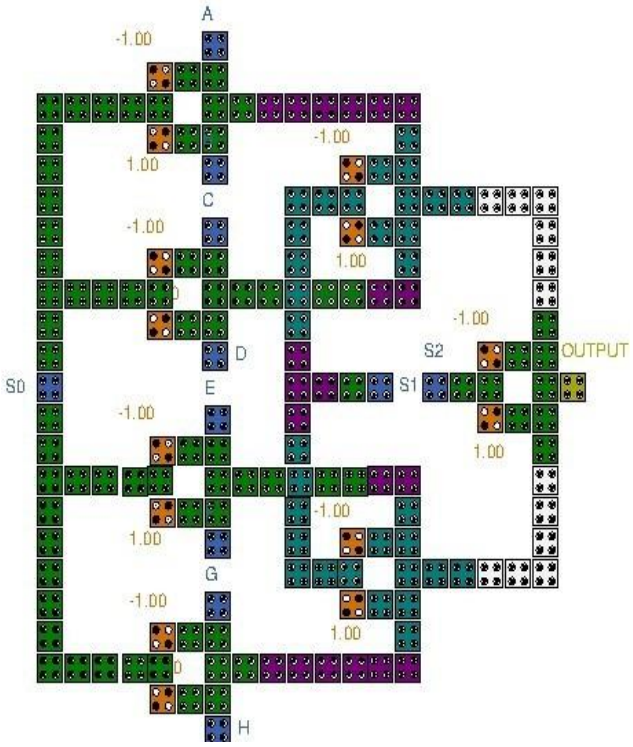

Figure 7. QCA Design of proposed 8:1 MUX

V. SIMULATION RESULTS

The proposed structure of 8:1 multiplexer is stimulated with QCADesigner version 2.0.3 with default simulation parameters. The desired output is achieved with a delay of one clock zone. In addition, this design is built using 164 cells on 0.23 micro meter square area. The stimulation results of the proposed 8:1 multiplexer is provided with input and output wave forms below. The input vector table that was given to the circuit is as shown in Table II. The expected output according the truth table should be as 00110011. The stimulated output in Figure 8 of the 8:1 Multiplexer shows the expected output of 0011001 with a delay of one clock zone.

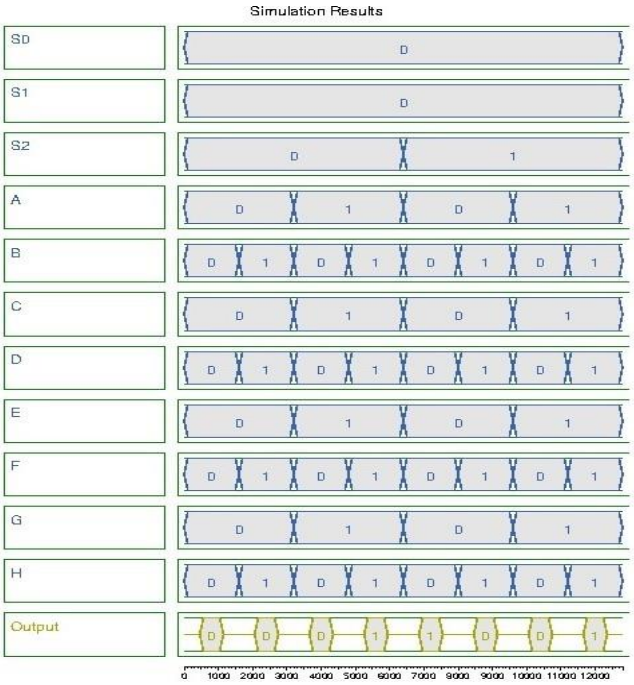

Figure 8. 8:1 Multiplexer design simulation results using QCA Technology

Table- II: Inputs given to proposed 8:1 Multiplexer

Inputs											Output
S0	***S1***	***S2***	***A***	***B***	***C***	***D***	***E***	***F***	***G***	***H***	
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	1	0	1	0
0	0	0	1	0	1	0	1	0	1	0	1
0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1
0	0	1	1	0	1	1	1	1	1	1	1

VI. CONCLUSION

After diversely studying various multiplexers, we built the proposed design. Multiplexer is a very vital and fundamental element in digital circuits, hence building an efficient design will open gates to laying fundamental design to many complex circuits. Within this paper, various designs of 2:1 multiplexers were reviewed. The most optimized 2:1 multiplexer was chosen to construct the proposed 8:1 multiplexer that is presented in this paper. The comparison in Table III between the works of existing 8:1 multiplexer design with the proposed design shows improvement in cell count, latency and area compared to the previous QCA designs of multiplexer. Thereby making the proposed design more efficient and robust than all the referred previous works. This multiplexer circuit can be used in designing the core of Arithmetic-Logic Unit (ALU) processor by integrating various functionalities with a given logic to produce meaningful outputs.

Table- III: Inputs given to proposed 8:1 Multiplexer

Referred paper	Cell count	Area of occupancy (μm^2)	latency
[10]	633	0.67	11
[11]	576	0.82	9
[12]	462	0.87	7
Proposed design	164	0.23	6

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