Fully Parallel Architecture of QC-LDPC Decoder for IEEE 802.11n Application

Monica Kalbande, Shweta Hajare, Tejswini Panse, Pravin Dakhole

Abstract*: A Low density parity check (LDPC) code, have become most accepted error correction code for efficient and reliable communication due to a good performance. The VLSI implementation of LDPC decoder is a big challenge. Iterative message passing decoding algorithms propose excellent error correction performance but a large decoding complexity for different code lengths and code rates. The LDPC codes decoder also faced many difficulties such as small chip areas , reduced interconnect complexities, lower power dissipation. In this paper, the design of the of Quasi Cyclic(QC)LDPC decoder for the IEEE 802.11n standard with 1/2 code rate, 648coward length and sub-block size z =27 have been designed. Initially different iterative algorithms for LDPC decoding are discussed. The Fully parallel architecture of the LDPC decoder for IEEE 802.11n standard using Min Sum decoding algorithm (MSA)has been designed. Further, the design Quasi Cyclic(QC) LDPC decoder for IEEE 802.11n have been modified by using a Finite State Machine (FSM) to control the complete decoding process.

Keywords* : IEEE 802.11n , LDPC decoder, Min Sum, Quasi Cyclic.

I. INTRODUCTION

Forward-error-correction (FEC) can detect and correct the error at the receiver end show increase in parameters like the speed, throughput, and less power consumption of the system. FECs are used in the satellite or deep space long distance communication, wireless communication and storage devices [6]. Many coding techniques of forward error-correction schemes may be used for the error correction in the communication system. The very first error correcting code known as the hamming code was invented in 1950. Hamming codes have an ability to detect maximum two-bit errors and correct it up to one-bit errors. In 1959, Hocquenghem, Bose and Ray-Chaudhuri introduced BCH codes which belong to a type of cyclic error correcting codes. Afterward, the Reed-Solomon code due to its good burst error correction property, it is used in CDs, DVDs and hard disks. In 1962 Gallager introduced a new code known as Low-Density Parity Check Codes (LDPC). But it was ignored up to 1990's. In between a new code was introduced known as convolutional codes. These codes are used for digital video, mobile communications and satellite communications. The turbo codes were introduced which has better error performance close to Shannon limit. Due to more decoding complexity of turbo code, the LDPC codes[1] were introduced by R. Gallager in 1960's in his PhD Thesis. These were again discovered by David MacKay and Neal in the mid-nineties[2]. LDPC codes beat all existing codes with its good error performance and less hardware complexity. All above error correction codes are studied on the basis of type of codes, their inventions, decoding algorithms and applications. LDPC codes have been accepted by the recent standards such as WLAN (IEEE802.11n), Mobile WiMAX (IEEE802.16e), DVB-S2 and, 10GBaseT (IEEE802.3an).

Quasi Cyclic(QC)LDPC codes beat all existing codes with their good error performance and less hardware complexity .The iterative message passing decoding algorithms propose excellent error correction performance and a good decoding complexity. A soft-decision based Sum-Product Algorithm (SPA) achieves good decoding performance but results into a very high decoding complexity [7]. To simplify the check node operation in SPA many modifications have been recommended. The check node operations are simplified by minimizing the non-linear function [8,9] and logarithmic functions which results into the reduction of implementation complexity [10].The another soft decision based algorithm is Min–Sum algorithm(MSA) [7] in which check-node operations of SPA algorithm are simplified to reduce the decoding complexity but at the same time it decreases the decoding performance. Hence many modifications [11] are suggested in the MSA algorithm as normalization of MSA decoding and off-set of MSA decoding to trade off between decoding complexity and error performance.

II. ITERATIVE DECODING

As per the Decoding complexity and error performance requirements of decoder, LDPC codes are iteratively decoded in many ways. Message passing is an iterative decoding algorithm that uses the structure of the Tanner graph. Message passing algorithm broadly classified into hard decision and soft decision.

Revised Manuscript Received on May 21, 2020.

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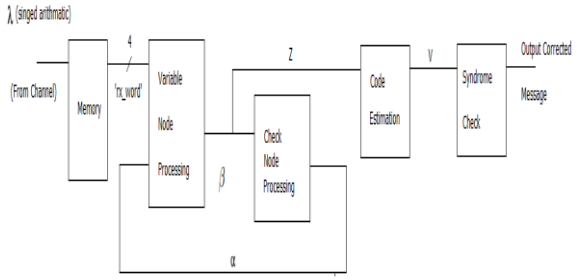


Fig.1 Iterative Decoding Algorithm

The Soft decoding algorithms based on the sign and magnitude(i.e. reliability information) whereas the hard decision decoding based only on the sign. In these algorithms, row and column operations are performed iteratively using check node message processing and variable node message processing. The iterative decoding algorithm is shown in "Fig.1" [12]–[16].Sum Product Decoding Algorithm (SPA)and Min Sum Decoding Algorithm (MSA)are two soft decision based decoding algorithms.

A. Sum Product Decoding Algorithm(SPA) [3]

Step 1 :Initialization :

The information λ_i derived from the Log-Likelihood Ratio (LLR) of received symbol y_i is computed by using " (1)".

$$\lambda_i = \ln\left(\frac{P_i(x_i = 0 \mid y_i)}{P_i(x_i = 1 \mid y_i)}\right) \tag{1}$$

Then for each iteration, αij are the messages from check node to variable node and βij the messages from variable node to check node are computed by using the tanner graph.

Step 2: Check Node Update(CNU) Processing:

In the Check Node (CNU) Update processing, αij messages are computed using "(2)".

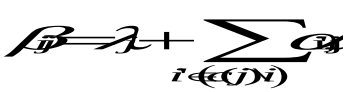
(2)

Where,

(3)

Step 3: Variable Node Update(VNU) Processing :

In the Variable Node Update(VNU) processing, βij messages are obtained by adding received information to λ. In Variable node update , βij messages are computed by "(4)".



(4)

Step 4 : Code Estimation:

The code estimation is given by "(5)".

$$\hat{Vi} = \begin{cases} 1 & if \quad yi < 0 \\ 0 & if \quad yi \geq 0 \end{cases} \tag{5}$$

Step 5 : Syndrome check:

Syndrome check "(6)" is given below for error detection purpose.

$$\begin{bmatrix} 00110\,010 \\ 1000100\,1 \\ 01001100 \\ 01010100 \\ 10001010 \\ 01010\,001 \end{bmatrix} \begin{bmatrix} v0 \\ v1 \\ v2 \\ v3 \\ v4 \\ v5 \\ v6 \\ v7 \end{bmatrix} \begin{cases} = 0 & if\ No\ error\ (Stop\ \mathrm{Pr}\,ocessing) \\ \neq 0 & if\ error\ occure(\mathrm{Re}\,peat\ \mathrm{Pr}\,ocessing) \end{cases} \tag{6}$$

Min-Sum Decoding Algorithm (MSA)[3]

Step:1 Check Node Update (CNU)Processing:

In the MSA decoding algorithm, the check node operation in SPA decoding algorithm is simplified by estimating the magnitude calculation in check node update processing with a minimum function]as shown in "(7)".

$$\alpha_{\mathrm{i,j\ MinSum}} = \underbrace{\prod_{j' \in V(i) \setminus j} sign\left(|\beta_{ij'}|\right)}_{Sign} \times \underbrace{\min_{j' \in V(i) \setminus j} \left(|\beta_{ij'}|\right)}_{Magnitude} \tag{7}$$

Step:2 Variable Node Update(VNU) processing :

The Variable Node Update(VNU) processing operation in MSA decoding algorithm is same as SPA decoding algorithm denoted by "(4)".

III. QUASI CYCLIC(QC)LDPC DECODER

Quasi Cyclic(QC)LDPC decoder architectures are categorized as fully parallel, serial and partly parallel. The partly parallel decoder architectures, row (Check Node) computation and column(Variable Node) computation operations are partly in parallel results into higher throughput compared to serial architecture. In the fully parallel architecture, the check node update(row)processor is directly connected to the variable node update(column) processor. Fully parallel decoder architectures have high complexity between interconnect of row(Check Node) processor and column (Variable Node) processor but deliver very high throughputs. Hence VLSI implementation of the fully parallel Quasi Cyclic(QC)LDPC decoder is the major challenge in the communication system.

IV. A FULLY PARALLEL ARCHITECTURE OF QUASI CYCLIC (QC)LDPC DECODER FOR IEEE 802.11N

The fully parallel architecture show that every check node of the parity check matrix H connects to the variable node. The advantage of fully parallel architecture is the highest throughput and lowest latency. The block structure of a proposed fully parallel decoder for the 1/2 code rate and 648 codeword length is shown in

"Fig.2" which consists of 648 variable nodes and 324 check Nodes.

A. CHECK NODE UPDATE (CNU) UNIT

In the Check node update processing operation the comparison of the modulus/magnitude of the inputs has been calculated. XOR gate is used for the sign bit calculation. The inputs and outputs are represented in sign-magnitude representation. The check node update processing unit of MSA decoding algorithm is shown" Fig.3"[17].

B. VARIABLE NODE UPDATE(VNU) UNIT

In Variable node update processing, the updated output messages from Check node processor units are added with the information obtained from the channel. The Variable Node Update unit of MSA decoding algorithm is shown" Fig.4"[17].

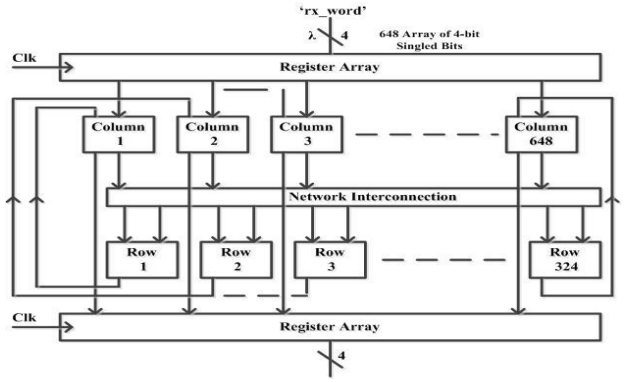


Fig.2 The fully Parallel architecture of Quasi Cyclic(QC)LDPC decoder for IEEE 802.11n

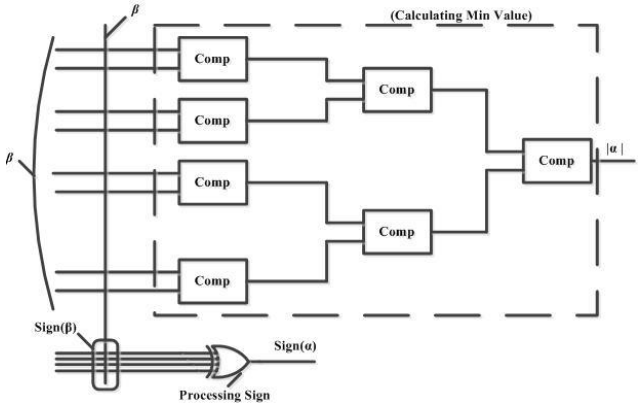


Fig.3 Check node update (CNU) unit

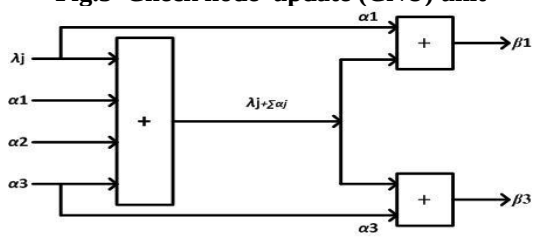


Fig.5 Variable node update(VNU) unit

V.QUASI CYCLIC (QC) LDPC DECODER FOR IEEE 802.11N WITH CONTROL UNIT

The fully parallel architecture of decoder is modified with the help of FSM that uses Min-Sum algorithm to decode the frame received from AWGN affected channel is shown in "Fig.6" . It is also capable of correcting the corrupted frame i.e. if any of the location is affected during transmission. It is iterative in nature. LDPC are represented by a parity check matrix or H matrix. Each row of the matrix H is represented by a Check node update unit (row processing). Each column of matrix is represented by a Variable node update unit (column processing). Message passing method is used between nodes to correct errors.

A. DECODER

This block uses Min-sum algorithm to decode the frame received from AWGN affected channel. It is also capable of correcting the corrupted frame i.e. if any of the location is affected during transmission. If is asserted (i.e. logic '1') then it means that decoding is successful. If it is logic '0' then it means the received frame was corrupted and an iteration should be performed by message passing method to correct the error.

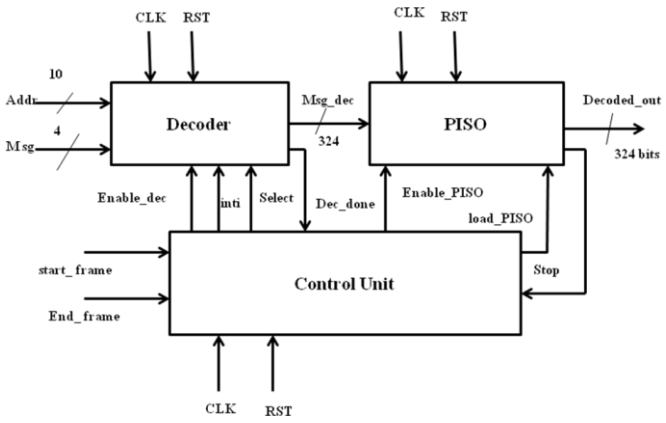


Fig. 6. Quasi Cyclic(QC)LDPC Decoder for IEEE 802.11n with control unit

B. CONTROL UNIT

This Control Unit used in the decoder is a Moore Finite State Machine with seven states to control unit which complete the decoding process. These seven states are wait_for_start, read_frame, decoding, check_iteration, iterate, load_PISO, enable_PISO.

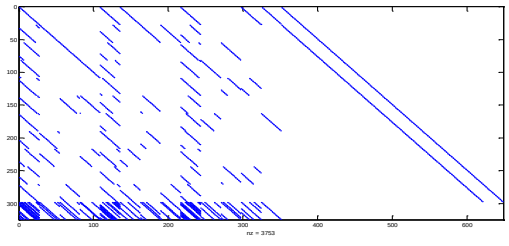
C. PARALLEL IN SERIAL OUT(PISO)

In this state, an enable_PISO signal is asserted to begin serial transmission of the decoded message[1:324] i.e. 1,2,3,4.....323,324. So PISO starts the serial transmission after receiving this enable_PISO signal. When the stop is acknowledged then it is confirmed that serial transmission of decoded message has ended.

VI. RESULT AND DISCUSSION

A. LOWER TRIANGULAR H MATRIX USED FOR QUASI CYCLIC(QC)- LDPC DECODER CODE IN IEEE 802.11N

The structured Parity Check Matrix for IEEE802.11n, N =648 bits, and R = ½ is formed by using an identity sub-matrix which is rotated by an amount specified by the shift matrix z=27 .The lower triangular H matrix using Matlab software is shown in "Fig.7 ".The H matrix dimension is H= (m x n)=324x648, Where gap matrix used is g=27 and a proposed lower triangular matrix is T= (m-g)x(m-g)=297x297.



.Fig. 7. Lower triangular H matrix used for Quasi Cyclic(QC)LDPC codes in IEEE 802.11n

D. FULLY PARALLEL QUASI CYCLIC(QC)-LDPC DECODER FOR IEEE 802.11N

A fully parallel decoder architecture for a Quasi Cyclic(QC)LDPC decoder for standard IEEE 802.11n for the code rate of ½ and the block length of 648 bits is synthesized on Xilinx Virtex-5 device. Table I shows the resources occupied by the fully parallel architecture of Quasi Cyclic(QC)LDPC decoder..

Table I : Resource consumption of Quasi Cyclic(QC)LDPC decoder for IEEE 802.11n

Design Summary				
		Total Used	***Total Available***	***Utilized***
Area	***No. of slice registers***	3140	207360	1%
	No. of slice Look Up Tables	51599	207360	24%
	Number of Fully used Look Up Tables –Flip Flop Pairs	969	53770	1%
Maximum. Frequency		69.06 MHz		
Throughput		82.24Mbps.		

Table II lists the Comparison of the existing Quasi Quasi Cyclic(QC)LDPC Decoders for wireless IEEE 802.11n application with proposed architecture.

Table II : Comparison of Quasi Cyclic(QC)LDPC Decoders for wireless IEEE 802.11n application.

Work	**Parity check matrix structure**	**Type of Architecture**			**Application standard**	**Decoding Algorithm**	**Code length**	**Code rate**	**Frequency**	**Throughput**	**Technology**
	QC/struct Non-struct	***Serial***	***Partial Parallel***	***Fully-Parallel***							
[19]	QC		√		CMMB standard	Layered Min-Sum Algorithm	9216	½ and 3/4	50MHz	90 Mb/s.	180mn CMOS
[20]	QC			√	IEEE802.16e	Min-Sum Algorithm	2304	1/2	950MHz	2.2Gbps	90nm CMOS
[23]	QC			√	WiMax	Min-Sum Algorithm	576	1/2	142 MHz	~11 Gbps	Virtex5 .
[21]	PEG	√			WiMax		2304	1/2	36MHz	232.5Mbps	Stratix 2
[24]	Hierarchical QC (HQC)				WiMax	Min-Sum Algorithm	2304	1/2	64MHz	44mbps	Virtex 2
[18]	QC			√	WiFi	Min-Sum Algorithm	648-1944	½ to 5/6	116MHz	617-1808Mbps	Virtex-4
[26]	QC			√	WiFi	Min-Sum Algorithm	1944	5/6	100MHz	37.5-281.15Mbps	Virtex-6
[25]	QC			√	WiFi	Min-Sum Algorithm	648	1/2	194MHz	76.60Mbps	Xilinx XC2VP30-7

[22]	QC		√		WiMax	Min-Sum Algorithm	2304	1/2	143M Hz	61Mbps	Virtex2
[Pro posed]	QC			√	WiFi	Min-Sum Algorithm	648	1/2	76.26 MHz	82.24Mbps	Virtex-5

B. QUASI CYCLIC(QC)- LDPC DECODER DECODER SYSTEM FOR IEEE 802.11N WITH CONTROL UNIT

The QC-LDPC decoder architecture with control unit of a the block length of 648 bits and a code rate of ½ for standard IEEE 802.11n. is synthesized on Xilinx Virtex-5, Virtex-6 and Altera's Cyclone IV, DE2-115 devices .The summary of resource consumption generated by the Xilinx and Altera's Synthesis tools is shown in Table III. The table contents display that hardware resources occupied by the Fully-parallel architecture of QC-LDPC decoder using MSA decoding algorithm are very less.

Table III: Resource consumption of QC- LDPC decoder for IEEE 802.11n with control unit

Design Summary				
		Virtex -5 XC5VLX330 TFF1738-2	***Virtex-6 6VLX760 FF1760-2***	***Cyclone IV, DE2-115***
Area	***Number of slice registers***	3139 out of 207360	7292 out of 948480	12437 out of 114480
	No. of slice Look Up Tables	51600 out of 207360	60851 out of 474240	113434 out of 117053
	Number of Fully used Look Up Tables –Flip Flop Pairs	969 out of 53422	3607 out of 62776	Not Applicable
Maximum Frequency		73.392 MHz	97.945 MHz	66.52 MHz
On Chip Power		3.486 W	4.448 W	3.021 W
Post Route Latency		38	38	38
Throughput		45 Gbps	51 Gbps	28 Gbps

VII. CONCLUSION & FUTURE WORK

In this paper, a fully parallel architecture of Quasi Cyclic(QC) LDPC decoder for IEEE 802.11n based on soft decision Min-Sum decoding algorithm is implemented. Various details like throughput and resource utilization have been documented .The Resource consumption in results shows that QC-LDPC decoder architecture has reduced complexity in terms of area. The work can be extended for other block length H matrix for IEEE 802.11n . Another change would be to optimize the system in terms of speed, size or power consumption. An irregular LDPC code can be also used for better error performance in advanced communication systems like OFDM, DVB-S2, IEEE 802.3 and Wi-Max.

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