

# Implementation of Quaternary Divider for Performance Optimization



Shweta Hajare, Monica Kalbande, Tejswini Panse, Pravin Dakhole

**Abstract:** In VLSI technology, designers concentrations is on area required and on performance of the device. In this design power consumption is one of the major concerns due to increase in chip density, continuous and decline in size of CMOS circuits and frequency at which circuits are operating. High-speed divider is an significant issue of high-speed computing. This paper presents quaternary division algorithm .This algorithm involves detect zero circuit designed with transmission gate. This proposed algorithm is faster than binary division algorithm as well as radix 4 SRT division algorithm in terms of speed & power. This type of fast divider can be used for the design of Arithmetic Logic unit.

**Keywords :** Quaternary transmission gate (T-gate), Quaternary Delta literal circuit, Quaternary detect zero circuit.

## I. INTRODUCTION

Divider is one of the important arithmetic blocks in many arithmetic application, a significant amount of energy is dissipated in division due its longer latency. For correct functioning longer latency is necessary. For achieving low-power dissipation, high reusability and reduced area of accessible building blocks the divider architecture is essential choice. For efficient processor design power, area and delay should be less. Division is always one of the most difficult operations in arithmetic and hence in VLSI architecture all the implementations of division algorithms required higher orders of time and space complexities. High speed of operation and circuit complexity in divider circuit corresponds to high power dissipation. In quaternary division ,division operation will takes place according to decimal division. A considerable amount of energy dissipated in division operation as compared to addition and multiplication. Division operation consist of two main component divisor and dividend. After division output is in

terms of quotient and remainder. The partial remainder need to check after each subtraction cycle, similar to multiplication, whether the resultant remainder is within the appropriate range also it has to be checked or if the remainder is negative or if is less than the divisor. Continuation of the

division process is done after checking these two conditions and further subtraction will be carried out.

In past in order to make division process more efficient various algorithms have been used, implemented such as SRT algorithm , Goldschmidt algorithm , restoring algorithm, non-restoring algorithm. For higher radix digit recurrence algorithm is implemented to reduce the iteration, which improves the latency. In SRT-based dividers difficulty of the quotient-digit range depends on operational speed. In structural level and algorithmic level, many division techniques had been developed to get better result in terms of reduction in latency of the divider circuitry by reducing the iteration [1]. Digital systems and calculators works on all arithmetic operations. Currently there is requirement of High speed methods of calculation. So the fast dividers design is an significant issue in high speed computing because for the total arithmetic operation division accounts for a significant fraction . Some authors reported work on radix 4 division such as Milos D. Ercegovic reported the architectures of division algorithms for radix 16 and radix 4 with the aim of reducing the delay of the quotient digit by flexibility in its computation and introducing more concurrency [2]. Tung N. Pham explored radix-4 SRT dividers with the choice of maximum redundancy . Using an ASIC flow and single, double and triple VT devices a highest redundancy divider is designed [3]. C.L.Wey reported a speedy radix-4 SRT division architecture which is an significant issue in high-speed computing [4].

This paper presents quaternary divider circuit designed with quaternary T-gate , quaternary delta literal circuit ,quaternary detect zero circuit. Result shows that area required in quaternary logic in terms of number of transistor and power is less as compared to binary and radix 4 divider circuit.

## II. DESIGN OF QUATERNARY VALUED LOGIC CIRCUIT

Quaternary valued logic is the type of multiple valued logic which offers all the benefit of MVL in terms of interconnection delay , power consumption and area [5]. Quaternary logic is four valued logic 0,1,2,3. In this paper these four logic levels are represented by 0v, 1v, 2v, 3v respectively [6].

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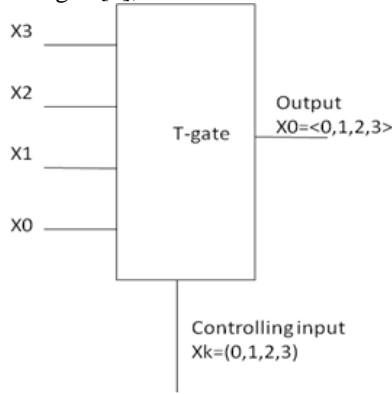
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**A.Design of Quaternary transmission gate (T-gate)**

Quaternary transmission gate (T-gate) is simply a multiplexer modified for multiple valued logic operations whose block diagram is shown in Fig.1. For quaternary valued system ,T gate has 5 inputs .

One of them is quaternary valued control input. The value of this variable decides which of the remaining quaternary valued inputs will be produced at the output [6].Depending upon the value of control input , corresponding input will be selected at the output. Fig.2 shows Gate level representation of transmission gate[7],



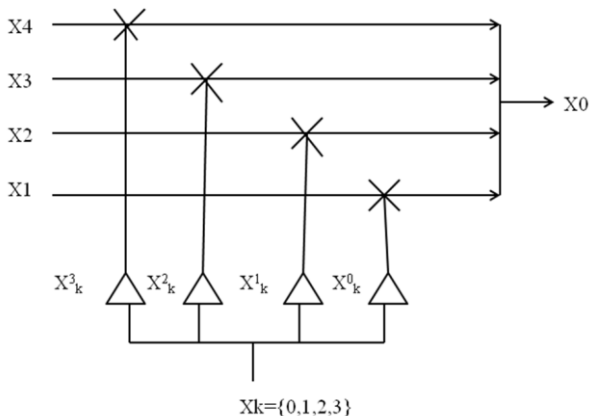
**Fig. 1.Block diagram of Quaternary transmission gate (T-gate)**

**Table- I: Quaternary system Delta Literal Truth Table**

Input	Output			
	$X^3_k$	$X^2_k$	$X^1_k$	$X^0_k$
0	3	0	0	0
1	0	3	0	0
2	0	0	3	0
3	0	0	0	3

**B.Design of Quaternary Delta Literal**

For providing controlling action Literals used in the representation. Respective input must be selected with appropriate control input .For quaternary system delta literal truth table is as shown in Table I.



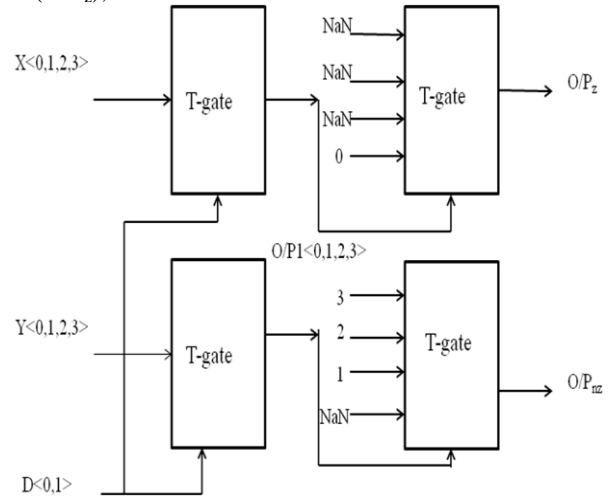
**Fig. 2.Gate level representation of T-gate**

**C.Design of Quaternary Detect Zero Circuit**

In division operation the number ‘zero’ is undesirable, which causes vague output when it's placed in the

denominator. As a result, a detect zero circuit is essential for each input before incoming the operation[11]. D is the selection input on which the operation of compact detect-zero circuit depends. If, the quaternary input X get selected then selection input D=0 and if the quaternary input Y get selected then selection input D=1,.

When X or Y inputs are given to T-gate 1 or T-gate 2, the O/P<sub>1</sub> is quaternary number has four states 0,1,2,3.T-gate 3 depends on O/P<sub>1</sub> and output from T-gate 3 is called output zero (O/P<sub>Z</sub>),



**Fig. 3.Detect zero circuit**

O/P<sub>Z</sub> is zero if O/P<sub>1</sub> equal to zero moreover, O/P<sub>Z</sub> is NaN. T-gate 4 depends on O/P<sub>2</sub> and called as output non zero (O/P<sub>nz</sub>), , O/P<sub>nz</sub> is NaN if O/P<sub>2</sub> equal to zero else, O/P<sub>Z</sub> is <123>. T In the mathematical expression the operator ^ is QMIN operation. QMIN operation is similar to binary AND gate .This is mathematically expressed as follows :

$$O/P_1 = (A \wedge D^{<30>}) + (B \wedge D^{<03>}) \tag{1}$$

$$O/P_Z = (0 \wedge O/P_1^{<3000>}) + (NaN \wedge O/P_1^{<0300>}) + (NaN \wedge O/P_1^{<0030>}) + (NaN \wedge O/P_1^{<0003>}) \tag{2}$$

$$O/P_{nz} = (NaN \wedge O/P_1^{<3000>}) + (1 \wedge O/P_1^{<0300>}) + (2 \wedge O/P_1^{<0030>}) + (3 \wedge O/P_1^{<0003>}) \tag{3}$$

**Table- II: Detect Zero Circuit Truth Table**

X	O/P1	O/P <sub>Z</sub>	O/P <sub>nz</sub>
0	0	0	NaN
1	1	NaN	1
2	2	NaN	2
3	3	NaN	3

**III. DESIGN OF QUATERNARY DIVIDER CIRCUIT**

Quaternary divider circuit consist of detect zero circuit and quaternary t-gate structure. In quaternary division if zero comes in the denominator, result is undefined & one can not implement the circuit so the detect zero circuit is introduced before the input.



For getting the quotient & remainder modulo 4 operation is done[9].

Mathematical expression of Quaternary Divider circuit is as follows

$$O/P_1 = (Z_0 \wedge X^{<300>}) + (Z_1 \wedge X^{<030>}) + (Z_1 \wedge X^{<003>}) \tag{4}$$

$$O/P_2 = (Z_0 \wedge X^{<300>}) + (Z_0 \wedge X^{<030>}) + (Z_1 \wedge X^{<003>}) \tag{5}$$

$$O/P_3 = (Z_0 \wedge X^{<300>}) + (Z_0 \wedge X^{<030>}) + (Z_0 \wedge X^{<003>}) \tag{6}$$

$$O/P_4 = (Z_2 \wedge X^{<300>}) + (Z_0 \wedge X^{<030>}) + (Z_1 \wedge X^{<003>}) \tag{7}$$

$$O/P_5 = (Z_3 \wedge X^{<300>}) + (Z_2 \wedge X^{<030>}) + (Z_0 \wedge X^{<003>}) \tag{8}$$

$$O/P_6 = (X \wedge Y^{<300>}) + (O/P_1 \wedge Y^{<030>}) + (O/P_2 \wedge Y^{<003>}) \tag{9}$$

$$O/P_7 = (O/P_3 \wedge Y^{<300>}) + (O/P_4 \wedge Y^{<030>}) + (O/P_5 \wedge Y^{<003>}) \tag{10}$$

Here NaN refer to not a number[8]

From these output expression quotient and remainder expression is as follows

$$Q = (O/P_6 \wedge D_1^{<300>}) + (Z_0 \wedge D_1^{<030>}) + (NaN \wedge D_1^{<003>}) \tag{11}$$

$$R = (O/P_7 \wedge D_1^{<300>}) + (NaN \wedge D_1^{<030>}) + (Z_0 \wedge D_1^{<003>}) \tag{12}$$

Fig. 5 and Fig.6 shows Comparative analysis of Quaternary divider in terms of area and Power .

Table- III: Quaternary divider Truth Table

X/Y	1	2	3
Quotient(Q)			
1	1	0	0
2	2	1	0
3	3	1	1
Reminder(R)			
1	0	2	3
2	0	0	2
3	0	1	0

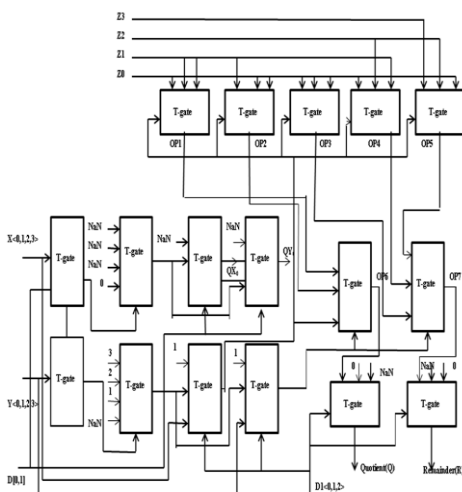


Fig. 4. Quaternary divider circuit

#### IV. RESULT

This paper proposed quaternary divider algorithm. Simulation of quaternary divider circuits is done using Tanner EDA tool with 180nm technology. The performance parameter of the Quaternary divider circuit is compared with radix-4 SRT & binary divider in terms of transistor count and power consumption. From the simulated results it is observed that as compared to radix-4 SRT & binary divider proposed quaternary divider is fast , its power consumption is less and area required is also less .

#### V. CONCLUSION & FUTURE WORK

This paper presents quaternary division algorithm. The design of quaternary division algorithm is based on Tgate and detect zero circuit. By using Detect zero circuit quaternary divider circuit is designed. The proposed quaternary divider circuit required 35% less number of transistor as compared to Radix 4 SRT divider circuit and 8.5% less number of transistor as compared to binary divider circuit[10]. In terms of power consumed by quaternary divider circuit is 30% less as compared to radix 4 SRT divider and 80% less as compared to binary divider circuit. So Quaternary divider is better as compared to binary and radix 4 SRT divider circuit. In future such type of quaternary divider circuit can be used for the designing of arithmetic logic unit.

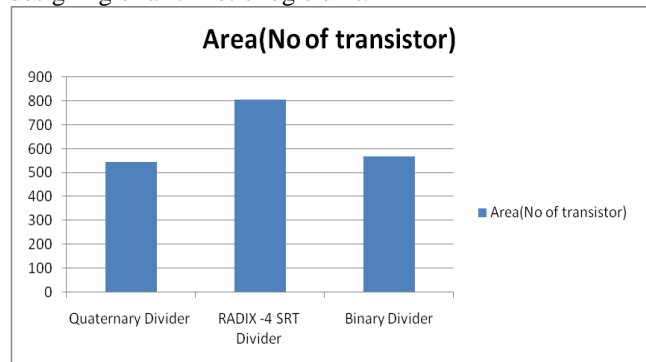


Fig.5 Comparative analysis of Quaternary divider in terms of area

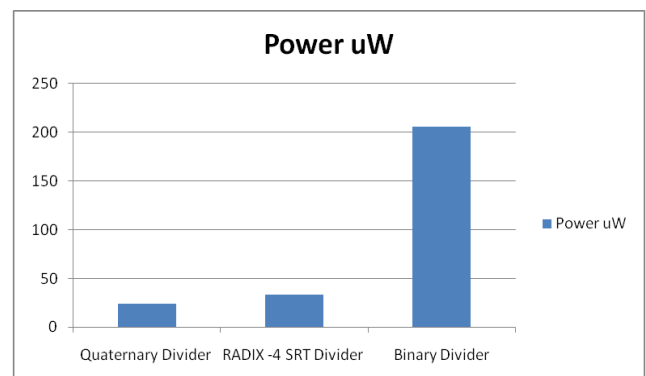


Fig. 6 Comparative analysis of Quaternary divider in terms of Power

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