# Design of Low Power Multiplexer and De-Multiplexer using Different Adiabatic Logics

**M. Swathi, A.V.N.S Lasya Priya, Lokesh Pudari, Kura Karthik**

***Abstract:*** ***In this paper we proposed, design and evaluation of 16:1 Multiplexer and 1:16 Demultiplexer using different adiabatic logics. Power consumption is the main factor in VLSI digital circuit design. Here we have introduced a CMOS-logic based 16:1 Multiplexer and 1:16 De-multiplexer with a low power adiabatic logic. In which we concentrate on the characteristics of the CMOS and adiabatic logics such as 2N2P, 2N-2N2P and Dual sleep. Wherein both 2N2P and 2N2N2P use a cross-coupled transistor structure for adiabatic operation. Adiabatic logic circuits use reverse logic and the power dissipation will be less compared to the CMOS circuits as the inputs are given to the n-type functional tree in 2N2P and 2N2N2P. For dual sleep logic an additional circuit is connected in series with general CMOS circuit known as sleep circuit. we have concentrated on energy recovery and power dissipation, as all these technique results in the low power dissipation. Dualsleep is considered as the best of the all the other adiabatic and traditional logics.***

***Keywords*****:** ***Low Power Dissipation, Energy Recovery, 2N2N2P Logic, 2N2P Logic, Dualsleep Logic.***

## I. INTRODUCTION

Multiplexer is a combinational circuit that gives single output using selection lines and accepts multiple inputs, multiplexer is also known as data selector. A multiplexer will have $2^n$ inputs has n select lines, which are used to select the input line to send to the output [1]. An electronic multiplexer makes multiple inputs into one output of the system or resource, for example, a converter or one communication line, which having one line for one signal, the multiplexer can sort it out. Similarly, this operation can be used in reverse order where one put to multiple outputs, a Demultiplexer is a device which takes one input and results in multiple outputs, which is selected using the selections lines. A multiplexer is usually used an inverted Demultiplexer at the end of the circuit. CMOS circuit consist of pull-up network and pull-down network in which the output depends on PMOS transistors i.e. pull-up network but in 2N2P and 2N2N2P logics the output depends on the pull-down network of the CMOS multiplexer and demultiplexer. Hence, CMOS multiplexer and demultiplexer dissipates more power so, to overcome that we are using adiabatic logic circuits. In this paper we are proposing 16:1 multiplexer and 1:16 demultiplexer using 2:1 and 1:2 multiplexers and de-multiplexer respectively. The equation of multiplexer is *Y=AS+BS.* The results of each logic are compared with the CMOS logic circuit.

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## II. ADIABATIC LOGICS

Adiabatic logic follows reverse logic. It follows two rules to reduce power dissipation i.e. Transistor will never get turned on where the voltage is between source and drain. And another point Transistor is never turned off where current is present in it. The adiabatic logics [2] used in this paper are 2N2P, 2N2N2P and Dualsleep logic.

### A. 2N2P Logic

The name 2N2P indicates that it is a combination of two P-MOSFETS and two N-type functional trees. As shown in fig.1 the input is given to the functional tree and inverted functional tree, the drains of the functional trees are connected to the input of PMOS in a cross coupled manner. Which results in the on/off state of P-MOSFETS. An AC power supply *VDD* is used for 2N2P gates, so as to recover and reuse the supplied energy.

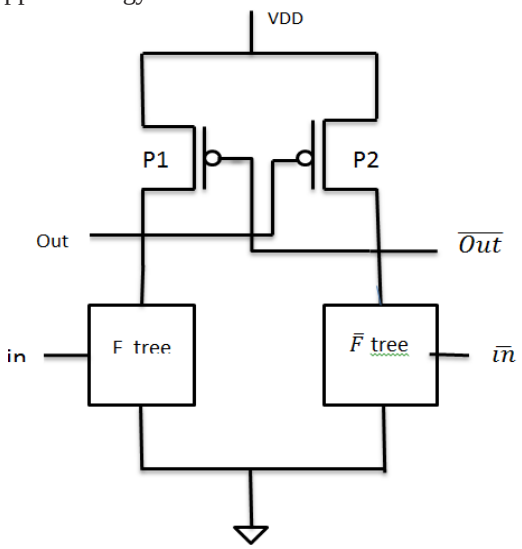


**Fig: 1 2N2P Logic Block Diagram**

The output of out is fully inverted because of the cross coupled transistors, the circuits suffer from non-adiabatic loss both in precharge and recover phase. By the input combination, the cross coupled is turned off and on. When functional tree is on then the connection between the ground and input of PMOS is connected which results in the on condition of PMOS then the 'Logic 1' is obtained at the output [5]. A major disadvantage of this circuit is the coupling effects, because the two outputs are connected by the PMOS latch which makes both outputs interfere each other.

### B. 2N2N2P Logic

2N2N2P Logic mainly derived from 2N2P logic to reduce coupling effect which belongs to the quasi-adiabatic logic family. Its main problem over 2N2P is the cross coupled nature of N-MOSFET switches which results in to non-floating outputs for the recovery phase. An update version of the 2N2P logic is 2N2N2P logic with the only difference that it has extra two NMOS transistors which are connected in series with PMOSFETs. Where, the cross coupled PMOS transistors common to both the logics [4]. 2N2N2P logic looks similar to SRAM cell which has a cross coupled full inverter.

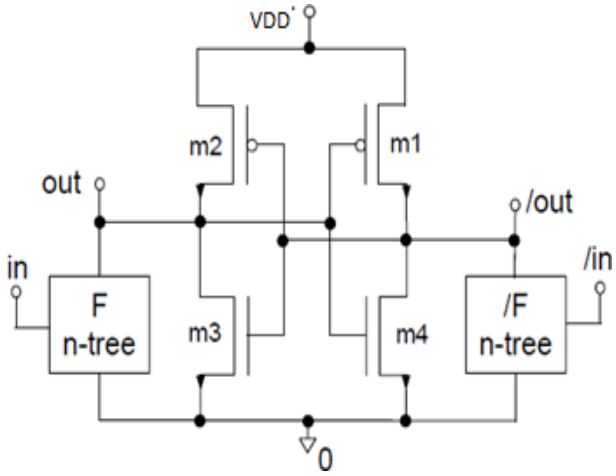


**Fig: 2 2N2N2P Logic Block Diagram**

In this logic as shown in fig.2 there are 2PMOS and 2NMOS functional trees. Here, 2PMOS and functional trees are connected parallel to the transistors which are connected in series with the 2PMOS transistors. In this a cross coupled connection is established between the PMOS and parallelly connected pull-down network. Functional tree is the pull-down network of a circuit, here we consider the pull-down network of CMOS Multiplexer and Demultiplexer [5]. The left functional tree and right functional tree are inverted to each other. In which this network turns on the PMOS transistors by the 'Reverse Logic'. The input of these functional trees is also inverted with respect to the functional tree type.

### C. Dualsleep Logic

In this logic as shown in fig.3 there is an additional circuit which make the circuit on and off, the additional circuit with respect to the normal CMOS Multiplexer and Demultiplexer is the sleep circuit [6]. Sleep circuit is the combination of PMOS and NMOS which are connected in parallel whose inputs are shorted together, for CMOS multiplexer and demultiplexer this sleep circuit is connected in series. In Dual Sleep two extra sleep circuits are used which are placed/connected near the VCC and ground. These circuit consist on one PMOS transistor and one NMOS transistor, this circuit is called as sleep circuit because at a time on of the circuit goes with respect to the inputs of SLEEP_N and SLEEP_P. The Dual sleep logic has the two extra circuits which one in connected between the pullup network and VDD and other circuit is connected between the pulldown network and GND. Here, the operation of Dualsleep is that when SLEEP_P is ON [7] then automatically the SLEEP_N goes to off state and vice versa, which makes the half of the circuit off and other half in ON state, this results in less power dissipation.

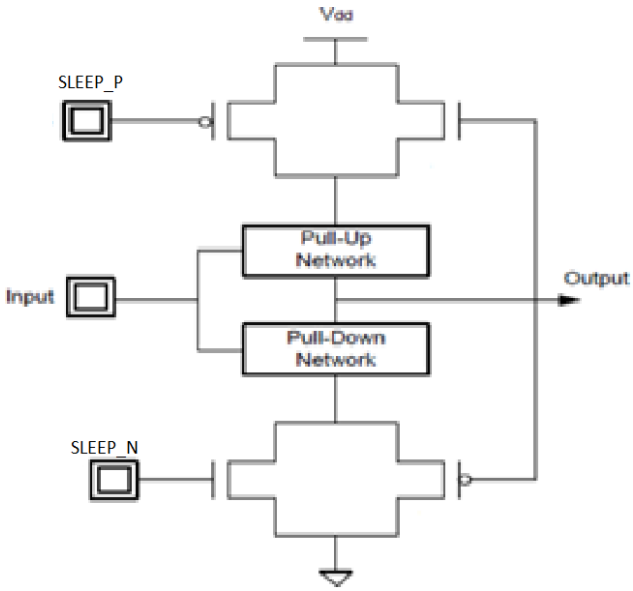


**Fig: 3 Dualsleep Logic Block Diagram**

## III. IMPLEMENTATION

### A. Conventional CMOS 2:1 Multiplexer

The implementation of this circuit is based on the equation $Y=\overline{A}S+BS$ as shown in fig.4. The output of 2:1 multiplexer is based on the selection line. When the selection line S=0 the output is observed as A and when S=1 the output is observed as B. The CMOS multiplexer consumes more power as there

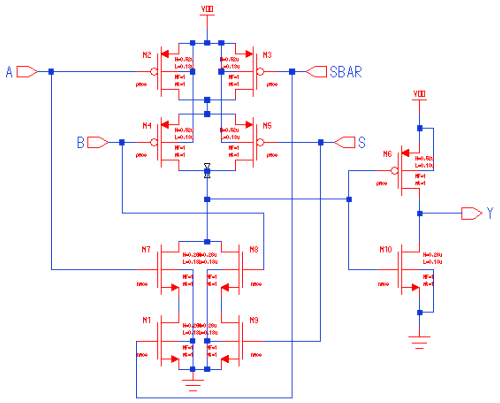


**Fig: 4 CMOS 2:1 Multiplexer Schematic**

are a greater number of P-MOSFETs, where the P-MOSFETs width is four times the length i.e. ratio 1:4 size of length and width respectively. So, the power dissipation of CMOS circuit is basically high comparing with adiabatic logic where most of the transistors are N-MOSFETs whose length to width ratio is 1:2. By observing these factors we can say that the adiabatic circuits use low power comparing to the CMOS.

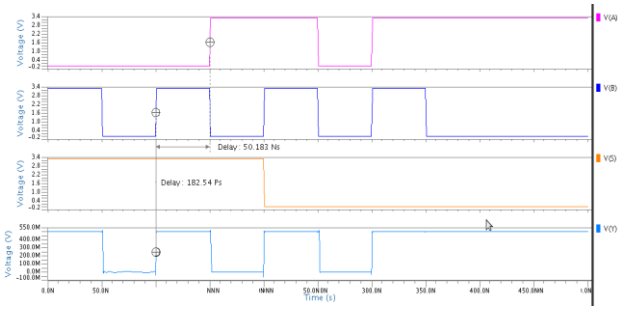

**Fig: 5 CMOS 2:1 Multiplexer Waveform**

From fig.5 we observing the waveforms, we can conclude that A is on while S=0 and B is on when for S=1 where the input pattern of A is 00011011, B is 10101010, S=11110000 and the output pattern is Y=10101011.

### B. Adiabatic logic 2N2P 2:1 Multiplexer

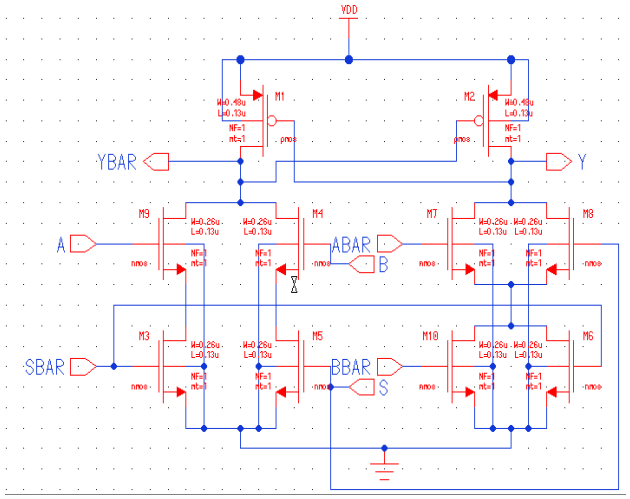


**Fig: 6 2N2P 2:1 Multiplexer Schematic**

The 2N2P logic is the adiabatic logic whose transistors are cross coupled each other and the functional trees are connected in series with the P-MOSFETs i.e. F and F are given the input and input respectively. Here there are only two P-MOSFETs comparing to the CMOS circuit and the remaining circuit are all the N-MOSFETs where the length

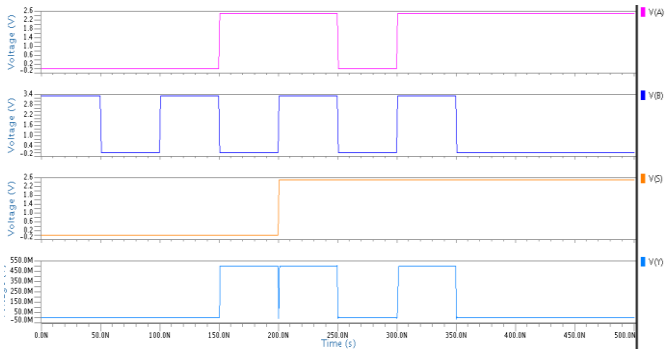

**Fig: 7 2N2P 2:1 Multiplexer Waveform**

and width of circuit is decreased which resultant in the low power dissipation circuit. In this adiabatic logic we get both inverting and non-inverting outputs. After constructing the circuit, the circuit is evaluated by giving different patterns of input. Where the functional tree makes the P-MOSFETs on and off according to the input pattern.

From fig.7 the inputs are taken in the form of pattern A=00011011, B=10101010, S=00001111 and output resultant is observed as Y=0001101.

### C. Adiabatic logic 2N2N2P 2:1 Multiplexer

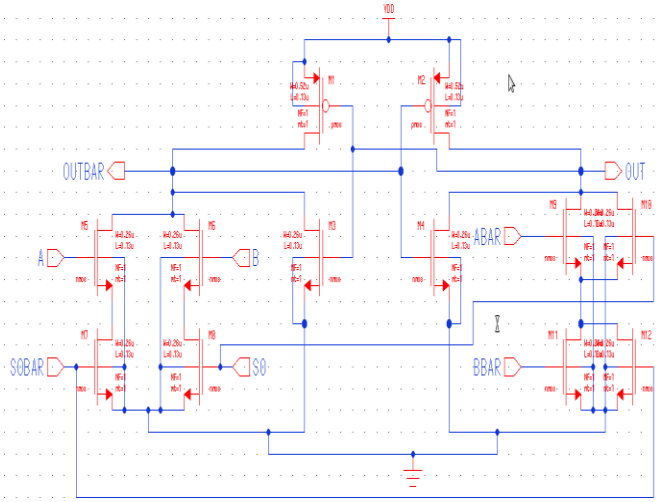


**Fig: 8 2N2N2P 2:1 Multiplexer Schematic**

As the logic diagram of 2N2N2P is derived from 2N2P logic which represents that two more N-MOSFETs are connected in series with the pull-up network P-MOSFETs, where the n-type functional trees are connected in parallel with the N-MOSFETs. The cross coupled nature of these adiabatic logic makes on and off using the inverting and non-inverting inputs of the functional trees. The 2N2N2P is the updated version of 2N2P as the coupling effect is high by the advancement of 2N2P which results in decrease of coupling effect. But as the number of transistors increase the area also increases. So, the power dissipation also increases comparing to the CMOS multiplexer.

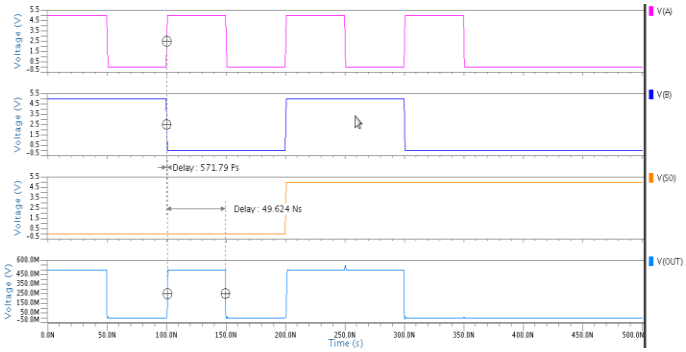

**Fig: 9 2N2N2P 2:1 Multiplexer Waveform**

From fig.9 the inputs are taken in the form of pattern A=10101010, B=11001100, S=00001111 and output resultant is observed as Y=10101100.

### D. Adiabatic logic Dualsleep 2:1 Multiplexer

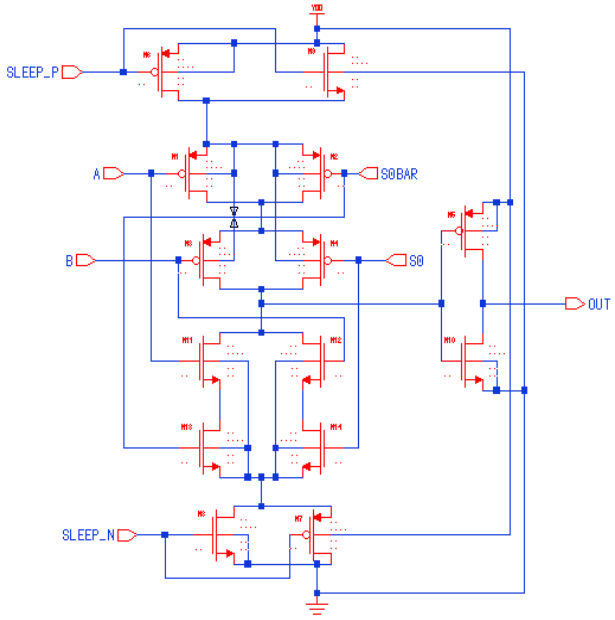


**Fig: 10 Dualsleep 2:1 Multiplexer Schematic**

The multiplexer is designed using the adiabatic Dualsleep logic diagram where the traditional CMOS multiplexer is placed in between the sleep circuits.

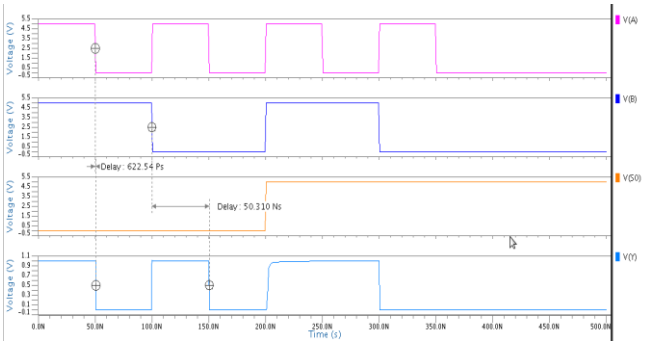


**Fig: 11 Dualsleep 2:1 Multiplexer Waveform**

From fig.11 the inputs are taken in the form of pattern A=10101010, B=11001100, S=00001111 and output resultant is observed as Y=10101100.

### E. Conventional 1:2 CMOS De-multiplexer

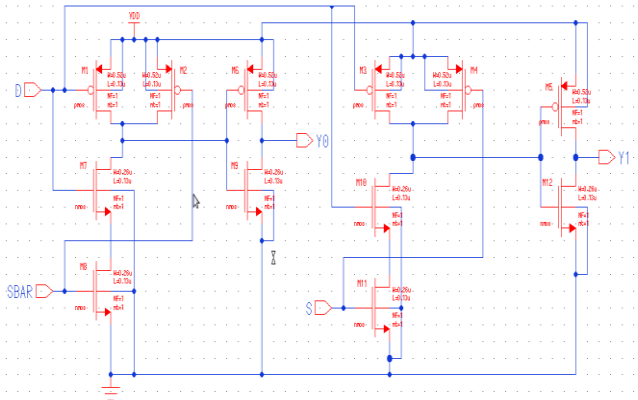


**Fig: 12 CMOS 1:2 Demultiplexer Schematic**

The traditional CMOS demultiplexer is the combination of two circuits where each circuit gives one output. The data D is the common input for both the circuits.

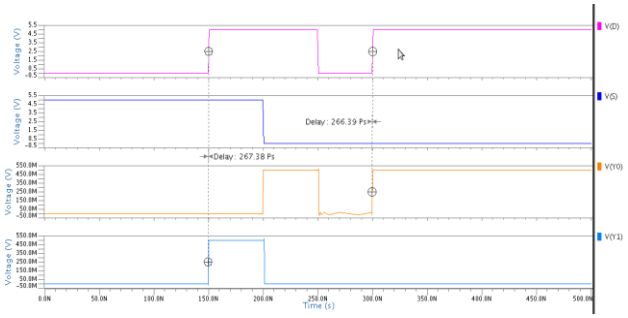


**Fig: 13 CMOS 1:2 Demultiplexer Waveform**

From fig.13 the inputs are taken in the form of pattern A=10101010, B=11001100, S=00001111 and output resultant is observed as Y=10101100.

### F. Adiabatic logic 2N2P De-multiplexer

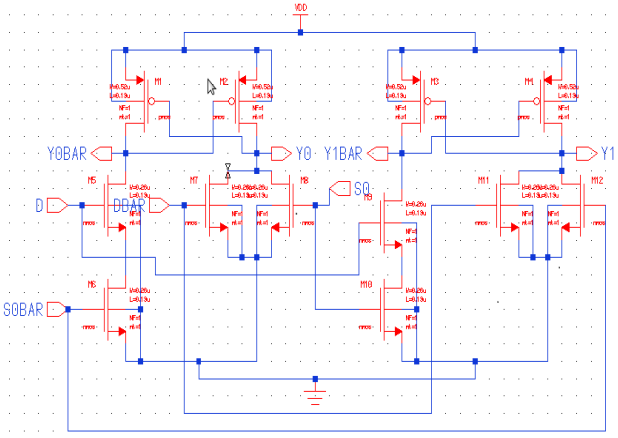


**Fig: 14 2N2P 1:2 Demultiplexer Schematic**

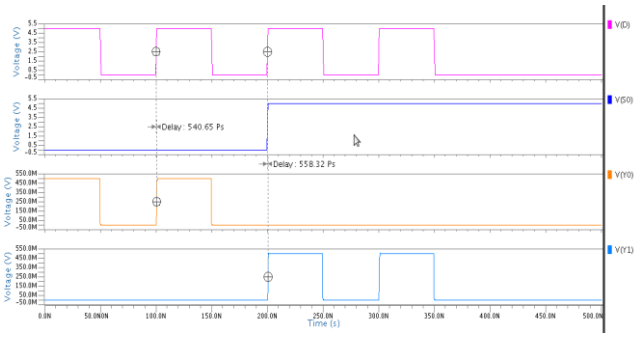


**Fig: 15 2N2P 1:2 Demultiplexer Waveform**

From fig.15 the input pattern D=10101010, $S_0$=00001111 and output resultant is observed as $Y_0$=10100000 and $Y_1$=00001010.

### G. Adiabatic logic 2N2N2P De-multiplexer

The Demultiplexer is designed using the adiabatic 2N2N2P logic diagram, where the traditional CMOS multiplexer pull-down network is used as functional tree.

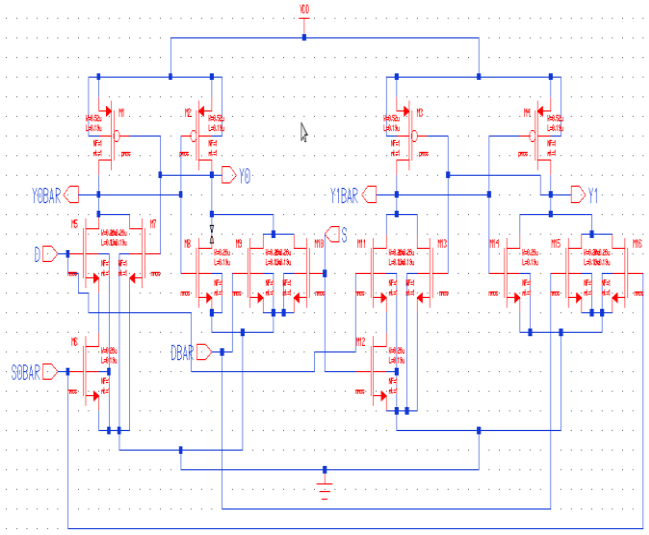


**Fig: 16 2N2N2P 1:2 Demultiplexer Schematic**

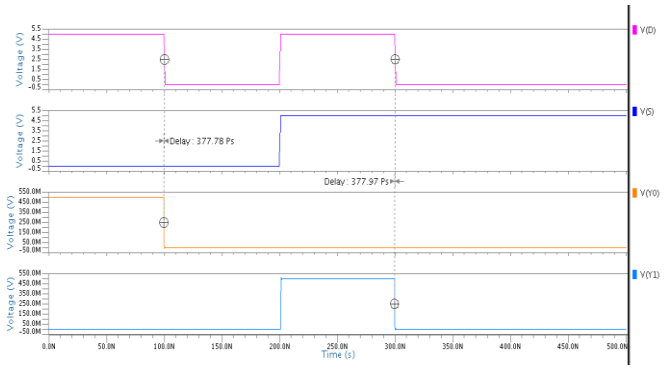


**Fig: 17 2N2N2P 1:2 Demultiplexer Waveform**

From fig.17 the input pattern D=11001100, $S_0$=00001111 and output resultant is observed as $Y_0$=11000000 and $Y_1$=00001100.

### H. Adiabatic logic Dual sleep De-multiplexer

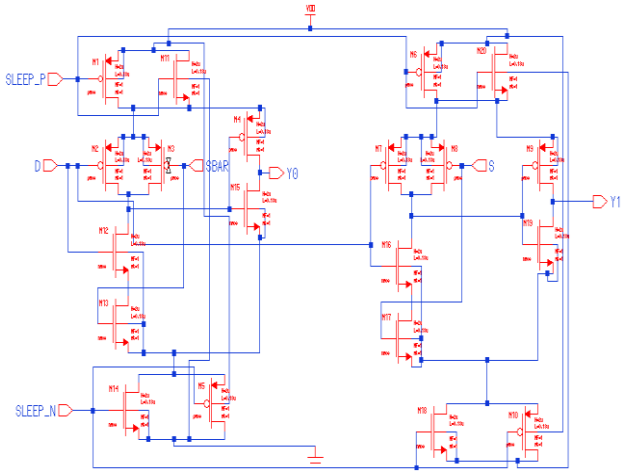


**Fig: 18 Dualsleep 1:2 Demultiplexer Schematic**

The multiplexer is designed using the adiabatic Dualsleep logic diagram where the traditional CMOS multiplexer is placed in between the sleep circuits.

From fig.19 the input pattern D=10101010, $S_0$=00001111 and output resultant is observed as $Y_0$=10100000 and $Y_1$=00001010.

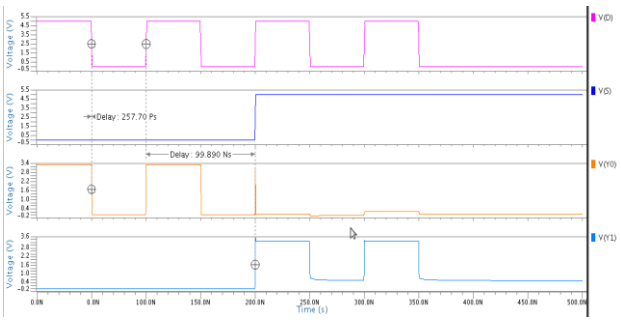


**Fig: 19 Dualsleep 1:2 Demultiplexer Waveform**

### I. Conventional 16:1 CMOS Multiplexer

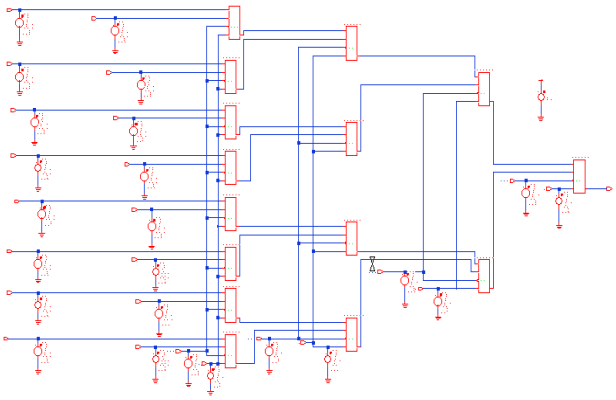

**Fig: 20 CMOS 16:1 Multiplex Schematic**

To build 16:1 multiplexer, we used fifteen traditional CMOS 2:1 multiplexer which are placed according to the logic of multiplexer where four selection lines are used to get the desired output.

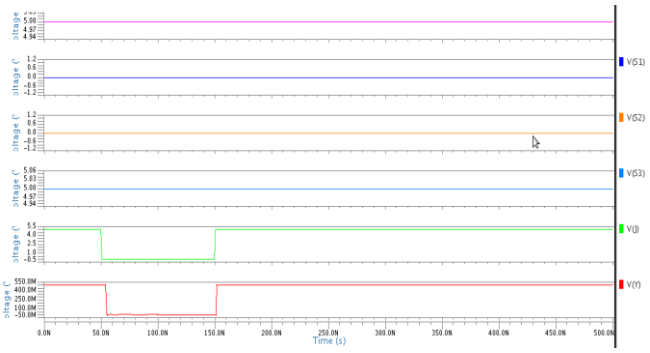


**Fig: 21 CMOS 16:1 Multiplexer Waveform**

From fig.21 the inputs are taken in the form of pattern S3=1, S2=0, S1=0, S0=1 and output resultant is observed in accordance with input is Y=J (1001).

### J. 16:1 2N2P Multiplexer

To construct 16:1 2N2P multiplexer, we used fifteen 2N2P 2:1 multiplexer which are placed according to the logic of multiplexer where four selection lines are used to get the desired output.

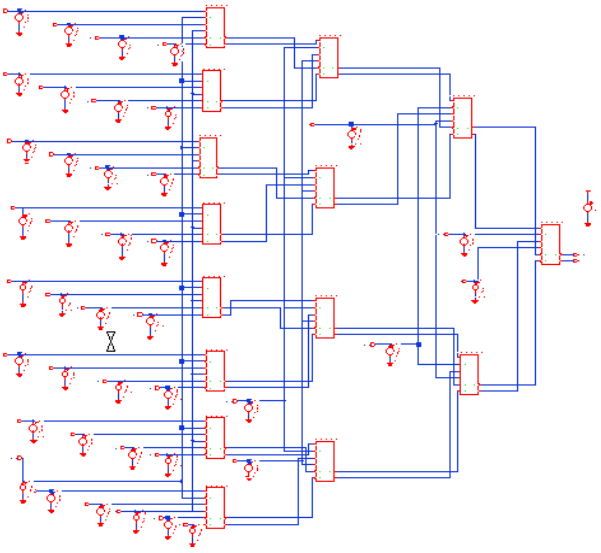

**Fig: 22 2N2P 16:1 Multiplexer Schematic**

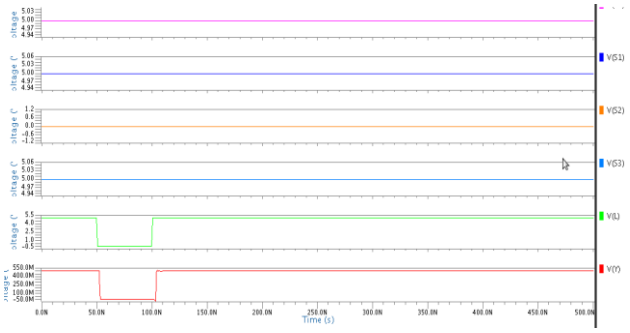

**Fig: 23 2N2P 16:1 Multiplexer Waveform**

From fig.23 the inputs are taken in the form of pattern S3=1, S2=1, S1=0, S0=1 and output resultant is observed in accordance with input is Y=L (1011).

### K. 2N2P16:1 Multiplexer

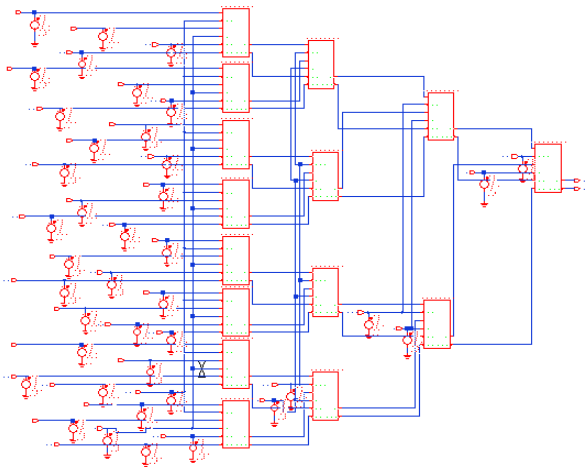

**Fig: 24 2N2P 16:1 Multiplexer Schematic**

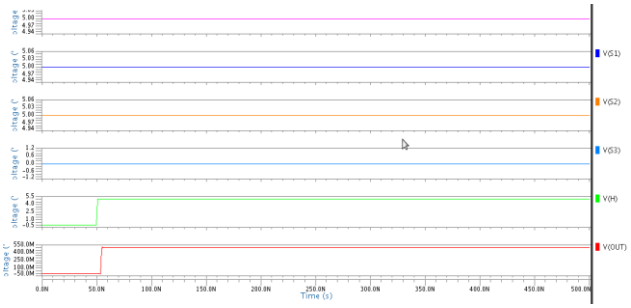

**Fig: 25 2N2P 16:1 Multiplexer Waveform**

The 16:1 2N2N2P multiplexer is the combination of fifteen 2N2N2P 2:1 multiplexer which are placed according to the logic of multiplexer where four selection lines are used to get the desired output.

### L. Dualsleep 16:1 Multiplexer

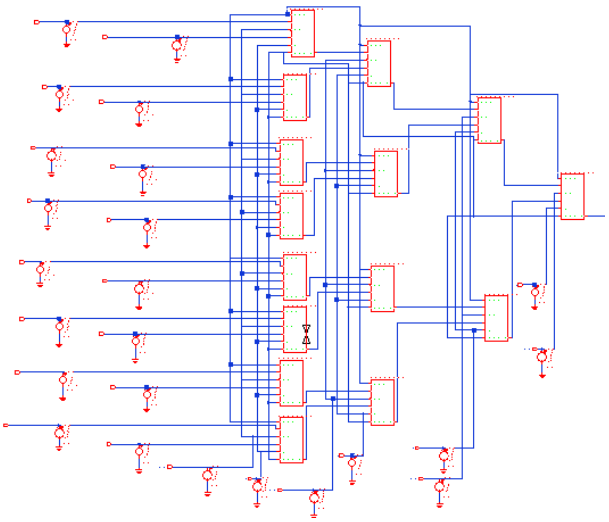

**Fig: 26 Dualsleep 16:1 Multiplexer Schematic**

To construct 16:1 Dualsleep multiplexer, we used fifteen Dualsleep 2:1 multiplexer which are placed according to the logic of multiplexer where four selection lines are used to get the desired output.

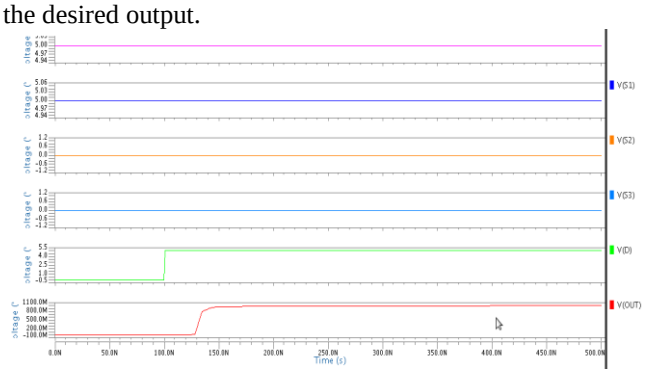

**Fig: 27 Dualsleep 16:1 Multiplexer Waveform**

As shown in fig.27 the inputs are taken in the form of pattern S3=0, S2=0, S1=1, S0=1 and output resultant is observed in accordance with input is Y=D (0011).

### M. 1:16 CMOS Demultiplexer

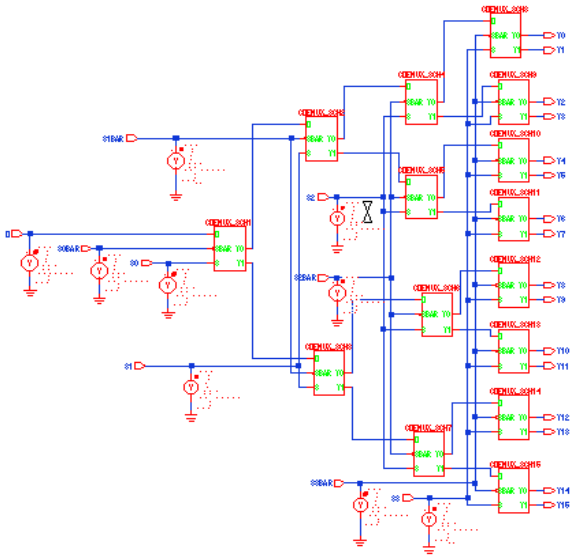

**Fig: 28 CMOS 1:16 Demultiplexer Schematic**

To build 1:16 Demultiplexer, we used fifteen traditional CMOS 1:2 Demultiplexer which are placed according to the logic of demultiplexer where four selection lines are used to get the desired output.

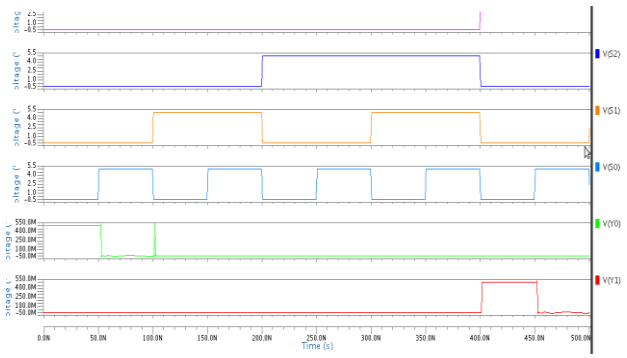

**Fig: 29 CMOS 1:16 Demultiplexer Waveform**

In demultiplexer, we get multiple outputs for single input. So, the output is of all 16 combinations i.e. 0000 to 1111.

### N. 1: 16 2N2P Demultiplexer

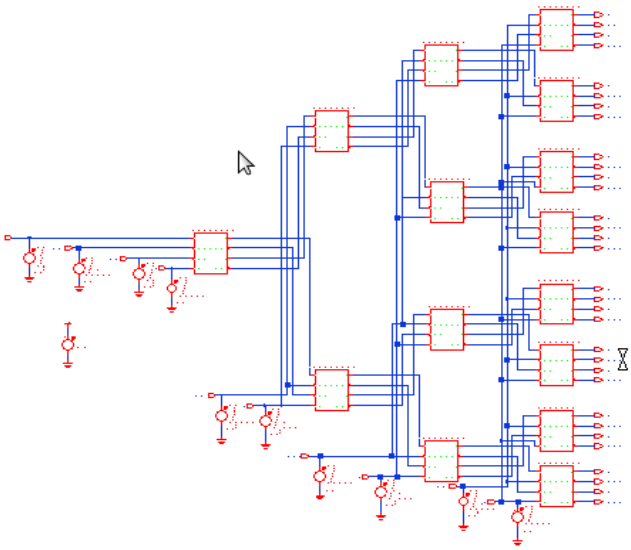

**Fig: 30 2N2P 1:16 Demultiplexer Schematic**

To build 1:16 2N2P Demultiplexer, we used fifteen 2N2P 1:2 Demultiplexer which are placed according to the logic of demultiplexer where four selection lines are used to get the desired output.

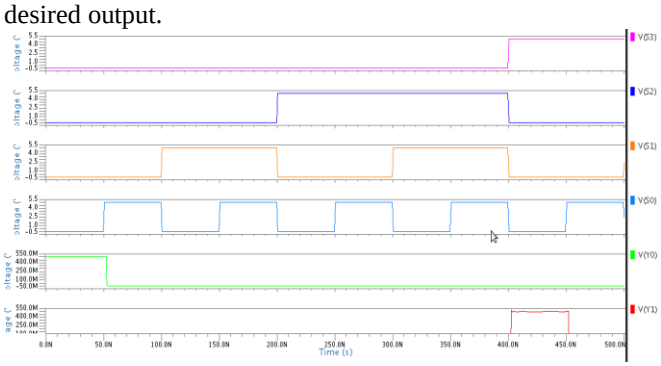

**Fig: 31 2N2P 1:16 Demultiplexer Waveform**

### O. 1:16 2N2N2P Demultiplexer

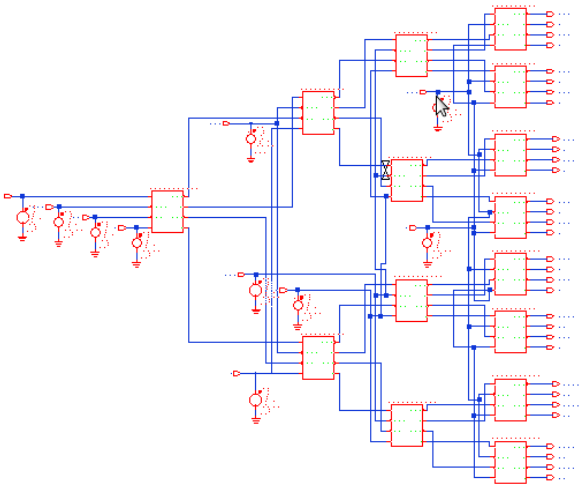

**Fig: 32 2N2N2P 1:16 Demultiplexer Schematic**

To construct 1:16 2N2N2P Demultiplexer, we used fifteen 2N2N2P 1:2 Demultiplexer which are placed according to the logic of demultiplexer where four selection lines are used to get the desired output.

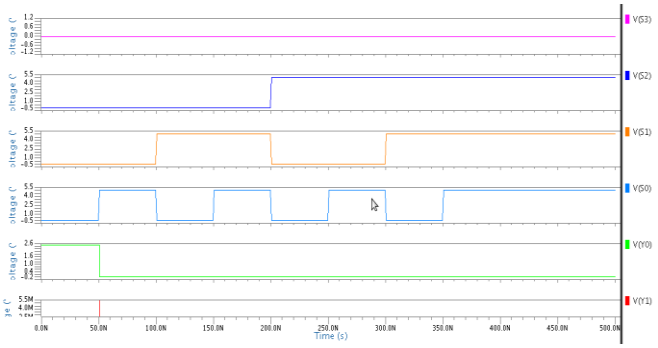

**Fig: 33 2N2N2P 1:16 Demultiplexer Waveform**

In demultiplexer, as shown in fig 32 and 33 we get multiple outputs for single input. So, the output is of all 16 combinations i.e. 0000 to 1111.

### P. 1:16 Dualsleep Demultiplexer

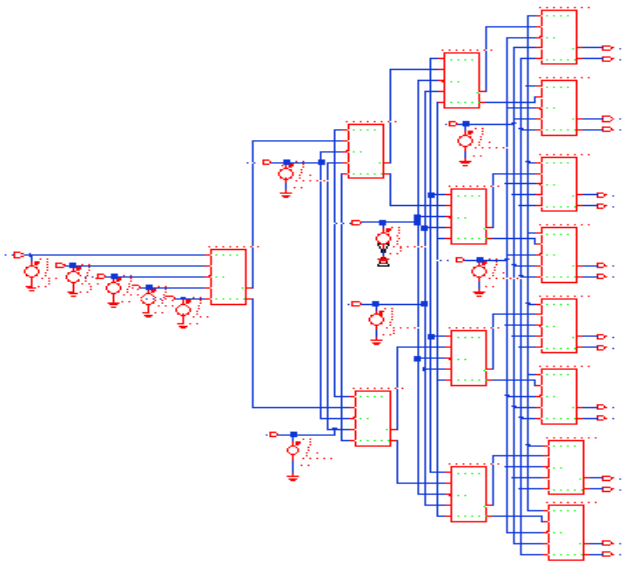

**Fig: 34 Dualsleep 1:16 Demultiplexer Schematic**

To build 1:16 Dualsleep Demultiplexer, we used fifteen Dualsleep 1:2 Demultiplexer which are placed according to the logic of demultiplexer where four selection lines are used to get the desired output.

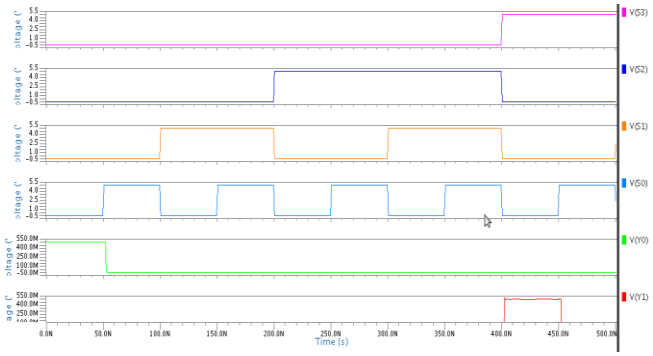

**Fig: 35 Dualsleep 1:16 Demultiplexer Waveform**

## IV. RESULT

The equation of Multiplexer is $Y=A\bar{S}+BS$ and equation of Demultiplexer is $Y0=DS$ and $Y1=DS$ where 'S' is the selection line. For the following equation the truth table for multiplexer and demultiplexer is

**Table 1. Multiplexer truth table**

| S | A | B | Y |
|---|---|---|---|
| 0 | 1 | X | 1(A) |
| 1 | X | 1 | 1(B) |

**Table 2. Demultiplexer truth table**

| S | D | Y |
|---|---|---|
| 0 | 1 | Y0 |
| 1 | 1 | Y1 |

## V. RESULT

The following result is for 2:1 multiplexer and 1:2 Demultiplexer.

| Logic | Power Dissipation (Multiplexer) | Power Dissipation (Demultiplexer) |
|---|---|---|
| CMOS | 426.9916pW | 1.7011nW |
| 2N2N2P | 1.3041nW | 2.1807nW |
| 2N2P | 876.8084pW | 1.3287nW |
| Dualsleep | 270.4738pW | 880.5749pW |

For 16:1 multiplexer and 1:16 Demultiplexer we get,

| Logic | Power Dissipation (Multiplexer) | Power Dissipation (Demultiplexer) |
|---|---|---|
| CMOS | 7.8653nW | 10.6211nW |
| 2N2N2P | 17.7401nW | 25.1275nW |
| 2N2P | 11.3671nW | 12.3476nW |
| Dualsleep | 4.450nW | 6.9137nW |

## VI. CONCLUSION

As we observe the above tables, the power dissipation of adiabatic logic less than the traditional CMOS logic circuit. The dual sleep logic is the best in adiabatic logic, where the power dissipation is very less compared with the other adiabatic logic and CMOS logic. Even though the number of transistors is more the power consumption is less because of the sleep circuit technique. So, Adiabatic dual sleep logic technique is more efficient technique than remaining techniques. The 16:1 multiplexer and 1:16 de-multiplexer are designed in CMOS logic as well as in all the adiabatic logic.

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