Optimization Method for Delay and Power Using Enhanced CSS FLIP FLOP with 24 Transistors

G. Ravi kishore, N. M. Nandhitha

Abstract: ***New way optimization method is an Enhanced CSS F^{2}A new method titled in this paper to explain the improved flip flop design with 24 transistor's using circuit-shared static flip-flop (ECSSFlip Flop).this implementation enhances power and delay where we utilize 5 NOR gates and 2 INV's(inverters), these methods are these methods are utilized in the quality cell libraries, The ECSS FLIP FLOP utilizes a positive intercessor clock signal, it is produced from a main clock, to require information into a main latch and a negative fringe of the foundation clock to carry the info during a gated latch. Cadence(Virtuoso) simulations at 180-µm found optimized at different frequency now the ability by a power dissipation of 9.516nW and delay by 3.634 ns in comparison to CSS FLIP FLOP***

Keyword's: ECSS FLIP FLOP, FLIP FLOP (F^2), Power, Delay, gate

I. INTRODUCTION

In digital VLSI circuits the efficiency of both power & delay has become the bottleneck and tougher. advanced technology needs a great implementation, over a decade CMOS technology has showed advancement in reducing the power & delay in IC designs. Digital logic design implementations with universal gates or logic gates improved the functionality of many circuits to optimize the power dissipation or delay of the proposed circuit. Now the enhancement made with a concept of how to approach a new way with low power & frequency techniques with decreased applied voltage is direct metod to attain minimized power and adjusting the frequency for delay plays crucial role. we know CMOS is known for less power relying up on supply voltage, now the designers task is to plan FF's as they're wide employed in digital systems like a broadly useful register, a pipeline register and a limited state machine.

is for very low power digital circuits. It consists of 5 NOR and 2INV's gates. The count of transistors 24, that is same because we know the typical circuit shared static f^2 (CSSF^2). Our proposed f^2 achieved ower- dissipation of 5.884nW and clock atomic weight delay of 3.461 ns, at 0.5-V Power supply and 1MHZ clock frequency.

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II. LITERATURE SURVEY

The approach given in this study is written with an aim to beat the barriers of the downsides. the discussion is formed in a absolute edge trigger register flip flop that is made on the master slave idea concept that isn't at all sensitive to any cover of clock called timed CMOS or CSSMOS [1]. Ultimately an investigation of transistor size has demonstrated that base estimated transistors should be utilized if the parasitic capacitances are not exactly the dynamic door capacitances in a course of rationale entryways [2]. Moreover, in all cases, the aim in down in power consumption is clear: moderate the circuit very slow as attainable, with the minimum possible offer voltage.[3]. A huge conversation are unmistakable in the power of intensity dissemination region calculation as conjointly on correlation methodology and creative investigation. the point of the examination system is to coordinate a huge exhibit of flip-flop topology in CMOS innovation [4].

Disadvantages and Draw Backs for existing techniques:

The CSS FLIP FLOP is the most helpful technique compared to alternative typical techniques, however yet we have to find power dissipation and delay for optimization. TheCSS FLIP FLOP carries with it same 24 transistors as TBF^2. TBF^2 are utilized in standard cell libraries. However utilization (TBFF) becomes very narrow to work with low voltages below the Vth. Proper reason behind this is the yield of the tri state buffers are connected in wired-Or can lead to the increase of the power dissipation. The NLF^2 and CLF^2 contain more number of transistors compared to TBFF and CSS F^2. If the semiconductor device count was increased the area or power dissipation may also increase.

To define the low power and less delay F^2, we propose associate Enhance Circuit Shared Static F^2 contains Nor's and INV's with a small range of Transistors. Can be operated at lower voltages

III. NEW WAY TECHNIQUE:

Proposed Enhance circuit shared static flip-flop (ECSS F^2) Consists of gates which include 5 universal NORs (NOR1-NOR5) and 2 Inverters, and also the total range of transistors are twenty four. The Inverters are used to generate management signals of CLKB and CLK2 from root clock of CLK. NOR1, NOR2, and NOR3 structure an ace lock, while NOR3, NOR4, and NOR5 structure a slave. We can find that NOR3 is shared both inside the ace and slave locks, and is adjusted to accumulate data in the master latch and transfer it to the slave latch. Found with this way we can Enhance circuit shared static flip-flop (ECSS F^2) works.

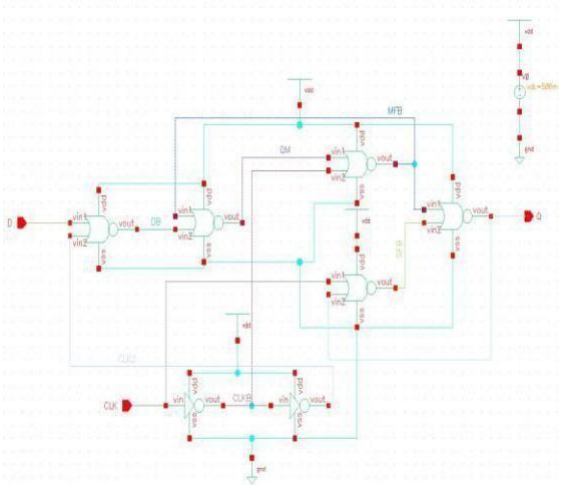

Fig.1. Schematic diagram (ECSS FLIP FLOP)

NOR and NOT gate Designing: An implementation to Nor Gate which belongs to logic family. it's also named as universal gate because of its implementation on different gates. Nor operation is defined as Y=~(A+B). Whenever the both inputs

are '0',then the outcome will be '1', to the remaining in and out's will be '0'. The static nor is designed with the combination of PMOS and NMOS, that is as shown in figure
CMOS.

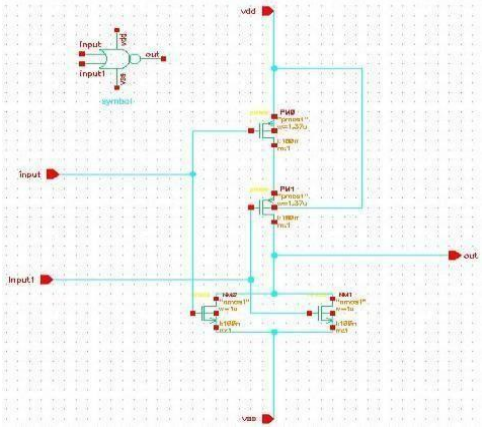

Fig.2.Nor diagram Schematic

Not Gate:

An implementation to Nor Gate know as logic gate
. It is also called as buffer or inverter. normally logical Not operation is Y=~A. basically for every zero input we get an one as output and for every one we get zero as output. Two inverters connected in a series can form a buffer. In the conversion of NOR logic to OR and NAND logic to AND we need NOT gate. The static Not gate is combination of PMOS and NMOS, which is known as CMOS. Below figure shows the schematic.

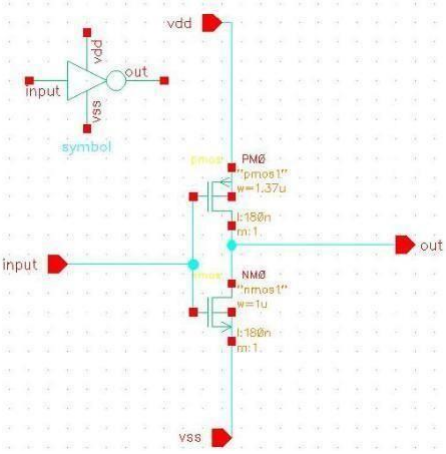

Fig.3. Not Schematic

Timing outline of circuit output is shown in the fig.4. The First latch operates using a positive fringe of control signal of CLK2. once input data, CLK2, and CLKB are low and high, severally, NOR1 works as an electrical converter and the outcome of NOR3 is reset to low. Thus, NOR2 conjointly works as Associate in Nursing inverter, and the data is transferred to QM as "D0". Then, once CLK2 and CLKB become '1' and '0', severally, the outcome of NOR1 is reset to '0'. Therefore, NOR2 and NOR3 type the master latch.

To utilize time perfctly, the other latch frequently uses a negative edge of clock signal of CLK. once CLK and CLKB are '1' and '0', accordingly, now out put of NOR4 is reset to '0' and NOR5 works as an inverter. Then, once CLK and CLKB become '0' and '1', severally, the output NOR3 is reset to low. Therefore, NOR4 and NOR5 type the slave latch, and the data is control at letter as "D0". present proposed method EHANCE_CSS F^2 which operates as a master-slave flip- flop with less number of transistors.

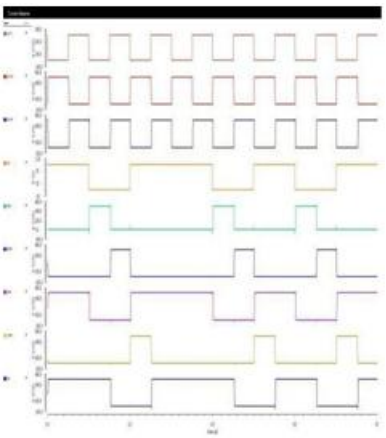

Fig.4. simulated Timing Diagram for enhancedCSS FLIP FLOP

Simulated Waveform:

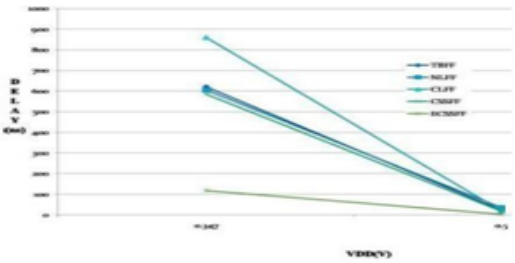

Fig.5. Power delay variations in simulated Waveform of ECSS FLIP FLOP

Power Graph:

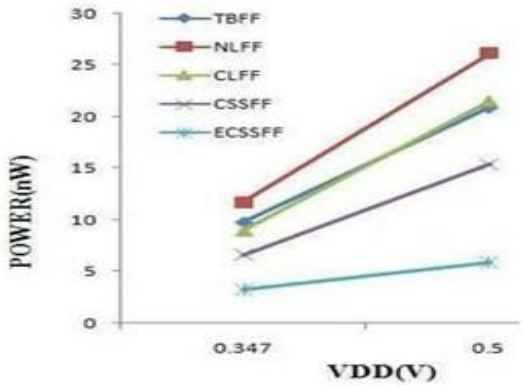

Fig.6. Finding Dissipation of Flip Flops as a work of VDD

Delay Graph:

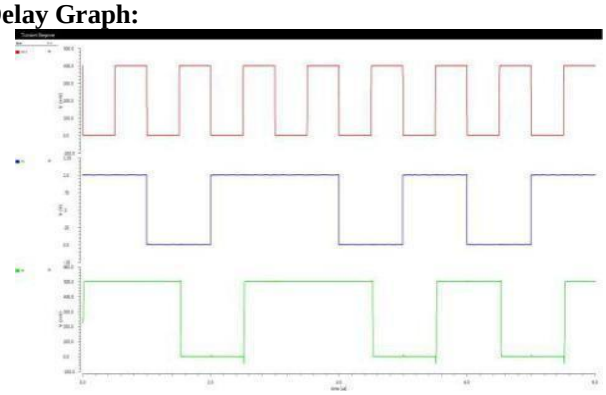

Fig.7. Delay of Flip Flop as a work

TABLE I

FlipFlops	Frequency (MHz)	Power (nW)	Delay (ns)
24T (CSSFlip Flop)	1	15.4	17.4
ECSS Flip Flop	1 (V-bit)	5.884	3.461
ECSS Flip Flop	0.41-1.0 (V-pulse)	12.22	3.439
ECSSFlip Flop	0.41-1.0 (V-bit)	6.396	3.634

Outcomes for the P & D variations

The work of the flip disappointment can explain depending on the parameters, for example, Frequency, PMOS, NMOS Width, Power and Area. The working recurrence of Enhanced CSS FLIP FLOP was great when contrasted with different techniques

TABLE II

FF	P- MOS Width (µm)	N- MOS Width (µm)	Frequency (MHz)	Voltage (V)	Power (nW)	Delay (ns)
ECSS FLIP FLOP (180nM)	1.37	1	1	0.5	5.884	3.461

ECSS FLIP FLOP Values At 0.5V

IV. CONCLUSION & FUTURE SCOPE

Cadence/SPICE simulation in 180 µm and 90 µm standard CMOS process Our proposed ff achieved power- dissipation of 5.884 nw and clock delay of
3.461 ns , at 0.5-V Power supply and 1MHz clock frequency which optimized the power by 9.516 nw and delay by 13.939 ns is compared to CSS FLIP FLOP. present circuit can operate at 0.347 V with enhanced power dissipation low. This process can also be enforced in FIN-FET, SET & CNT-FET and in GNR to optimize power and delay.

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