Real Time Simulation of Wind Farm Connected MMC-HVDC System

Naini Raju Manchala, Sreedevi J, Rajashekar P Mandi, Meera K.S

Abstract*: Real time simulators play a major role in R&D of Offshore wind farm connected modular multilevel converter (MMC)-HVDC system. These simulators are used for testing the actual prototype of controllers or protection equipment required for the system under study. Modular multilevel converter comprises of number of sub modules (SMs) like Half/ full bridge cells. While computing time domain Electromagnetic transients (EMTs) with the system having large number of SMs pose a great challenge. This computational burden will be more when simulated in real time. To overcome this, several authors proposed equivalent mathematical model of MMC. This paper proposes the real time simulation start-up of offshore wind farm connected modular multilevel converter (MMC)-HVDC system. This paper also describes about how the above said systems is simulated in OPAL-RT based Hypersim software.

***Keywords* : Modular multilevel converter, Offshore wind farm, Real-time simulator, FPGA**

I. INTRODUCTION

Over the years offshore wind farm planning has increased and the capacity is increasing day by day. Moreover, they are several miles away from onshore grids. Several offshore winds of capacities over 1000MW are planned in North Sea coast of Germany and Northwest coast of United Kingdom [1]. There was always a heated argument between DC and AC proponents over the years. The advantages like long distance bulk power transmission, long distance under water cable crossings, connecting two different frequency systems and power transfer through long distance underground cables make HVDC more popular than HVAC transmission [2].

Several authors in the literature described about the start-up sequence of MMC-HVDC technology [3]-[4]. No author in the literature described about simulation start up sequence of offshore wind farm connected MMC-HVDC system.

Revised Manuscript Received on March 5, 2020.

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Full scale modeling of MMC-HVDC with hundreds of SMs in per arm/valve as shown in Fig.1 is computationally immense talk, as it requires CPUs with high computing power and memory [2]. Detailed models which replicate the IGBT and its anti-parallel diode conductions are inefficient as the time required for simulation is prohibitively long. To overcome this, several authors proposed equivalent model which replicate the actual MMC. Authors in [5][6] proposed average value model. This model assumes that all the capacitors in each SM are balanced and also assume an equivalent capacitor which replaces all the SM capacitors of the valve. One of the drawbacks of this model is that it cannot replicate the actual inner dynamics of MMC to the microscopic level. In [7][8] authors used Norton equivalent of valve in order to achieve real-time performance with reduced computational burden. In [9], IGBT switch is represented as resistance and capacitor as current source with conductance in parallel to it.

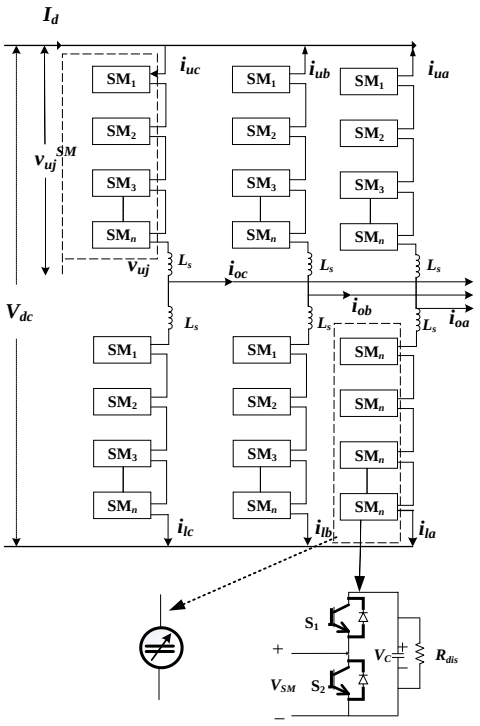

Fig. 1.MMC configuration

Authors in [10] proposed state space nodal method. The network under study is decoupled into system using nodal equations and such systems are solved using state space equations. In [11] authors proposed a surrogate network equivalent for each valve for both HB-SM and FB-SM separately. According to the switching states the SMs are divided into three sections (Blocked, Unblocked and Bypassed SMs) and a Thevenin's equivalent is used for each

SM capacitor. Both Thevenin's and Norton's equivalent of the large electrical circuits still require huge computationalpower in order to recalculate to solve for every change of state of switches

In this paper an equivalent circuit proposed by authors in [12] is considered. Every detail of all the SMs in MMC are considered in this method and using Euler integration, it directly calculates the individual SMs capacitor voltages in parallel. As this method uses an equivalent circuit with certain topology it requires very less computational burden when compared to Thevenin's and Norton equivalents. This method can be implemented for HB-SM, FB-SM and other SMs like Double clamped SMs.

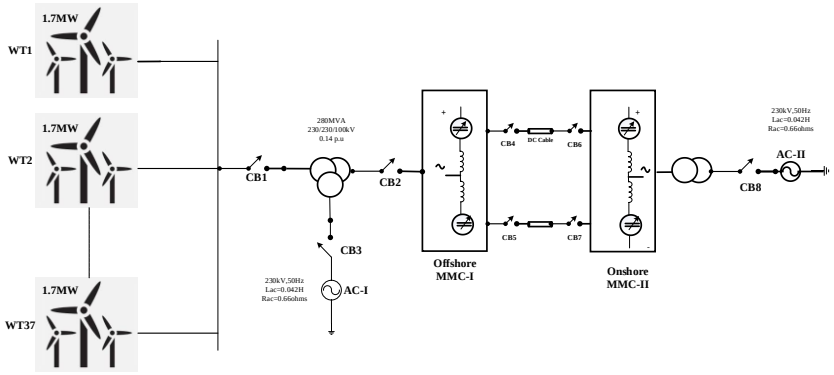

Fig. 2. Wind farm connected MMC-HVDC system

II. . BASIC STRUCTURE OF OWF CONNECTED MMC-HVDC SYSTEM

The SLD (single line diagram) of OWF connected MMC-HVDC system is shown in Fig .2. Wind turbine driven DFIG is considered for this study and modelling of DFIG is described in detail in the literature [13]- [16]. Each wind turbine connected DFIG has capacity to generate 1.7MW and 37 number of such DFIGs constitute Offshore Wind farm. Modelling of MMC-HVDC is explained in detail in the following sections. Parameters of MMC-HVDC systems are given in Table.1

Table-I.Main circuit parameters

Circuit components	*Parameters*
AC system voltage (AC-I&AC-II)	230 kV
AC system inductance (AC-I&AC-II)	0.04 H
AC system resistance (AC-I&AC-II)	0.64 ohm
Tertiary Transformer rating	100 MVA
Tertiary Transformer ratio	230/230/100 kV
Tertiary Transformer leakage reactance	18 %
DC bus voltage	+/-100 kV
Equivalent arm resistance *Rs*	0 ohms
Number of SMs per arm N	250
SM Capacitance	24mF
Arm inductance *Ls*	0.0024H

A. Opearating principle and topology of MMC

Modular multilevel converter consists of N number of SMs. Each SM can be half bridge/ full bridge or any other converter cells. Half bridge can generate two level output voltage and full bridge SM can generate three level output voltage. All the SMs are connected in series in each arm along with arm reactor *Ls* as shown in Fig. 1.

A half bridge SM is considered for present study and can be seen in Fig. 1. In normal operation each HB-SM has three states: First is Blocked state where both switches are OFF (and) and Second is Inserted state where V_{SM} =*Vc*(when switch S_1 is ON and S_2 is OFF) and Third state is Bypassed state where V_{SM} =0 (When switch S1 is OFF and switch S2 is ON). Capacitor voltage of SM is set and can be controlled to its nominal value in normal operating condition. Then, the per-unitized total voltage across the arm is nothing but the voltage across the SMs which are ON. With this we can conclude that each arm can be an equivalent controllable voltage source like in the case of voltage source converters.

B. Modelling of SubModule in FPGA

Mathematical modelling of each SM is carried out in Field programmable gate array (FPGA) at discrete fixed time step. V_C represents the voltage of capacitor in each SM, which is nothing but the discrete integral of charging current through the capacitor represented by iC. as depicted in Eq.1. Here the values (n-1) and n represent the previous step value and the present step value respectively and ΔT_{fpga} represents FPGA time step (500ns for this particular study) and SM capacitance is represented by *C*.

$$V_{C.n} = V_{C.(n-1)} + \frac{\Delta T_{fpga}}{C_{SM}} \times i_{C.n} \quad (1)$$

$$i_{C.n} = K \times i_{am} - \frac{V_{C.(n-1)}}{R_{dis}} \quad (2)$$

$$V_{SM} = K \times V_{C.n} - i_{am.n} \times R_{on} \quad (3)$$

The charging current of the capacitor is obtained as shown in Eq.2. Where K represents the state of the upper switch in SM and arm current is represented by i_{am}.. The arm current fill flow through the upper arm when the switching state K=1 and passes through the capacitor and the discharge resistance connected parallel to it (R_{dis}). Otherwise the lower switch in SM will bypass the arm current. Forward Euler integration method is used where the capacitor voltage in the previous state is used to break the algebraic loop. The error introduced due to method is negligible as the time step consider is much smaller than the voltage discharge time constant of the capacitor. Lastly the SM voltage is obtained as shown in Eq.3 and it is represented by V_{SM} and conduction losses of the IGBT switches represented with resistive losses as internal resistance is represented as R_{ON}.

Modelling of SM in FPGA is shown in Fig. 3. Here it can be observed that IGBT switching state and the arm currents

are the inputs to the SMs in FPGA and total SMs voltage at the terminal is the output from FPGA. Capacitor voltage of each SM is the internal state and remaining parameters are all known. With the use of base power and nominal voltage of SM, all the parameters are converted into per unit values using nominal voltage and power of SMs as base values. FPGA has capability of larger parallel operating units. For the present study, the bit stream used has the capability of solving 1530 SMs at 500ns time step in one FPGA unit. MMC with larger number of SMs like more than 500 SMs per arm which means 3000 SMs and more for both converters can be solved in two FPGA Virtex-7 and Virtex-6 boards.

C. Decoupling and Simualition at Mutli rate

The voltage across all the SMs in one arm is the defined as output voltage of MMC as depicted in Eq.3.

The second term in this equation is insignificant (as resistance under conducting state is small) and the first term is predominant. Moreover, due to presence of arm reactor, the arm current cannot change abruptly. Due to this reason, the arm current from the previous time can be utilised for finding the total SM capacitor voltage as shown in Eq.3.Thus, the output voltage of MMC is obtained mainly by switching states and voltage of capacitor in each SM. These capacitor voltages are non-other than those defined by the historic values in the internal states. This is how the SMs of each arm in MMC can be evaluated separately in FPGA and is also decoupled for the rest of system.

Simulation of whole system is carried out at different sampling rates. Mathematical modelling of MMC is carried out in FPGA as demonstrated in previous at sampling time of 500ns and the rest of the systems including DFIG based wind farms is simulated in CPU at sampling time of 30micro seconds. Here in the CPU the MMC is represented as a controllable equivalent voltage source.

The FPGA and CPU have to be synchronized; the exchange of data occurs at sampling time of CPU. This is because the data present in the FPGA updates at faster rate than compared to the CPU. Express link PCIe will act as channel for the transfer of data from CPU to FPGA and vice versa. FPGA send output terminal voltage to the CPU and CPU will send arms current in turn to FPGA. Due to arm reactor, the arm current changes gradually and is transferred from CPU to FPGA at the instant of synchronization (instantaneous value at the instant of sync). Until the next sync instant, it is held for one-time step of CPU.

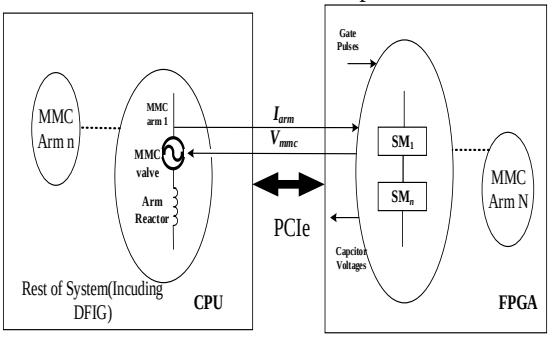

Fig. 3. FPGA and CPU simulation at Multi rate

The output terminal voltage of MMC is updated in FPGA after parallel processing at a faster rate. Due to inter step switching events there may be many step changes within each CPU time step. It is not advisable to transfer instantaneous value of the output voltage of MMC at every CPU time sampling which may lead to inaccurate results due to problem of aliasing at poor sampling of signal (at CPU time step).The arm current mainly depends on arm reactor but have accurate results as it is required to send average value of the MMC output voltages calculated within FPGA to CPU over the time period of CPU time step

III. CONTROL STRUCTURE OF MMC

The overall control structure of MMC is given in Fig. 4. Multilevel voltage signals are achieved by comparing the sinusoidal reference signal with many carrier singles and the process is called pulse width modulation (PWM). Phase shifted carrier PWM modulation technique is utilized for generation of gate pulses.

The reference sinusoidal signal n_i consists of both DC component and sinusoidal fundamental component whereas in the frequency domain, the synthesized multilevel signal *Ni* after PWM consists of components as shown in Eq.4.

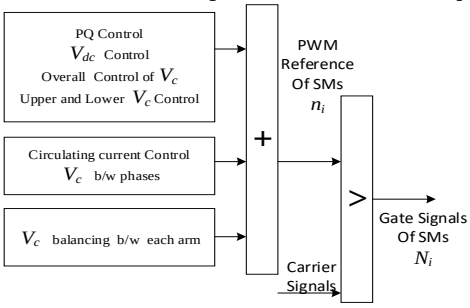

Fig. 4.Control structure of MMC

$$N_{1i} = n_{1i} + harmonics \quad (4)$$

Fig. 4. shows the overall control structure required for the normal operation of MMC and the SM capacitor voltage balancing control scheme is one among them. SM capacitor voltage balancing control scheme is described in detail in [17]

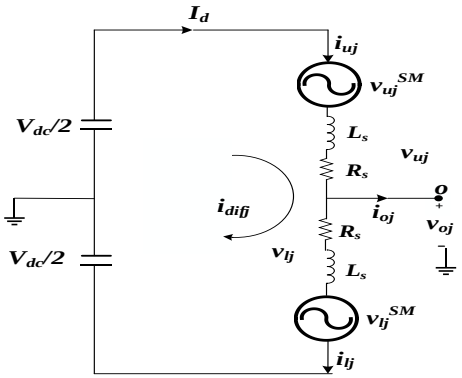

Fig. 5.MMC single phase equivalent

A single-phase equivalent of MMC is shown in Fig. 5 where$R_s$and L_s are arm resistance and inductance respectively.V_{dc} and $I_d$are the 'dc' voltage and current respectively. $v_{oj}$is the converter 'ac' output voltage of *j* phase and $i_{oj}$is corresponding 'ac' line current of phase *j*.v_{lj}^{SM} and v_{uj}^{SM}represent the converter

arm voltage which is generated by total voltage across the SMs of lower and upper arms respectively of phase *j*.From Fig. 5, the lower arm current i_{l_j} and upper arm current i_{u_j} can be expressed in terms of difference currents i_{dif_j} and 'ac' line current of the corresponding phase as shown in Eq.1 and 2.

$$i_{u_j} = i_{dif_j} + \frac{i_{o_j}}{2} \quad (5)$$

$$i_{l_j} = i_{dif_j} - \frac{i_{o_j}}{2} \quad (where\ j=a, b, c) \quad (6)$$

In each phase the inner current of each phase flows through lower and upper arms is shown in Eq.6.

$$i_{dif_j} = \frac{i_{u_j}+i_{l_j}}{2} \quad (7)$$

From Fig. 5, the following equations of MMC can be characterized as

$$v_{o_j} = v_j - \frac{R_s}{2} + i_{o_j} - L_s \frac{di_{o_j}}{2} \quad (8)$$

$$L_s \frac{di_{dif_j}}{dt} + R_s \times i_{dif_j} = \frac{V_{dc}}{2} - \frac{v_{lj}^{SM}+v_{uj}^{SM}}{2} \quad (9)$$

Where v_j is called the inner EMF generated in phase j and is expressed as of upper and lower arm voltages generated by cascaded SMs.

$$v_j = \frac{v_{lj}^{SM}-v_{uj}^{SM}}{2} \quad (10)$$

Here v_{o_j} is considered as 'ac' voltage and i_{o_j} as 'ac' current of phase j and the control variable v_j can control i_{o_j} .The current control scheme proposed by many authors earlier can be adopted for MMC and Eq. 9 determines the MMC inner dynamic performance and can be redefined as

$$v_{dif_j} = L_s \frac{di_{dif_j}}{dt} + R_s \times i_{dif_j} = \frac{V_{dc}}{2} - \frac{v_{lj}^{SM}+v_{uj}^{SM}}{2} \quad (11)$$

Where v_{dif_j} is called inner unbalance voltage of respective phase.

Modular multilevel converter configuration with its unique feature requires additional controls apart from basic controls of Voltage source converters (Active and reactive power control). All the multiple control schemes of MMC are classified as Active and Reactive power control, DC voltage control scheme, SM capacitor voltage control (Balancing among each SM and Overall SM control) and Circulating current suppression control.

A. Reactive and Active power Control scheme

The basic control scheme for MMC is similar to conventional *dq* control of VSC. Where the ac voltage of VSC is controlled to the reference value which is recalculated so that both reactive and active powers tract the actual set points as shown in Fig. 6. The actual control logic is described in [18]. The voltage across the upper and the lower arm phase reactors v_{u_j} and v_{l_j} are controlled as per the same reference value of the control loop, then the lower and the upper arm equally contribute to the phase currents.

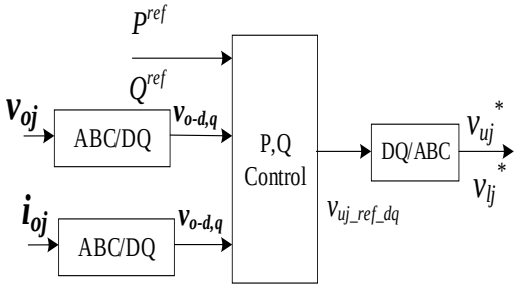

Fig. 6.Reactive and Active power control

B. DC link voltage control

In Static VAR compensator (SVC) the DC capacitor voltage determines the DC voltage and is regulated with active power control scheme. But in case of DC voltage control in MMC is direct and fast using separate control scheme while neglecting DC capacitor link. DC voltage is determined by the following equations form Fig.7.

$$V_{dc} = v_{lj}^{SM} + v_{uj}^{SM} + v_{u_j} + v_{l_j} \quad (12)$$

In order to regulate DC voltage (V_{dc}) to 1 pu, the gating pulse of $SMN_{1i}$is calculated as shown in Fig. 7and also the reference PWM signals $n_{1i}$are calculated.

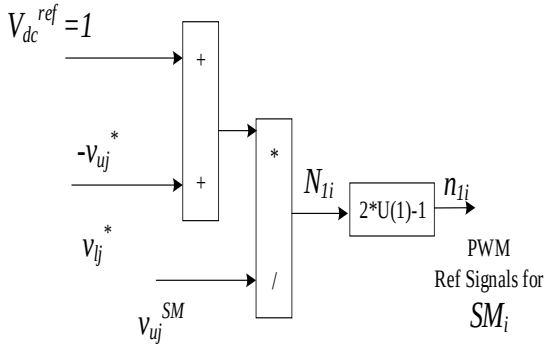

Fig. 7.DC link voltage control

C. Circulating current suppression control scheme

The main cause for the generation of circulating current is the difference among the voltages of each phase in MMC which was observed by authors in [19]-[20]. These circulating currents are basically negative sequence current with frequency twice than that of fundamental [22]. This leads to increase in the rms value of arm current which in-turn results in increase of converter power losses [19]. In each phase these circulating currents get super imposed on the 'dc' current component [22]. As a result of all the above discussion, it can be concluded that inner difference current described in Eq.3 that consists of two parts. One is the 'ac' component corresponding to circulating current and the other is the 'dc' current component (One-third of complete 'dc' current component). Unbalanced inner voltages and currents are transformed to *dq* reference frame using ABC/DQ transformation and Fig. 8 depicts the circulating current transfer function.

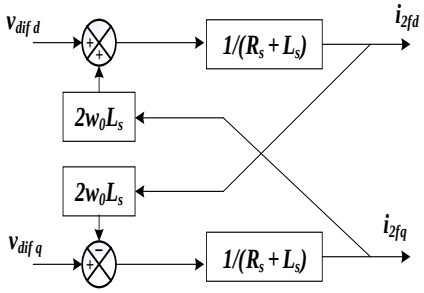

Fig. 8.Circulating currents transfer function

In order to minimize the circulating current, reference value of both circulating currents in 'dq' reference are set to zero i.e.,$i_{2f_{d_{ref}}} = 0$ and $i_{2f_{q_{ref}}} = 0$. With cross coupling

compensationandPIcontroller, the control signals$v_{dif_{d_ref}}$ and $v_{dif_{q\_ref}}$ are obtainedas shown in Fig. 9. Finally, the unbalance inner difference voltage in 'a-c-b' reference frame is obtained using inner transformation matrix.

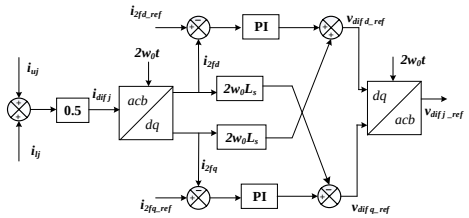

Fig. 9.Circulating current suppression control scheme

IV. SIMULATION RESULTS

The start-up sequence of MMC-HVDC connected Offshore wind is a bit complex as the all the SM capacitors need to be charged to certain level before evacuating power generatedby windfarm through HVDC link. Initially CB_1 and CB_3 are closed (also CB_2, $CB_8$and all DC breakers are open)as all the windfarms are energized and the power generated from these windfarms can be seen as P_{ac1} and Q_{ac1}in Fig. 10(c). Per unit voltage in the DC link are charged to 0.576pu on left and 0.61pu on right as shown in Fig. 10(a) at this stage as the AC breakers CB_2 and $CB_8$are open. Fig.10(b) depicts the real and reactive power flow at the point of common coupling(PCC) where DFIG is connected to MMC-HVDC link. Fig. 10(d) presents the real and reactive power entering the Offshore MMC converter.$I_{arm.}$

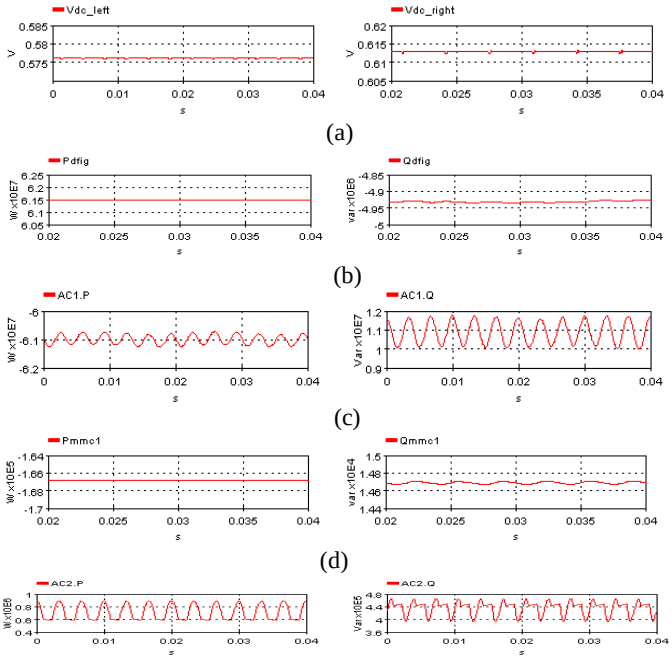

Fig. 10. Simulation results before uncontrolled charging (a) DC voltage in PU on near MMC-I&II. (b)Real and reactive power generated by DFIG. (c). (d) Real and reactive entering MMC-1 (e)Real and reactive AC-II

A. Uncontrolled charging of SM capacitors from AC grid

As the second stage of start-up sequence of offshore wind farm connected MMC-HVDC systems, the CB_2 and CB_8 are closed. Immediately after closing these ac circuit breakers, it is observed from the Fig. 11 that the pu voltage of the DC link on the left and the right are charged to around 0.7pu.

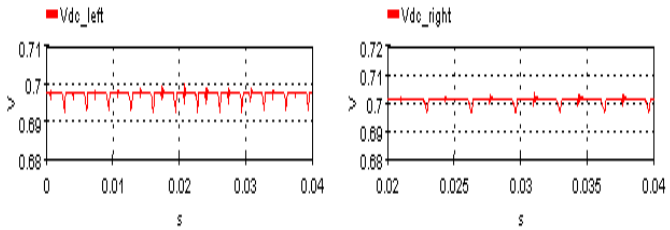

Fig. 11. DC voltage in PU on near MMC-I&II after uncontrolled charging.

B. Controlled charging of SM capacitors from AC grid

After the dc link voltages are charged to 0.7 pu unit, the IGBT pulses of both onshore and offshore converters are enabled. This results in both the DC link voltages are charged to 1 PU as shown in Fig.12. As both the DC breakers are open (CB_4-CB_7) both the converters operate in STATCOM mode.

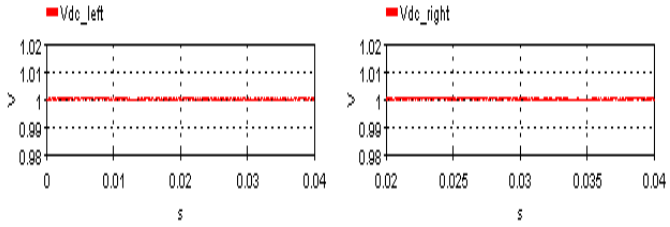

Fig. 12. DC voltage in PU on near MMC-I&II after controlled charging.

C. Power Evacuation through HVDC link with PQ control and disconnecting offshore AC grid

One of the major advantages of MMC is that both active and reactive power can be controlled independently. After the pulse signal of both offshore and onshore grid are enabled, Voltage of the DC link will attain 1 pu(STATCOM mode of operation) and later the DC breakers are closed. Active power control enables the flow of real power in both the direction (Mode of operation of MMC as inverter/converter which will depend on the active power control). Keeping this in view active power control isset in such a way that the Offshore MMC will act as rectifier and onshore will act as inverter. Both the converters can either supply reactive power orabsorb reactive as per the requirement.

In the present scenario, the active power control is set in such a way that the total power generated by the windfarms is evacuated through HVDC link and the power observed by AC-1 (both active and reactive power) is zero as shown in Fig. 13(b). At this instant angle in phase locked loop(PLL) is adjusted and CB3 is opened to disconnect AC source (AC-I). From Fig. 13, it can be observed that the real power received at AC-II is 59.5MW and the negative sign indicates the real powerabsorption.

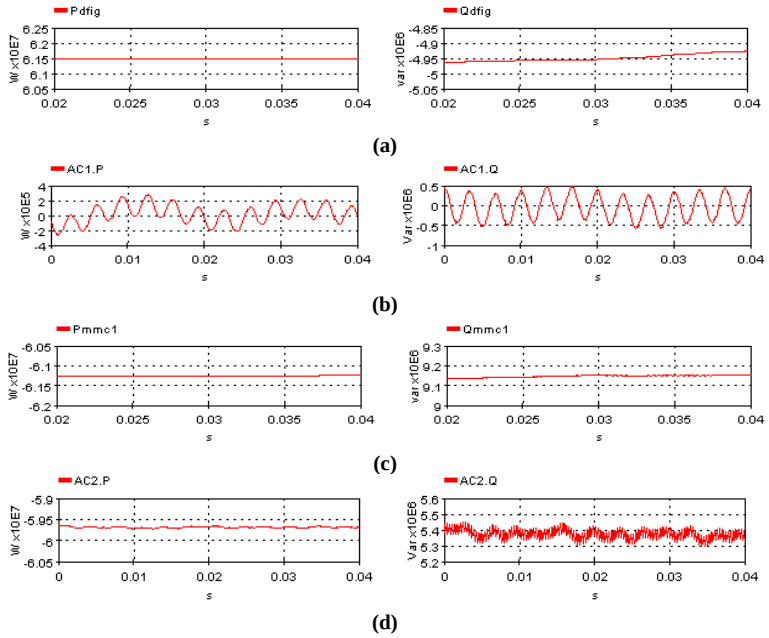

Fig. 13. Simulation results after disconnecting AC-1 (a) DC voltage in PU on near MMC-I&II. (b) Real and reactive power generated by DFIG. (c) Real and reactive power entering MMC-1 (d) Real and reactive power in AC-II

V. CONCLUSION

Modular multilevel converter comprises of number of sub modules (SMs) like Half/ full bridge cells. While computing time domain Electromagnetic transients (EMTs) with the system having large number of SMs pose a great challenge. To overcome challenge this paper need for real time simulation and also proposed the real time simulation of offshore wind connected MMC-HVDC system and its startup sequence. This paper also describes about the mathematical modelling of MMC in CPU and FPGA and multi rate sampling and its advantages are also explained in detail. Thecontrol architecture of MMC and its necessity is explained in detail. The start up sequence of the wind farm connected MMC-HVDC system is explained.

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