

Circulating Current Suppression Control in Surrogate Network of MMC- HVDC System

Naini Raju Manchala, Sreedevi J, Rajshekar P mandi, Meera K.S

Abstract: Modular multilevel converter consists of hundreds of submodules (SMs) like half bridge and full bridge converters etc. These hundreds of SMs and electrical nodes poses challenges while computing electromagnetic transients (EMTs). This problem becomes more complex while computed in real-time. To overcome this, an equivalent topology to model MMC arm/valve called surrogate network is utilized. But, the major ambiguity integrated with surrogate network model is SM capacitor voltage balancing. This leads to variation in voltage among the three phases which are parallel and produces circulating current between the three phases. A control circuitry is proposed in this paper to suppress/minimize circulating currents between the phases. Apart from circulating current suppression, the 'ac' output voltage is also enhanced at the converter with this proposed controller. Simulation is carried out in RSCAD software using RTDS simulator.

Keywords: Modular multilevel converter (MMC). Surrogate network. Circulating currents in MMC.

I. INTRODUCTION

Over the last decade high voltage direct current (HVDC) systems based on voltage source converter (VSC) based has of gained a lot of momentum because of its wide spread applications in solar power, wind energy, smart grids technology and distributed generations[1]. Recently, MMC technology has gained importance over VSC technology [2]-[6]. Ability to generate 'ac' voltages with less harmonic content due to multilevel capability in MMC reduces the requirement of filters. By increasing the SM number, both voltage and power can be scaled as per the requirement.

Modular multilevel configuration is shown in Fig.1 and modelling of full-scale MMC-HVDC with large number of cells as SMs per arm is an immense task. Systems with huge memory and computing power are required to carry on such tasks and simulation time is also large. In an attempt to decrease the simulation time, authors in [7], [8] proposed an average value model of MMC. Although, the authors in [7], [8] proposed an efficient method to model the MMC-HVDC system for system studies.

It cannot completely replicate the internal dynamics of MMC to the nanoscopic level during transient studies. Authors in [3], proposed full scale modelling of MMC-HVDC based on EMT approach. Thevenin equivalent and Dommel's Norton circuits for SM capacitors and two-state resistive approach for IGBT switching devices are used to represent the entire arm of the MMC into two terminal Thevenin equivalent circuits. In [9] authors proposed accelerated model. This accelerated model is based on generalized circuit theory of Kron [10]-[12]. Authors in [13] proposed two simplified average models of slow dynamic study in MMC. This model is appropriate for small signal and transient stability studies where manipulations in MMC active and reactive power are helpful in achieving 'ac' side system stability.

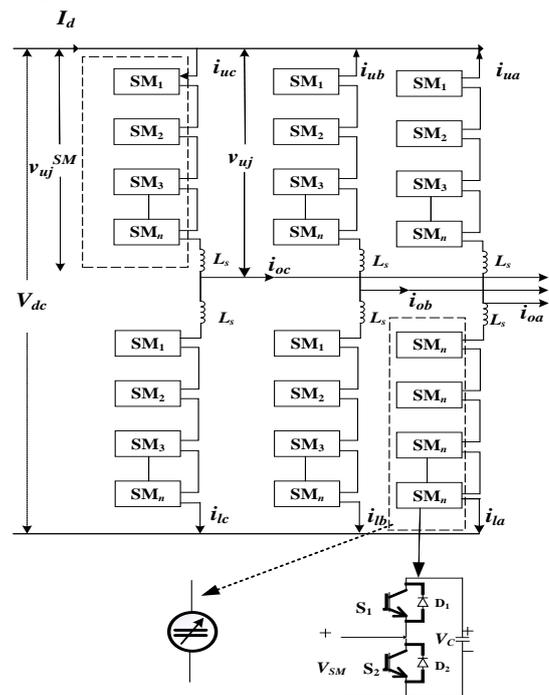


Fig.1 MMC configuration

Generally, in EMT simulations all the power system network line and machines are simulated at 50 μsec time-step [14]. But the switching operation of VSC-HVDC is carried out at few μsec. Every time the converter switch turns ON/OFF, conduction matrix in the Dommel algorithm has to be inverted. This inverting or decomposing of conduction matrix is avoided with the use of small time step VSC model (2 μsec) as proposed in [15]. MMC valve modelling in real time is much more challenging as it contains large number of SMs for each arm.

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It is quite time consuming to evaluate such large number of switching devices in small time-step. Surrogate network proposed by authors in [16],[5] to model MMC valves in real time is used to overcome above mentioned ambiguities. Surrogate network is explained in detail in section II.B. This paper also presents control circuitry to suppress circulating current in surrogate MMC model.

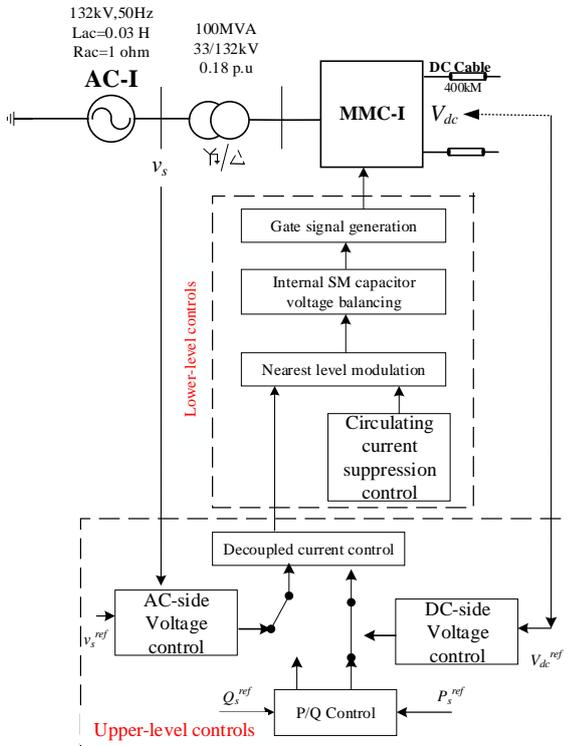


Fig.2. MMC-HVDC system along with control architecture

Main problem associated with MMC is SM capacitor voltage balancing. Authors in [17], [18] proposed an algorithm to balance SM capacitor voltages by sorting method. Tracking the arm current direction, the SMs with capacitor voltages higher and lower than the nominal value are sorted and triggered. SM capacitor voltage variation in each arm results in voltage difference among the three phases which are in parallel and in turn lead to circulating current among them. Arm currents are distorted due to presence of these circulating current in all the six arms. This will lead to increase of rms value of currents in each arm and also increases converter losses [19]. Authors in [20] investigated the circulating current problems with various load phase angles. In [21], [22] authors discussed about relationship between parameters of arm inductor and amplitude of circulating current.

Circulating current can be reduced with the increase in size of arm inductor but cannot completely eliminate them. Moreover, it is not a popular practice of using inductor of high voltage due to large voltage drop across it and also they are of high cost. Authors [19], [22] proposed an efficient control circuitry to eliminate circulating current. In this control circuitry, the generated EMF and the component which is to be controlled must be in-phase with each. Also, the converter arm impedance angle should be measured accurately and need to be compensated. During the balance condition, these circulating currents consist of negative sequence component and frequency double to that of fundamental frequency. A new control scheme is presented in

this paper to mitigate the circulating currents in MMC based on rotational negative sequence components at double line-frequency.

The structure of rest of the paper is as follows. Basic structure and modelling of MMC-HVDC in RTDS is described briefly in Section II. A brief description of control architecture along with internal SM capacitor voltage balancing is depicted in Section III. Section IV describes the proposed control circuitry to suppress circulating current in surrogate MMC model. The simulation results presented in Section V to justify the proposed control scheme.

II. BASIC STRUCTURE AND MODELLING OF MMC-HVDC

A. Modular multilevel converter configuration

Three phase modular multilevel converter configuration is shown in Fig.1. Each phase leg has upper arm (u) and lower arm (l) and midpoint of each converter phase leg is connected to the three phase 'ac' system. Each arm consists of N number of SMs and an inductor L_s connected in series. Sub modules can be half, Full bridge or any other converter cell etc. A half bridge SM is considered for present study and can be seen in Fig.1. In normal operation each HB-SM has three states: First is Blocked state where both switches are OFF (S_1 and S_2) and Second is Inserted state where $V_{SM}=V_C$ (when switch S_1 is ON and S_2 is OFF) and Third state is Bypassed state where $V_{SM}=0$ (When switch S_1 is OFF and switch S_2 is ON).

B. Basic structure of MMC-HVDC

Single line diagram of MMC-HVDC system and its control architecture is shown in Fig.2 and system parameters are shown in Table.1. Authors in [16],[5] proposed a fictitious network called surrogate network for full scale MMC-HVDC link. A surrogate network with six HB-SMs is shown in Fig.3 to understand the operations of the network that mimics the actual MMC. The surrogate network when compared to real MMC valve generates similar computational results.

Three sections namely: 'Blocked' SM section, 'Deblocked' SM section and Reaction section constitute Surrogate network as shown in Fig.3. The SM3 and SM4 which are isolated or not included in the surrogate network come under 'Bypassed' SM section as there is no path for flow of arm current through them. Capacitor present in the 'Bypassed' section will discharge through the parallel conductance branch. Capacitor of each SM is introduced into either 'Deblocked (Inserted)', 'Blocked' or 'Bypassed' section. From Fig.3 with positive direction of arm current the blocked and 'Deblocked' (inserted) SMs will be charged and while the current is negative only the 'Deblocked' SM will discharge and 'Blocked' SMs will not discharge because of presence of antiparallel diodes. The position of diodes D1 and D2 in the surrogate network will provide the correct operation of all capacitors in the SMs.

With the negative direction of arm current diode D2 will conduct which will bypass the capacitor of 'Blocked' SM leaving no path for discharge. In a single HB-SM, at an instant the arm current will flow either through IGBT or diode which is antiparallel to it.

Therefore the total impedance and voltage and across the valve can be accurately modelled by multiplying the turn ON resistance and voltage of diode D1,D2 in one SM with the total SMs present in the arm. Irrespective of SMs number in the arm, the number of switching elements present in the surrogate network are only two. This will reduce the computational burden significantly during simulation

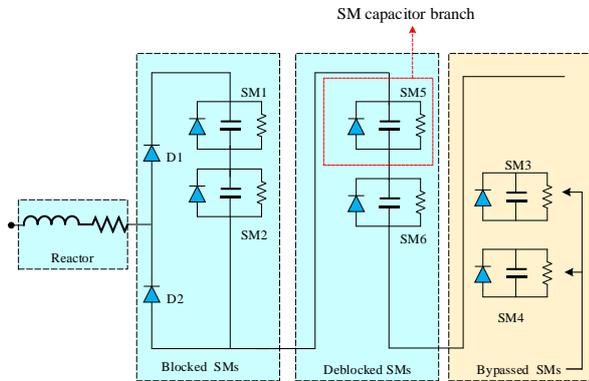


Fig.3. Surrogate network of Half- bridge SM

Main circuit parameters

Circuit components	Parameters
AC system voltage V_s	132 kV
AC system inductance	0.03 H
AC system resistance	1ohm
Transformer rating	100 MVA
Transformer ratio	132/33 kV
Transformer leakage reactance	18 %
Equivalent arm resistance R_s	0 ohms
Sub modules per arm	512
Capacitance of each SM	50000 micro F
Arm inductance L_s	0.0027 H
DC resistance $R_{dc}/2$	0.01 ohm
DC bus voltage $V_{dc}/2$	33 kV

In order to mimic the performance of antiparallel diode in real SMs, the surrogate network has upward directed diodes are connected across each capacitor. They will not allow the capacitor to charge to negative voltage as the diodes D1 and D2 are unable to do so. However, these upward directed diodes are not modelled as switching elements. They only are present to force the voltage across the capacitor to 0kV when the calculated value is other than 0 kV. Surrogate network for full bridge is described in [5].

III. OVERVIEW OF CONTROL ARCHITECTURE

Control architecture for MMC-HVDC is shown in Fig.2. Each terminal is controlled commonly using ‘dq’ decoupled control scheme [23]. The control system hierarchy is depicted in Fig.4. Major task of the master controls is to provide the reference values to each terminal and control modes for the converters. These control modes set the converters weather to operate in active power /‘dc’ voltage control mode or ‘ac’ voltage /Reactive power control mode. The upper level control has two control stages. First is called power control loop which receives signals from master control set points and generate ‘dq’ current component references. Second is decoupled current control loop which generate reference waveforms that represent terminal ‘ac’ voltages. Lower level controls normally produce gates pulses to generate the

signals (‘ac’ waveforms) as requested by upper level controls. Lower level controller mainly constitutes of three parts. First is the proposed circulating current suppression control scheme which is presented in section IV, next are Nearest level modulation techniques (NLM) and internal SM capacitor voltage balancing controls. In [24] authors proposed more efficient stair-case technique called Nearest level modulation technique (NLM). This will transform the modulated signals to integer order number that vary between 0 to 512. Where 512 are the total SMs considered per each arm. The reason for selecting 512 SMs is to generate waveforms with less number of harmonics.

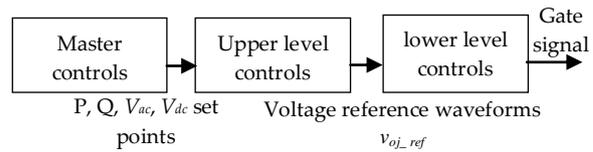


Fig.4. Control hierarchy

C. Internal SubModule capacitor voltage balancing

Basic principle is that all the voltages of SM capacitor are equal at beginning of each small-time step. During the ensuing time step, all the SM capacitors cycled notionally from bypassed state to inserted state with the state duration that is obtained by comparing the SM order with the SM number. As a result of which, all the SM capacitor voltages are almost equal after each small-time step. In fact, in each arm/valve the computations are carried out for one ‘Deblocked/Inserted’ SM, one ‘Bypassed SM’ and one ‘Blocked’ SM. The variation in the voltage of these SMs will determine the total voltage variation by multiplying individual change with total number of such SMs in each section. Later, the net variation in voltage is distributed equally among the SMs of the arm. This is how the SM capacitor voltage balancing is carried out internally. Despite of this internal SM capacitor voltage balancing, it is observed that there is small voltage difference among the three parallel phases of the MMC. This leads to circulating current as explained earlier. To overcome this a circulating current suppression control logic is proposed

IV. CIRCULATING CURRENT SUPPRESSION CONTROL

The control scheme proposed is highlighted in Fig.2.A single phase equivalent Surrogate MMC mode is shown in Fig.5 where R_s and L_s are arm resistance and inductance. V_{dc} and I_d are the ‘dc’ voltage and current respectively. v_{oj} is the converter ‘ac’ output voltage of j phase and i_{oj} is corresponding ‘ac’ line current of phase j . v_j^{SM} and $v_{u_j}^{SM}$ represent the converter arm voltage which is generated by total voltage across the SMs of lower and upper arms respectively of phase j . From Fig.5 the lower arm current i_{lj} and upper arm current i_{uj} can be expressed in terms of difference currents i_{dif_j} and ‘ac’ line current of the corresponding phase as shown in Eq.1 and 2.

$$i_{u_j} = i_{dif_j} + \frac{i_{o_j}}{2}$$

(1)

$$i_{o_j} = i_{dif_j} - \frac{i_{o_j}}{2} \quad (\text{where } j=a, b, c) \quad (2)$$

In each phase the inner current of each phase flows through lower and upper arms is shown in Eq.3.

$$i_{dif_j} = \frac{i_{u_j} + i_{l_j}}{2} \quad (3)$$

From Fig.5, the following equations of MMC can be characterized as

$$v_{o_j} = v_j - \frac{R_s}{2} i_{o_j} - L_s \frac{di_{o_j}}{dt} \quad (4)$$

$$L_s \frac{di_{dif_j}}{dt} + R_s * i_{dif_j} = \frac{V_{dc}}{2} - \frac{v_{u_j}^{SM} + v_{l_j}^{SM}}{2} \quad (5)$$

Where v_j is called the inner EMF generated in phase j and is expressed as of upper and lower arm voltages generated by cascaded SMs.

$$v_j = \frac{v_{l_j}^{SM} - v_{u_j}^{SM}}{2} \quad (6)$$

Here v_{o_j} is considered as ‘ac’ voltage and i_{o_j} as ‘ac’ current of phase j and the control variable v_j can control i_{o_j} . The current control scheme proposed by many authors earlier can be adopted for MMC and Eq. 5 determines the MMC inner dynamic performance and can be redefined as

$$v_{dif_j} = L_s \frac{di_{dif_j}}{dt} + R_s i_{dif_j} = \frac{[V_{dc} - (v_{u_j}^{SM} + v_{l_j}^{SM})]}{2} \quad (7)$$

where v_{dif_j} is called inner unbalance voltage of respective phase.

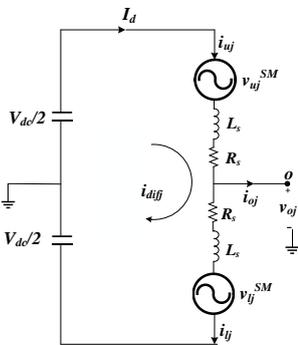


Fig.5. MMC single phase equivalent

The main cause for the generation of circulating current are inner difference among the voltages of each phase in MMC which was observed by authors in [20]-[22]. Basically circulating current are negative sequence currents with double line frequency [22]. They lead to increase in converter losses and rms value of arm current [19]. In each phase these circulating currents get super imposed on the ‘dc’ current component [22]. As a result of all the above discussion, it is can be concluded that inner difference current described in Eq.3 consists of two parts. One is the ‘ac’ component corresponding to circulating current and the other is the one third ‘dc’ current component. Inner difference current expressions of all the three phases are as follows:

$$i_{dif_a} = \frac{I_d}{3} + I_{2f} \sin(2w_o t + \phi_o) \quad (8)$$

$$i_{dif_b} = \frac{I_d}{3} + I_{2f} \sin[2(w_o t - \frac{2\pi}{3}) + \phi_o] = \frac{I_d}{3} + I_{2f} \sin(2w_o t + \phi_o + \frac{2\pi}{3}) \quad (9)$$

$$i_{dif_c} = \frac{I_d}{3} + I_{2f} \sin[2(w_o t + \frac{2\pi}{3}) + \phi_o] = \frac{I_d}{3} + I_{2f} \sin(2w_o t + \phi_o - \frac{2\pi}{3}) \quad (10)$$

Where I_{2f} represents circulating current peak value with twice the frequency as fundamental and I_d is called the total dc current. ϕ_o is defined as initial phase angle and w_o is defined as fundamental frequency. Three phase ‘ac’ components in Eq. 8 to 10 are transformed using negative sequence rotational reference frame to two ‘dc’ components as shown in Eq.13. The transformation matrix using form conversion is given below.

$$T_{acb/dq} = \frac{2}{3} \begin{pmatrix} \cos \theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin \theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{pmatrix} \quad (11)$$

Where $\theta = 2w_o t$, and the a-c-d is the phase sequence of transformation.

Eq.7, rewritten in a-c-b phase sequence is given below.

$$\begin{pmatrix} v_{dif_a} \\ v_{dif_b} \\ v_{dif_c} \end{pmatrix} = L_s \frac{d}{dt} \begin{pmatrix} i_{dif_a} \\ i_{dif_b} \\ i_{dif_c} \end{pmatrix} + R_s \begin{pmatrix} i_{dif_a} \\ i_{dif_b} \\ i_{dif_c} \end{pmatrix} \quad (12)$$

Substituting Eq.8 to Eq.10 in Eq.12 and applying ‘a-c-b’ to ‘dq’ transformation yields.

$$\begin{pmatrix} v_{dif_d} \\ v_{dif_q} \end{pmatrix} = L_s \frac{d}{dt} \begin{pmatrix} i_{2fd} \\ i_{2fq} \end{pmatrix} + \begin{pmatrix} 0 & -2w_o L_s \\ 2w_o L_s & 0 \end{pmatrix} \begin{pmatrix} i_{2fd} \\ i_{2fq} \end{pmatrix} + R_s \begin{pmatrix} i_{2fd} \\ i_{2fq} \end{pmatrix} \quad (13)$$

Here v_{dif_d} and v_{dif_q} represent the unbalance inner voltage difference v_{dif_j} in negative sequence rotational ‘dq’ reference frame at double line frequency. i_{2fd} and i_{2fq} represented in ‘dq’ reference as :

$$i_{2fd} = 1.5 i_{2f} \sin \phi_o \quad (14)$$

$$i_{2fq} = 1.5 i_{2f} \cos \phi_o \quad (15)$$

Eq.13, can be depicted in the form of transfer function as shown in Fig.6.

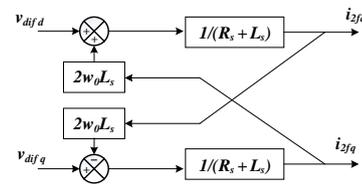


Fig.6. Circulating currents transfer function

Addition of lower and upper arm currents ($i_{lj} + i_{uj}$) generates inner difference current i_{dif_j} as shown in Eq.3 and later they are transformed to negative sequence rotational ‘dq’ reference

frame i_{2f_d} and i_{2f_q} respectively. Circulating currents in 'dq' reference are made zero i.e., $i_{2f_d_{ref}} = 0$ and $i_{2f_q_{ref}} = 0$ to minimize the circulating current. With cross coupling compensation and PI controller, the control signals $v_{dif_d_{ref}}$ and $v_{dif_q_{ref}}$ are obtained as shown in Fig.7. Finally, the unbalance inner difference voltage in 'a-c-b' reference frame is obtained using inner transformation matrix.

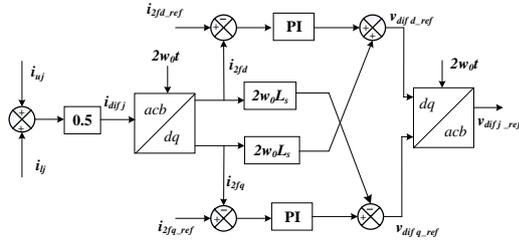


Fig.7. Circulating current suppression control scheme

V. SIMULATION RESULTS

D. Steady state results

Modular multilevel converter (MMC-I) is set to operate at DC voltage control mode at 1 pu and MMC-II is set to operate active power control mode at 60MW and both MMC-I & II operate in reactive power control mode (i.e 0 MVAR). Simulation results depicted in Fig.8, Fig.9 and Fig.10 shown the impact of circulating current suppression control logic. Initially circulating current control is disabled and at time instant of 0.2 sec the control logic is enabled. The inner difference current consisting of 'dc' current and double line frequency circulating current at MMC-I is shown in Fig. 8(a). Before enabling control logic, it can be noticed that inner difference current is peaking on the positive side to 0.13kA and 1.275kA on the negative side. After enabling circulating control scheme, it is observed that current is reduced to 0.28kA on the negative side. Fig.8. (b) and (C) shows phase 'a' currents at MMC-I (upper and lower arm). After enabling control logic, it is noticed that harmonic distortion is reduced, and waveform becomes sinusoidal.

In Fig.8. (d), shows the total upper arm branch voltage including the voltage across the inductor and 'Deblocked' section voltage of upper arm is shown in Fig.8. (e). After enabling circulating current suppression at 0.2sec it is observed that the Total harmonic distortion (THD) is around 1.5%. From Fig.9(a) and (b) it is observed that both real power and reactive power at PCC are stabilised. The phase voltage and current on ac side of MMC-I at terminal 'O' which is the PCC are depicted in Fig.9(c) and (d) respectively. It can be observed that there is no significant change in 'ac' side quantities this makes clear that the control logic has does not affect MMC outer dynamics. After carrying out harmonic analysis on the 'ac' voltage before and after the application of control it is observed that THD of voltage of phase 'a' at PCC is reduced from 8.27 % to 1.17% as shown in Fig.9(c). Similarly, Fig.9(d) depicts the AC current of Phase 'a' flowing through the PCC near MMC-I.

Simulation in real time of MMC-HVDC system with surrogate network topology for MMC valve (along with proposed circulating current suppression control scheme) is

carried out at a time step of 50 μ s and proper steady state results are obtained as shown in Fig.8-9. This surrogate based valve model simulated in RTDS is validated with the dynamic study results from simulation of same MMC-HVDC system in offline platform PSCAD at increased time step.

E. Dynamic study results

To validate the surrogate network topology (along with circulating current controller scheme), a fault on AC side is applied (three phase fault) at PCC (terminal 'O') at 0.11sec and the fault is cleared after 50msec. Then the real time results obtained are compared with simulation results obtained in offline platform for the same contingency as shown in Fig. 10. From Fig.10 it is observed that the real and reactive power through MMC-I are similar in both Realtime and offline simulation. It is also observed from the Fig.10(c) and (d) that the at the positive and negative pole DC voltage are almost similar.

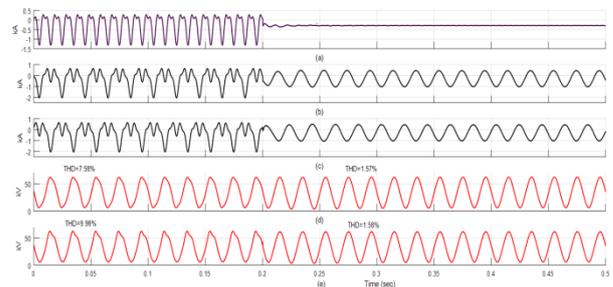


Fig.8. Simulation results of MMC-I before and after enabling control logic. (a) Difference current of Phase 'a'. (b) Phase 'a' Upper arm current. (c) Phase 'a' lower arm current. (d) Phase 'a' upper arm branch voltage. (e) Deblock valve section voltage of phase 'a'.

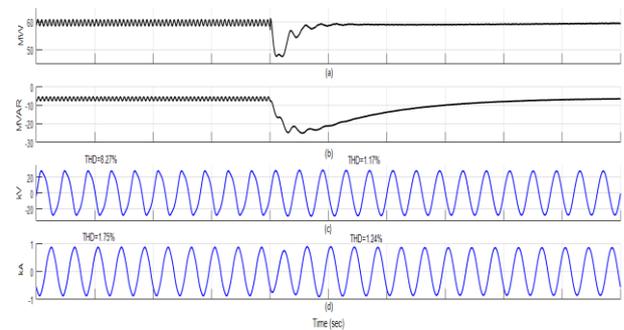


Fig.9. Simulation results of MMC-I before and after enabling circulating current suppression control. (a) Real power flowing through PCC at 'ac' terminal 'O'. (b) Reactive power flowing through PCC at 'ac' terminal 'O'. (c) Ac voltage of phase 'a' at terminal 'O'. (d) AC current of 'a' phase through PCC.

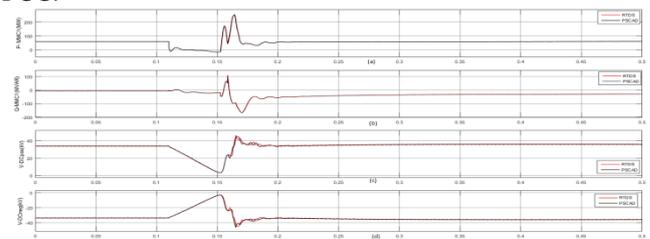


Fig.10. Three-phase AC fault at PCC. (a) P(MW) through MMC-1. (b) Q(MVAR) through MMC-I. (c) DC voltage of positive terminal at MMC-1 end.

(d) DC voltage of negative terminal at MMC-1 end.

VI. CONCLUSION

Simulation of MMC-HVDC system using surrogate network model for HB-SM is carried out in RSCAD software using RTDS simulator. This paper presents how internal voltage balancing in SM capacitors performed using surrogate network. Internal dynamics of MMC are also analysed and the transfer function of circulating current and unbalance inner difference voltages are investigated. Simulation results clearly show the effect of proposed circulating current control logic. With the circulating current reduction it is noticed that not only the inner dynamic performance of MMC is improved but also the converter output voltage quality is also improved.

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