

Small Signal Modeling and Analysis of a Dual Input Interleaved DC-DC Converter



Sivaprasad Athikkal, Kumaravel Sundaramoorthy

Abstract: The idea of DC-DC converter with multi-input is yet to attain a vital role in the field of 'hybrid energy system (HES)' integration and electric vehicle applications. So, the analysis of the dynamic behavior of the multi input converters is crucial in designing a proper controller to achieve a stable performance. This paper reports a 'small signal model (SSM)' and the performance analysis of a 'dual-input DC-DC converter (DIC)'. The parasitic resistances of capacitor and inductor are considered in the modelling. The significant transfer function (TF)s are derived with the help of the SSM, and the Bode plots for the TFs have been obtained. The performance analysis shows that the derived TFs allow better closed loop performance of the system. The simulation of the DIC converter in MATLAB/Simulink® has been carried out and the simulation waveforms are presented. A hardware setup of the DIC converter is fabricated and experimented in the laboratory. The dynamic performance of the DIC is analyzed under the variations in the source and load conditions. The presented converter with a closed loop controller can be used in the applications to formulate a HES with solar-PV, battery, fuel cell, etc. Also the performance comparison of the DIC converter has been performed with other reported converters which shows that the DIC converter has higher efficiency and several other potential merits.

Keywords: Power electronics, multi input DC-DC converters, hybrid energy system, small signal modelling.

I. INTRODUCTION

The non-conventional energy power generation technologies like wind, solar, biomass, fuel cell, etc., are attracted much due to their clean and nonpolluting nature. But, autonomous operation of wind/solar etc., is not recommended due to their highly unpredictable nature. Incorporating sources with diverse voltage - current (V-I) characteristic using the concept of Hybrid Energy System (HES) is generally utilized to satisfy the indigenous energy requirement [1]. Power electronic circuit is a must in the integration of different energy sources [2]. Diversification of various sources is realized by multiple numbers of individual converters in the traditional methods. But, the use of more number of converters to incorporate multiple sources results in difficulty in the overall system design and poor efficiency.

The model of Multiple Input DC-DC Converters (MICs) is introduced to integrate multiple sources. Fig. 1 shows the block diagram of the MIC. These MICs have a simple structure, and lower intricacy [3-6]. The analysis of the converter in dynamic form is so crucial to design an effective control scheme and to obtain better voltage regulation. Thus, the development of a model is essential to understand the behavior of the system during dynamics. By using discrete time models, the dynamic analysis of a system can be performed, but the complexity in the expressions associated with this method may limit its application. Then, continuous time models based analysis is introduced to reduce the complexity with a high accuracy. However, the associated non-linear model does not give an actual idea about the physical process of the converter.

The concept of the small signal model (SSM) is developed to overcome these issues. This method has been widely employed in order to approximate the character of non-linear devices in terms of linear equations. The SSM of the conventional single input DC-DC converters such as buck-boost, buck, boost converters etc., are reported in the literature. The concept of developing SSM of DC-DC converters is described in [6-7]. The idea of average current mode control based on the SSM for the converters operating under Continuous Conduction Mode (CCM) is presented in a detailed manner [8]. The necessity of deriving a SSM and the development of a suitable control strategy depend on the derived SSM for KY converter is explained in [9].

Various small signal modelling concepts for DC-DC converter with bidirectional feature are compared and presented in [10]. The concept of small signal modelling of SEPIC and boost converter are discussed in [11, 12]. Even though the parasitic elements of the converter components are considered, only the peripheral study using the derived SSM is conducted. The analysis of the converter under the source and load side disturbances is not validated with experimental results.

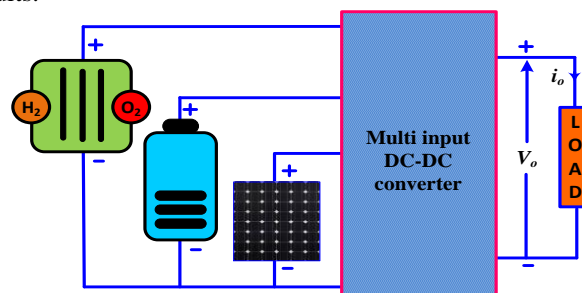


Fig. 1. Block diagram of the MIC.

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The small signal modeling analysis for an interleaved boost converter is reported [13]. The possibility of the controller design to realize fast rejection of disturbances using the derived SSM is discussed. However, the Bode plot and pole-zero analysis are not conducted and the performance of the converter during the source and load side disturbances are not validated experimentally. The concept of SSM for a dual active bridge dc/dc converter is explained [14, 15]. But the detailed discussion on steady state and transient analysis are not presented.

The SSM and related steady state and dynamic analysis of multi input converters are not much reported in literature. A generalized SSM for an open loop multiport dc/dc converter is presented in [16]. The idea of developing a SSM for a double input buck-boost converter is discussed in [17] where, the study on the stability aspects of the presented converter is not explained and the dynamic response of the converter is not analyzed based on the experimental results. The analysis of a non- restricted dual input buck converter based on the SSM is explained in [18].

In this paper, a small signal modelling of a DIC with two input sources is reported. The steady state and dynamic equations that are helpful to interpret the behavior of the converter are also extracted. The analysis of the modes of operation the DIC is carried out based on fixed frequency switching strategy. This paper is structured as follows: After this introduction part, Section II discusses the operating modes of the DIC converter, and Section III presents the SSM of the DIC. Simulation waveforms of the converter are shown in Section IV. The experimental validation of the converter is VI.

II. DUAL INPUT DC-DC CONVERTER

Fig. 2 shows the circuit of the DIC for integrating the HES (solar PV/ wind). The DIC operates in the buck-boost mode. In this converter, the switches are realized by IGBT without an anti-parallel diode. Otherwise, there will be a circulating current when a source with a high voltage is turned on to deliver energy to the inductor L. Here, the power diversification from the input energy sources to the load is controlled by tuning the duty ratios of corresponding power switches S_1 , and S_2 which are associated with the respective sources.

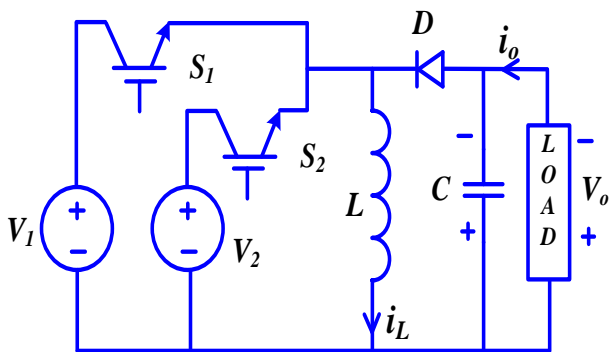


Fig. 2. Structure of DIC converter.

A. Operating States of DIC Converter in CCM

The DIC converter presented in this paper has three modes, i.e., when S_1 - ON, S_2 - ON, and both the switches are OFF in

a single switching cycle. The conduction period for both the semiconductor switches can be determined by the duty ratios computed from the design. The changes in the inductor's current and the voltage due to transition of operating states for one cycle are shown in Fig. 3 (a). The three operating states of DIC converter due to the switching scheme adopted are discussed below.

Mode 1: In mode 1, the device which in conduction is S_1 while the remaining switching devices are in non-conducting state. As shown in Fig. 4 (a), source V_1 charges the inductor.

Mode 2: In mode 2, the device which in conduction is S_2 while the remaining switching devices are in non-conducting state as shown in Fig. 4 (b). Here, source V_2 charges the inductor.

Mode 3: In Fig. 4 (c), both S_1 and S_2 are in non-conduction. Hence, energy present in L is supplied to load and charges the capacitor. In the suggested control strategy, d_1 and d_2 are the duty cycles of the switches S_1 and S_2 subsequently. Hence, the switch S_1 conducts from $0 \leq t \leq d_1T$ (Mode 1) and S_2 conducts from $d_1T_s \leq t \leq (d_1T_s + d_2T_s)$ (Mode 2). Both the switches are turned OFF for the remaining time (Mode 3). The volt - second balance of the inductor is expressed as

$$v_1 d_1 + v_2 d_2 - v_0(1 - d_1 - d_2) = 0 \tag{1}$$

v_1 and v_2 are the input voltages of source 1 and 2 respectively. The output voltage of DIC, " v_0 " from (1) is expressed as:

$$v_0 = \frac{v_1 d_1 + v_2 d_2}{(1 - d_1 - d_2)} \tag{2}$$

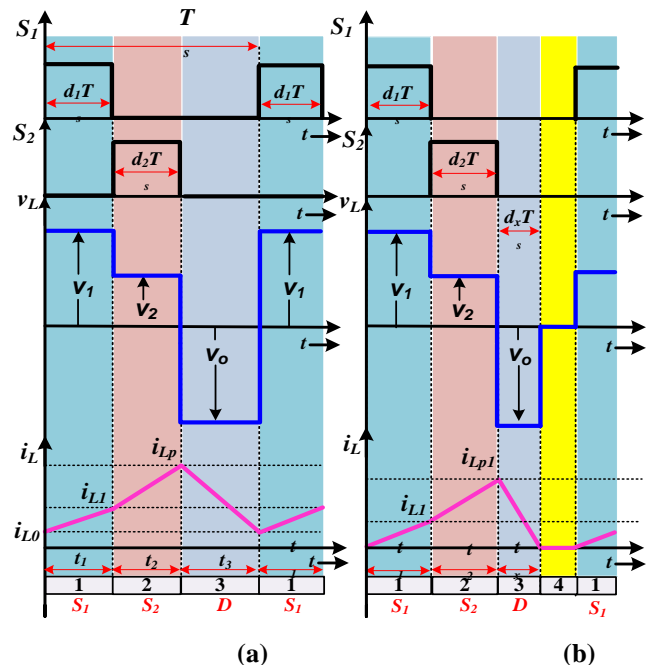


Fig. 3. Analytical waveforms of DIC converter.

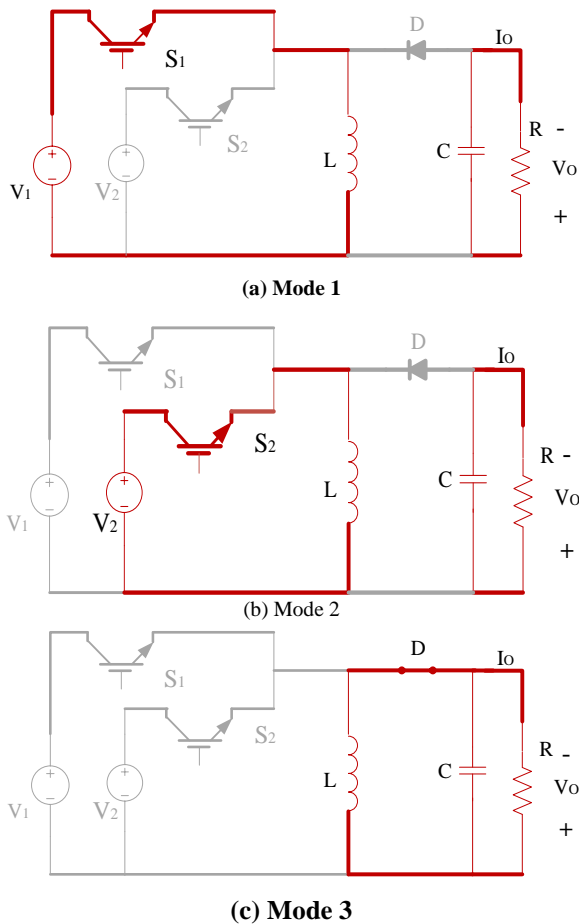


Fig. 4. Various working modes of the DIC converter.

B. Operating States of DIC Converter in DCM

The first two modes of operation of the DIC converter during the DCM are exactly similar to the CCM operation. In mode 3, the inductor L, discharges its stored energy to the capacitor and load till t_x as shown in Fig. 3 (b). When the entire energy is zero, the inductor current become zero. Hence, the inductor current is discontinuous till S_j is turned on. To derive the value of boundary between the CCM and DCM, the value of the input voltages are assumed as $V_2 = a V_1$; $V_1 = V$, where ‘a’ is a scaling factor. During CCM operation, the voltage across the capacitor is expressed as,

$$V_c = \frac{V_1 d_1 + V_2 d_2}{1 - (d_1 + d_2)} \tag{3}$$

The above equation is simplified and the voltage gain of the BDC for CCM operation is given by

$$G_{CCM} = \frac{V_c}{V} = \frac{d_1 + a d_2}{1 - (d_1 + d_2)} \tag{4}$$

Similarly, the voltage gain of the DIC for DCM operation is given by

$$G_{DCM} = \frac{d_1 + a d_2}{\sqrt{2\tau_L}} \tag{5}$$

where, $\tau_L = Lf_s/R$. τ_L is the normalized inductor time constant and R is the resistance of load. From (4) and (5), the expression of the boundary normalized inductor time constant is given by

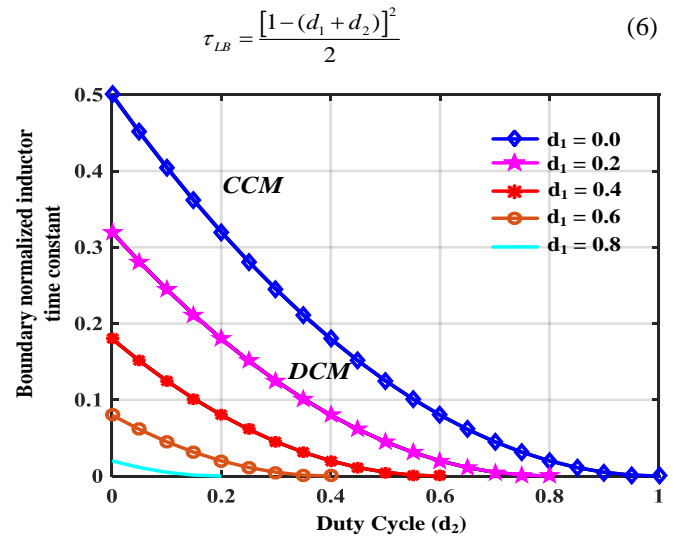


Fig. 5. CCM and DCM boundary conditions of the DIC.

Fig. 5 shows the variation of τ_{LB} with respect to the value of d_1 and d_2 . The converter operates in the DCM when the value of τ_L is less than τ_{LB} .

III. SMALL SIGNAL MOELLING OF THE CONVERTER

Basically, the state space and TF are the two ways of representing the dynamic model of any converter which consists of linear circuit elements like R , L, C and also non-linear circuit elements, called semiconductor switches. But, the circuit derived for each switching operation is a linear circuit. Hence, it is viable to develop a dynamic and output equation for each switching operation. Since, the energy storage elements (L/C) present in the converter are dynamic elements, a dynamic variable is linked to each element. The inductor current and the capacitor voltage are considered as the dynamic variables in this converter model. The dynamic and output equations of the converter for all three modes of operations are expressed below. According to Mode 1 operation, the state equations are written as follows

$$\frac{di_L}{dt} = \frac{v_1}{L} ; \frac{dv_c}{dt} = -\frac{v_c}{RC} \tag{7}$$

In general, the state space representation of any system is expressed as shown in (8).

$$\dot{x}' = A x + B u \text{ and } y = C x + D u \tag{8}$$

From (7) the state space representation of the converter for Mode 1 operation is given as:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [v_1] \tag{9}$$

Output equation is:

$$\begin{bmatrix} v_o \\ i_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{10}$$

where i_g is the source current. From Mode 2 operation:

$$\frac{di_L}{dt} = \frac{v_2}{L} \frac{dv_C}{dt} = -\frac{v_C}{RC} \quad (11)$$

From the above equation, the state space representation is,

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [v_2] \quad (12)$$

Output equation is,

$$\begin{bmatrix} v_o \\ i_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (13)$$

From Mode 3 operation:

$$\frac{di_L}{dt} = -\frac{v_C}{L} \frac{dv_C}{dt} = \frac{i_L}{C} - \frac{v_C}{RC} \quad (14)$$

From the above equation, the state space representation is,

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [v_1] + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [v_2] \quad (15)$$

Output equation is,

$$\begin{bmatrix} v_o \\ i_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (16)$$

A. State Space Average Model of the DIC

The state space average model of the DIC is obtained by cumulating the values of states in three different modes of operation into a single state space model. The final average large signal model state equation of the DIC converter is,

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-d_1-d_2)}{L} \\ \frac{(1-d_1-d_2)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L} & \frac{d_2}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (17)$$

Average large signal model output equation of the DIC is:

$$\begin{bmatrix} v_o \\ i_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ d_1 + d_2 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (18)$$

B. Small Signal Model of the DIC

In (17) and (18), parameters such as duty ratios, inductor and source current, input and output voltages have the steady state and small signal part as given: $d_1 = \bar{d}_1 + D_1$, $d_2 = \bar{d}_2 + D_2$, $v_o = \hat{v}_o + V_o$, $v_1 = \hat{v}_1 + V_1$, $v_2 = \hat{v}_2 + V_2$, $v_c = \hat{v}_c + V_c$, $i_L = \hat{i}_L + I_L$, $i_g = \hat{i}_g + I_g$. By substituting the above values in the average large signal model shown in (17) and (18), the SSM state equation of the DIC converter is:

$$\begin{bmatrix} \dot{I}_L + \hat{i}_L \\ \dot{V}_C + \hat{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D_1-\bar{d}_1-D_2-\bar{d}_2)}{L} \\ \frac{(1-D_1-\bar{d}_1-D_2-\bar{d}_2)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_L + \hat{i}_L \\ V_C + \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{D_1+\bar{d}_1}{L} & \frac{D_2+\bar{d}_2}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 + \hat{v}_1 \\ V_2 + \hat{v}_2 \end{bmatrix} \quad (19)$$

Output equation is:

$$\begin{bmatrix} V_o + \hat{v}_o \\ I_g + \hat{i}_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ D_1 + \bar{d}_1 + D_2 + \bar{d}_2 & 0 \end{bmatrix} \begin{bmatrix} I_L + \hat{i}_L \\ V_C + \hat{v}_C \end{bmatrix} \quad (20)$$

With the following assumptions, i) Neglect $\hat{x}\hat{d}$ (since \hat{x} and \hat{d} are very small perturbations), ii) $\dot{X} = \frac{dX}{dt} = 0$ (because it is a steady state value), (19) and (20) becomes,

$$\begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-(D_1+D_2))}{L} \\ \frac{(1-(D_1+D_2))}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{D_1}{L} & \frac{D_2}{L} & \frac{V_C+V_1}{L} & \frac{V_C+V_2}{L} \\ 0 & 0 & -\frac{I_L}{C} & -\frac{I_L}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_1 \\ \hat{v}_2 \\ \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \quad (21)$$

$$\begin{bmatrix} \hat{v}_o \\ \hat{i}_g \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ D_1 + D_2 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & I_L & I_L \end{bmatrix} \begin{bmatrix} \hat{v}_1 \\ \hat{v}_2 \\ \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \quad (22)$$

C. Small Signal Model of the DIC with Internal Resistances of Inductor and Capacitor

Similarly, the SSM of the DIC has been conducted by including the internal resistance of inductor and capacitor and the variations in the state equation and output equation have been observed. The schematic representation of the DIC converter after incorporating the internal resistance of the capacitor and inductor are shown in Fig. 6. The state and output equation of the converter by considering internal resistances of L and C are derived in a similar manner as explained in (7)-(22). The state and output equation for each mode of operation are given below

Mode 1 operation:

$$\frac{di_L}{dt} = \frac{v_1}{L} - \frac{i_L r_L}{L}, \frac{dv_C}{dt} = -\frac{v_C}{(R+r_c)C} \quad (23)$$

where r_c and r_L are the internal resistance of capacitor and inductor respectively. From (23), the state space representation of the converter is derived as:

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{(R+r_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [v_1] \quad (24)$$

And the corresponding output equation is:

$$\begin{bmatrix} v_o \\ i_g \end{bmatrix} = \begin{bmatrix} 0 & \frac{R}{(R+r_c)} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (25)$$

Mode 2 operation:

Similarly, the state equation and output equation for mode 2 operation has been derived and are given in (26) and (27) respectively.

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{(R+r_c)C} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [v_2] \quad (26)$$

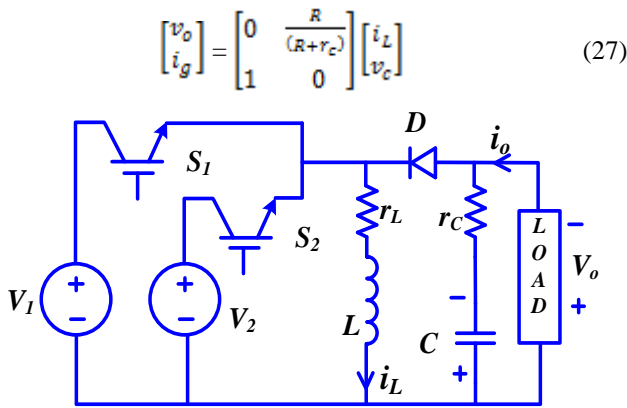


Fig. 4. Structure of DIC converter with internal resistances of capacitor and inductor.

Mode 3 operation:

Finally, the state equation and output equation for the DIC converter with internal resistances of inductor and capacitor (29) respectively,

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{(r_L + R/r_c)}{L} & \frac{R}{L(R+r_c)} \\ \frac{R}{(R+r_c)C} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [v_1] + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (28)$$

$$\begin{bmatrix} v_o \\ i_g \end{bmatrix} = \begin{bmatrix} r_c/R & \frac{R}{(R+r_c)} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (29)$$

The state space average model of the converter under this condition has been derived in a similar method which is explained in (21)-(22), and the final average large signal model state equation and average large signal model output equation are illustrated in (30) and (31).

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{[r_L + \frac{R}{r_c}(1-d_1-d_2)]}{L} & -\frac{R(1-d_1-d_2)}{L(R+r_c)} \\ \frac{R(1-d_1-d_2)}{(R+r_c)C} & -\frac{1}{(R+r_c)C} \end{bmatrix} + \begin{bmatrix} d_1 & d_2 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (30)$$

$$\begin{bmatrix} v_o \\ i_g \end{bmatrix} = \begin{bmatrix} r_c/R(1-d_1-d_2) & \frac{R}{(R+r_c)} \\ d_1 + d_2 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad (31)$$

After deriving the average large signal model, state equation and output equation, the SSM of the converter has been extracted in a similar fashion which is explained in section III (B) (i.e., (19)-(20)). The SSM of the DIC converter with the effect of internal resistances of capacitor and inductor are expressed below. The SSM state equation of the converter after incorporating the small signal perturbations is given in (32).

$$\begin{bmatrix} \dot{I}_L + \hat{i}_L \\ \dot{V}_C + \hat{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{[r_L + \frac{R}{r_c}(1-D_1 - \hat{d}_1 - D_2 - \hat{d}_2)]}{L} & -\frac{R(1-D_1 - \hat{d}_1 - D_2 - \hat{d}_2)}{L(R+r_c)} \\ \frac{R(1-D_1 - \hat{d}_1 - D_2 - \hat{d}_2)}{(R+r_c)C} & -\frac{1}{(R+r_c)C} \end{bmatrix} \begin{bmatrix} I_L + \hat{i}_L \\ V_C + \hat{v}_C \end{bmatrix} + \begin{bmatrix} D_1 + \hat{d}_1 & D_2 + \hat{d}_2 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 + \hat{v}_1 \\ V_2 + \hat{v}_2 \end{bmatrix} \quad (32)$$

Similarly the SSM output equation is derived as given below.

$$\begin{bmatrix} V_o + \hat{v}_o \\ I_g + \hat{i}_g \end{bmatrix} = \begin{bmatrix} \frac{R}{r_c}(1-D_1 - \hat{d}_1 - D_2 - \hat{d}_2) & \frac{R}{(R+r_c)} \\ D_1 + \hat{d}_1 + D_2 + \hat{d}_2 & 0 \end{bmatrix} \begin{bmatrix} I_L + \hat{i}_L \\ V_C + \hat{v}_C \end{bmatrix} \quad (33)$$

Here also by taking the assumptions, i) Neglect $\hat{x}\hat{d}$ (since \hat{x} and \hat{d} are very small perturbations), ii) $\dot{X} = \frac{dX}{dt} = 0$ (because it is a steady state value), (32) and (33) become,

$$\begin{bmatrix} \dot{I}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -\frac{[r_L + \frac{R}{r_c}(1-(D_1+D_2))]}{L} & -\frac{R(1-(D_1+D_2))}{L(R+r_c)} \\ \frac{R(1-(D_1+D_2))}{(R+r_c)C} & -\frac{1}{(R+r_c)C} \end{bmatrix} \begin{bmatrix} I_L \\ v_C \end{bmatrix} + \begin{bmatrix} D_1 & D_2 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 + R \frac{(r_c I_L + V_C)}{L(R+r_c)} \\ V_2 + R \frac{(r_c I_L + V_C)}{L(R+r_c)} \end{bmatrix} + \begin{bmatrix} \hat{v}_1 \\ \hat{v}_2 \\ \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \quad (34)$$

$$\begin{bmatrix} \hat{v}_o \\ \hat{i}_g \end{bmatrix} = \begin{bmatrix} \frac{r_c}{R}(1-(D_1+D_2)) & \frac{R}{(R+r_c)} \\ D_1 + D_2 & 0 \end{bmatrix} \begin{bmatrix} I_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 & 0 & -\frac{r_c}{R} I_L & -\frac{r_c}{R} I_L \\ 0 & 0 & I_L & I_L \end{bmatrix} \begin{bmatrix} \hat{v}_1 \\ \hat{v}_2 \\ \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \quad (35)$$

The expression of the TF (output voltage to duty ratio) of DIC converter for the buck-boost operation is derived from the SSM as given in (36).

$$\frac{\hat{v}_o}{\hat{d}}(s) = K_{vd} \frac{(1 - \frac{s}{w_{rhp}})}{1 + \frac{s}{Qw_0} + \frac{s^2}{w_0^2}} \quad (36)$$

Here, K_{vd} is the constant gain of the converter, Q is the damping ratio, w_0 is the pole frequency and w_{rhp} is the frequency corresponding to the right hand plane pole. The expression of the TF (Input current to duty ratio) of DIC converter for the buck-boost operation is derived from the SSM as given in (37).

$$\frac{\hat{i}_g}{\hat{d}}(s) = K_{id} \frac{(1 + \frac{s}{w_{id}})}{1 + \frac{s}{Qw_0} + \frac{s^2}{w_0^2}} \quad (37)$$

where, K_{id} is the constant gain of the converter and w_{id} is input current zero frequency, Q is the damping ratio and w_0 is the pole frequency.

From the above TFs, it is possible to observe the pole-zero and Bode plot of the system to analyze the system stability. Depending upon the SSM and TF derived, the frequency response has been verified in MATLAB platform. The Bode plots corresponding to the TFs $P_{V\partial_1} = \frac{v_o}{d_1}(s)$ and $P_{I\partial_2} = \frac{i_1}{d_2}(s)$ are shown in Fig. 7. From the Bode plot, it can be observed that, the phase margin is 90° . Hence, in this condition, an additional phase shift of 90° can be provided so that the system can be on the verge of stability.

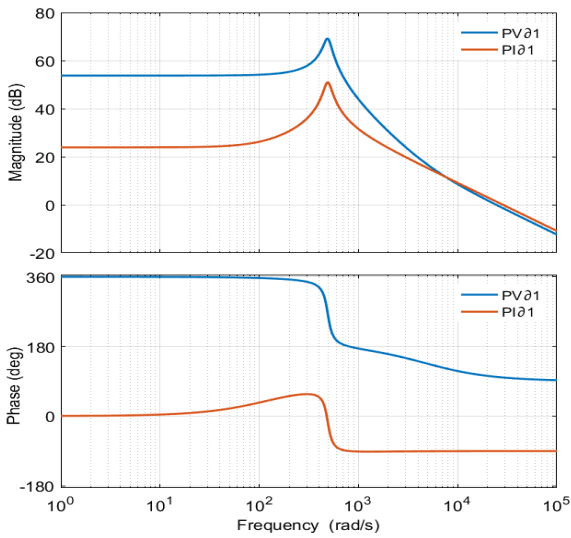


Fig. 7. Bode plots for TFs (a) $\frac{v_o}{d_1}(s)$ (b) $\frac{i_1}{d_1}(s)$

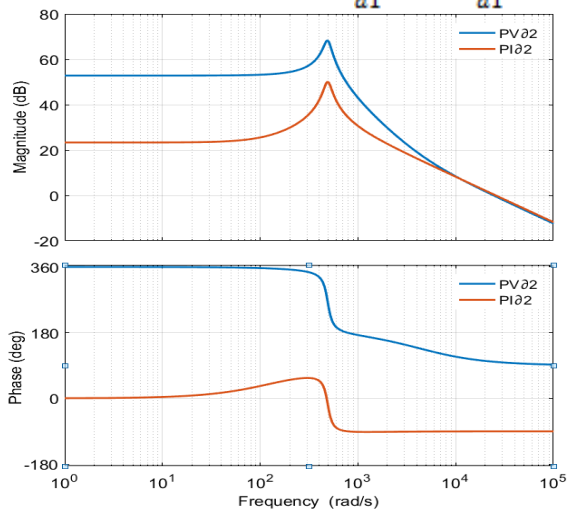


Fig. 8. Bode plots for TFs (a) $\frac{v_o}{d_2}(s)$ (b) $\frac{i_1}{d_2}(s)$

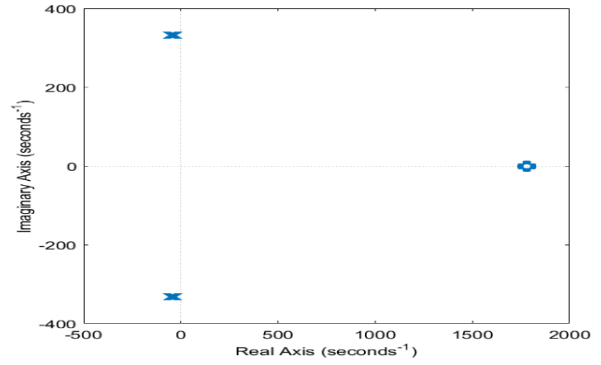


Fig. 9. Pole-zero representation of the TF model.

The Bode plots corresponding to the TFs $P_{V\partial_2} = \frac{v_o}{d_2}(s)$ and $P_{I\partial_2} = \frac{i_1}{d_2}(s)$ are shown in Fig. 8. The Bode plot shows that, the system is always stable since its magnitude plot is not crossing the zero dB line and phase plot is not crossing the 180° line. The pole-zero plot obtained from the TF model is shown in Fig. 9. From the plot, it can be observed that, the buck-boost converter discussed in the paper has a Right Hand Plane zero (RHP zero).

Usually, such types of system can be referred as non-minimum phase system. Since there is a presence of RHP zero, the overall open loop phase angle may drop to a sufficiently lower value, which may cause an unstable operation of the converter. Hence, the RHP zero is undesirable. The effective way to solve this problem is to move the RHP zero to higher frequencies while reducing the bandwidth of open loop gain plot to lower frequency. Then, the presence of RHP zero cannot affect the overall loop significantly. This analysis helps to design a suitable PI controller. A PI controller is designed for the proposed DIC converter to regulate the output voltage under load and source side disturbances.

IV. SIMULATION RESULTS

The simulation of the DIC is performed in MATLAB for both open and closed loop conditions. The results are verified for the CCM and DCM of the converter. The switching frequency of the converter is taken as 20 kHz. The simulation has been carried out by considering ideal components in the converter. The duty cycles of 0.37 and 0.37 are considered for the switches S_1 and S_2 respectively. The parameters of different components considered in the simulation are shown in Table I. The waveforms from the various parts of the circuit attained from the simulation of the DIC converter are illustrated in Fig. 10 (a). The figure shows that the variation of inductor voltage with respect to input source voltages V_1 , V_2 and the output voltage V_o . When the switch S_1 is ON, the inductor current changes from I_{L0} to I_{L1} . Similarly, when the switch S_2 is ON, the inductor current changes from I_{L1} to I_{Lp} .

When both the switches are OFF (Mode 3), the current through the inductor changes from I_{Lp} to I_{L0} . The buck operation of the DIC is verified by considering the duty ratios of 0.2 and 0.2 respectively for d_1 and d_2 . Here, the value of the load resistance is considered as 400Ω .

Fig. 10 (b) shows the simulation waveform of DIC converter for the buck operation. The simulation waveforms of the output voltages during the boost and buck operation of the DIC converter match with the theoretical values obtained using (2). The DCM operation of the DIC converter is verified for the same duty ration for the normalized inductor time constant of 0.15 and the corresponding value of load resistance is 1332 Ω . The DCM operation for the above parameters is verified in simulation and the output waveforms are shown in Fig. 10 (c).

Table- I: Simulation Parameters

Parameters	Specification
Source voltage V_1	150 V
Source voltage V_2	120 V
Duty ratio d_1	30 %
Duty ratio d_2	40 %
Inductor (L)	5 mH
Capacitor (C)	100 μ F
Switching frequency (f_s)	20 kHz
Output voltage (V_0)	400 V
Load	150 Ω

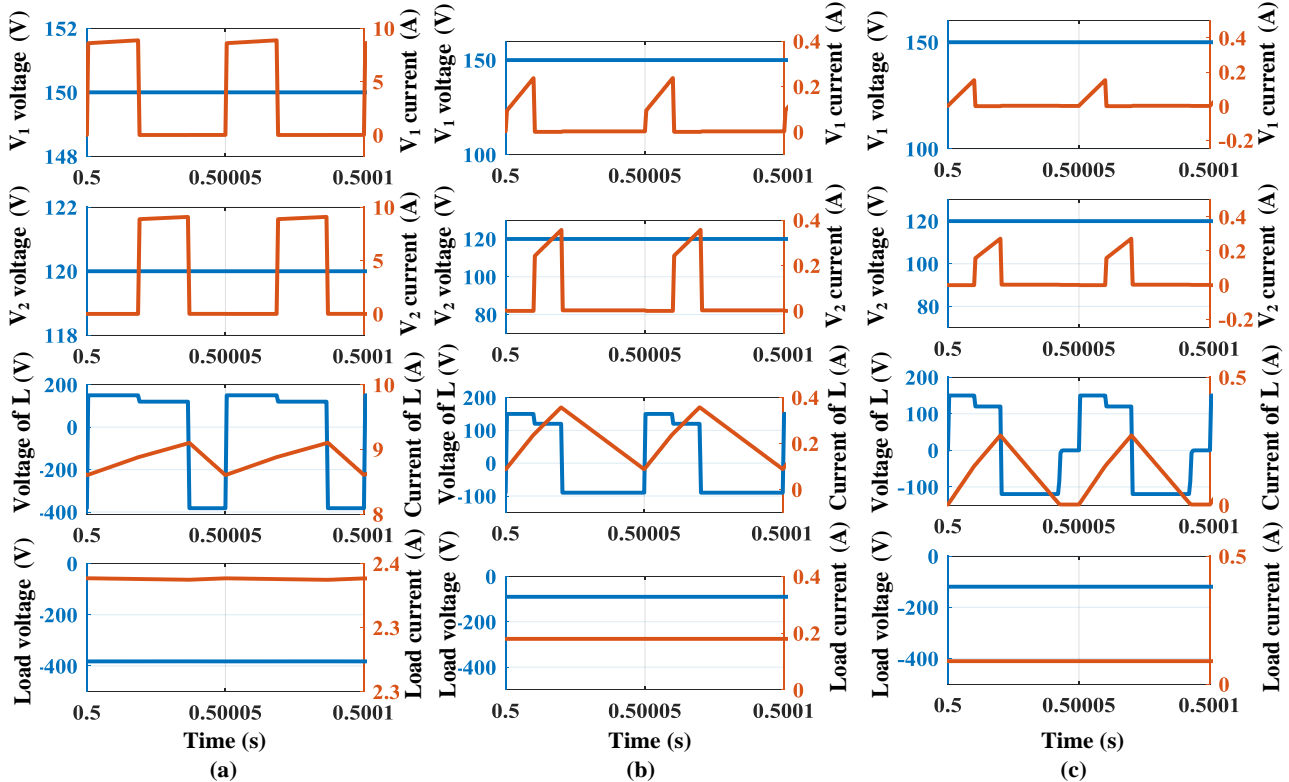


Fig. 10. Waveforms attained from the simulation of the DIC converter in buck-boost mode of operation: (a) DIC converter in CCM with boost (b) DIC converter in CCM with buck (c) DIC converter in DCM

V. EXPERIMENTAL RESULTS

A small scale experimental setup of the DIC has been fabricated and tested in the laboratory to verify the performance of the converter. The developed experimental setup is shown in Fig. 11. The fabricated converter is tested by considering two input sources V_1 and V_2 where $V_1 \neq V_2$. The controller for DIC converter is developed in the LabVIEW platform and the real-time interfacing is realized through NI cRIO-9081@ hardware with NI 9401 digital input/output module. In order to sense and measure the output current and voltage, NI 9227 and NI 9225 modules are used.

The waveforms of switching pulses, source currents, inductor current, inductor voltage, output current and voltage of the DIC under steady state condition are observed from the experiments and are also reproduced in Fig. 12. From the Fig. 12 (e), it can be seen that, the current of the inductor is initially increasing for the duty cycle d_1 , and for a short duration of the period after d_1 , the inductor is tending to discharge since there is a small delay between two switching pulses. The inductor current again increases with the

beginning of next duty cycle d_2 and finally discharges for a period of $1-d_1-d_2$. From these experimental waveforms, it can be observed that, the results obtained from the experimental setup are closely accorded with the simulation results. By comparing the experimental and simulation results it is clear that, the experimental results may slightly deviate from simulation results due to the drops of switches and diodes considered in the experimental setup whereas simulation is carried out by considering only the ideal components.

To assess the dynamic response of the DIC during a disturbance in both the source and load sides, a transient analysis is carried out and the results are shown in Fig. 13. A PI controller is designed using the stability analysis for the regulation of the output voltage under dynamic conditions.

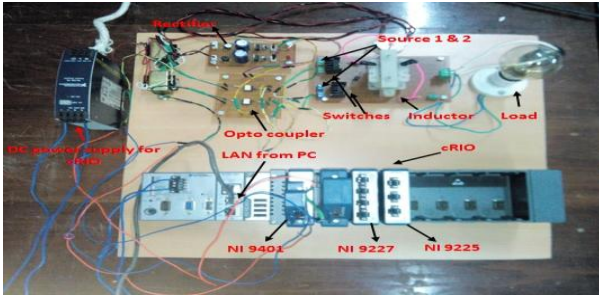


Fig. 11. Experimental prototype of the DIC converter.

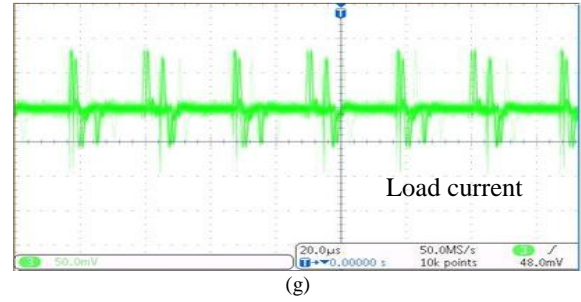
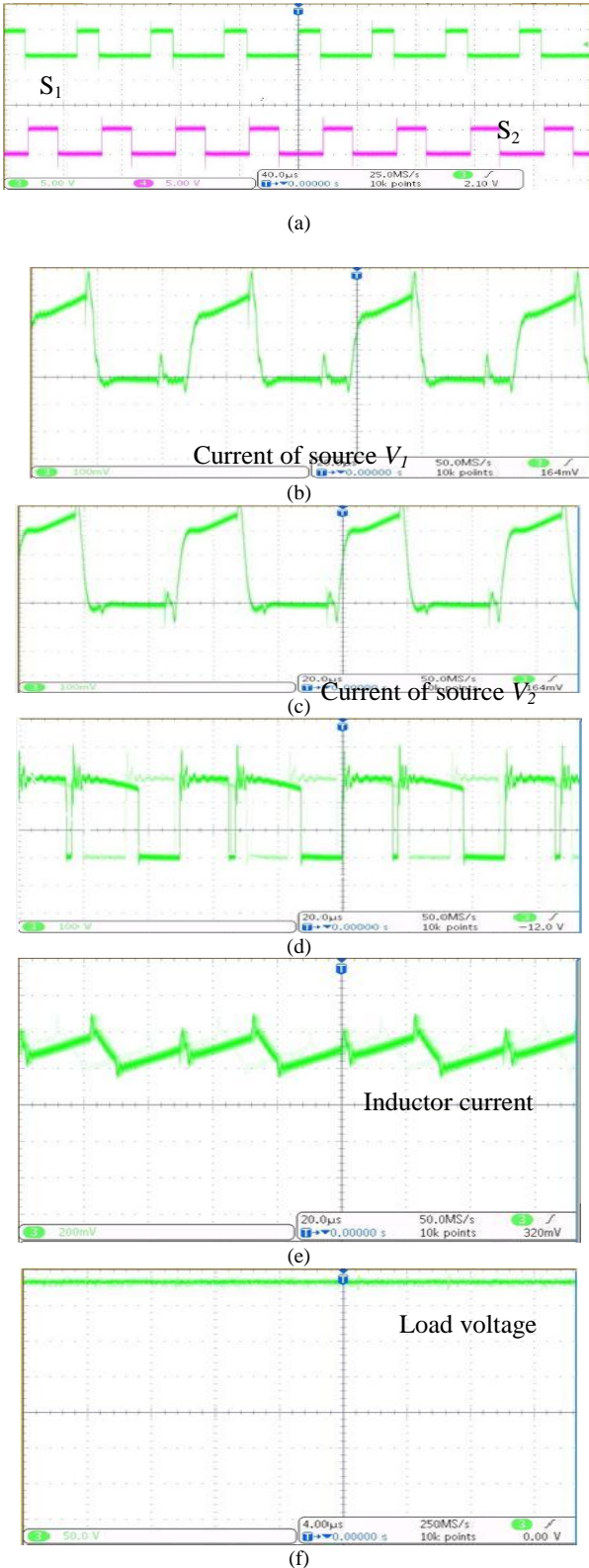
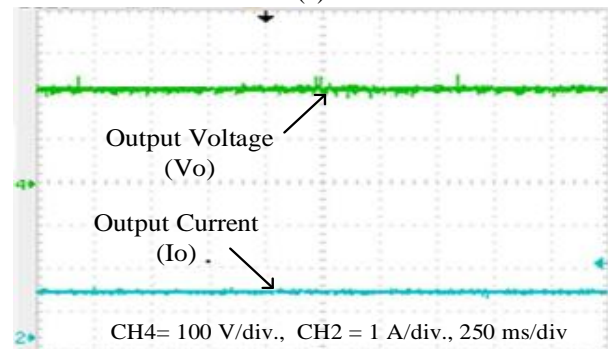
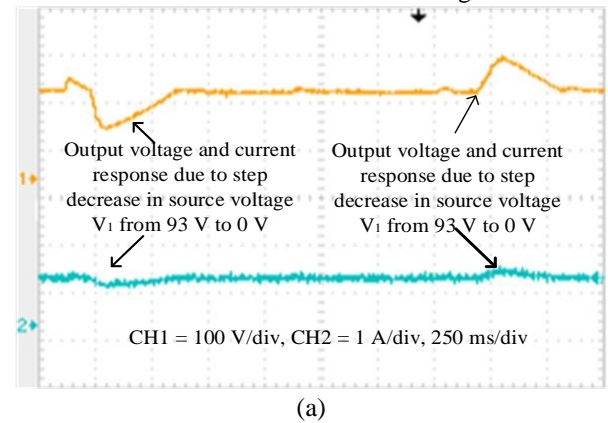
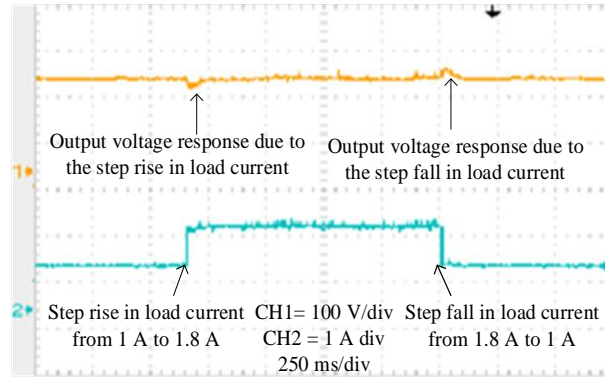


Fig. 12. Experimental waveforms (a) Pulses for switches S_1 and S_2 (b) Source current I_1 (c) Source current I_2 (d) Inductor voltage (e) Inductor current (f) Output voltage (g) Output current for $V_1=93\text{ V}$ and $V_2=91\text{ V}$, $d_1=0.3$ and $d_2=0.4$.

Initially, the output current and output voltage waveforms have been observed without any variations in the load or source as shown in Fig. 13 (a). Then, the response of the voltage and current of the load is noticed by incorporating sudden changes in the load as given in Fig. 13 (b). The converter output voltage is maintained at 200 V during the sudden variation in the output current from 1 A to 1.8 A as shown in Fig.13 (b). When the output current is decreased from 1.8 A to 1 A, the load voltage of the converter is returned to 200 V within a short time. Similarly to check the performance of the DIC converter for variation in the source conditions, a large perturbation is applied in source voltage V_1 . As shown in Fig. 13 (c), the perturbation is applied in the source 1. Firstly, the DIC is functioned with V_1 and V_2 for a short time span. Quickly source 1 (V_1) is dropped to zero (a rapid change in source 1 from 93 V to 0 V) and the minor deviation is detected in load current and voltage.





(c)

Fig. 13. Experimental waveforms of the DIC converter (a) During no changes in load or source (b) during varying load condition (c) during varying source condition.

Table-II: Comparison of DIC Converter with other reported converters

Topology	Inductor (L)	Capacitor (C)	Switches	Voltage stress (V)	Efficiency (%)	Modes
Converter in [3]	N	1	2N	V_o	78-88	BD, B
Converter in [5]	2	4	N+3	V_N	75-90	UD,B
DIC Converter	1	1	N+1	V_N-V_{N-1}	85-94	UD, B-B

BD: bidirectional, UD: unidirectional B:boost,B-B: Buck-boost

Likewise, the source 1 is restored (i.e., a sudden change in V_I from 0 V to 93 V) after a short period of time, and resultant output current and voltage response are noticed. The output current and voltage retain at their requisite values even after small deviations. So, it is observed from Fig. 13 (b-c) that though the variations are present in source and load values, the output voltage of the DIC is well retained at the required voltage rapidly. So, the experimental study on transients of DIC demonstrates the efficiency of the controller designed.

The comparison of DIC converter with the reported topologies is carried out with the parameters like count of diodes and IGBTs, efficiency, voltage stress etc. Table II summarizes comparison of the DIC converter with existing. From the results, it is noticed that the presented converter have numerous merits like lesser component count, lesser voltage stress, and higher efficiency.

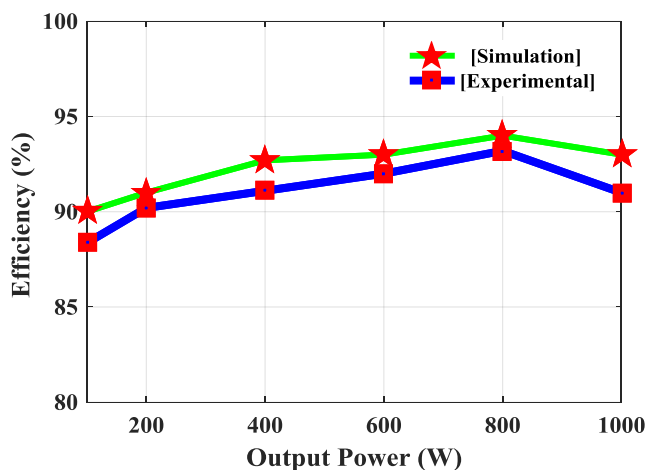


Fig. 14. Efficiency profile of the DIC converter

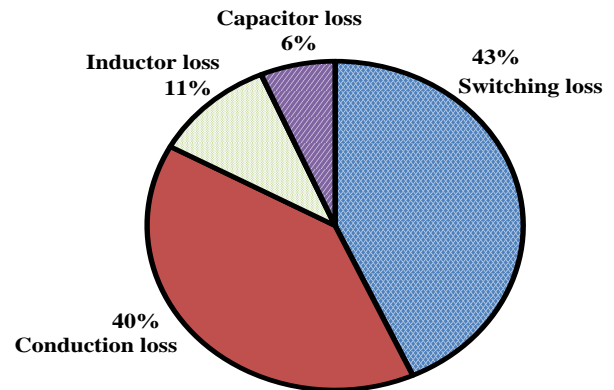


Fig. 15. Loss break-down analysis

The performance analysis of the DIC is verified in terms of the efficiency and loss break down. Fig. 14 shows the efficiency profile of both the simulation and experimentation. The figure proves that the converter can be operated with the maximum efficiency of approximately 94%. The detail loss breakdown analysis has been conducted to assess losses due to switches, diode, capacitor and inductor and Fig. 15 shows the wheel diagram of various losses of the DIC converter for the rated power of 1000W. The conduction and switching losses share the major portions. By designing a proper capacitor across the power semiconductor switch, a zero voltage switching can be achieved; hence, the switching loss can be brought down further.

VI. CONCLUSION

The small signal model for a DIC converter by state space averaging method is presented by considering the internal resistance of the capacitor and inductor to get a more accurate SSM. Depending upon the developed SSM, the TF of the converter is derived and the dynamic behavior of the DIC is analyzed using the pole-zero and Bode plot analysis.

From the analysis, it can be concluded that, the SSM of the converter is helpful to design a suitable controller to achieve stable performance. The simulation and experimental results confirm the effective operation of the DIC. From the experimental outcomes, the response of the converter during dynamic and steady state operations is found acceptable. The results show that the output voltage remains in the desired level with good regulation. The performance comparison of the DIC with the reported topologies has been conducted. Developed SSM by considering the parasitic resistance of the DIC converter and the stability analysis are the novel contribution of this paper. From the overall performance analysis of the DIC converter, it shows that the presented topology is well suited for hybrid energy applications.

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