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Fault Protection Enabled Gate Drive Circuit for 3-Phase Inverter

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Abstract*: Asynchronous motors used in applications like electric vehicles require protection against all possible fault conditions like short circuit, over voltage, over current etc., for their reliable operation. 3-phase inverter is used as power modulator for induction motor. In this paper a novel fault protection scheme is implemented for inverter used in modulating voltage and frequency of power supply driving 3-phase Induction Motor. Function of gate drive circuits used in power electronics converters is to provide isolation for gate signals and shift the voltage level of gate pulses to the required level to enable turn on and turn off the switches as desired. Gate signals are generated using Texas instrument F28069M board. Level shifting is achieved by buffer ICs and fault protection is provided by enabling shut down pin in the DSP on occurrence of fault. Hardware results show that modulation index of gate signals is set to zero under fault conditions and ensure total safety of Inverter driver circuit and power circuit used in the Inverter.

Keywords: Induction Motor, Inverter, gate drive circuit, F28069M, St-embed

I. INTRODUCTION

Three phase Inductions motors are widely used in applications like electric vehicles which require precise control. Advances in technologies like power electronics, Integrated circuits, digital signal processors and control systems have provided the strength of precise and real time control to Induction motors [1]-[2]. Techniques like Vector control have further strengthened the motors, which provide decoupled control as that of a separately excited DC motor. Response of the motor for transients like starting, speed reversal, etc., are improved by implementing vector control schemes [3] - [4]. Here along with the magnitude of current space vector position also considered in control scheme. This can be achieved by suitably controlling output voltage and frequency of three phase inverter [5]-[6]. The digital signal processor used for the control should have six pulse width modulation output pins, analog input pins to receive the feedback current and voltage signals from the motor [7]. Power switches for the inverter are selected based on the requirements like switching frequency and power rating.

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For high power and low frequency operation power thyristors are used. But the use of thyristors requires additional arrangements for commutation. For high frequency and low power applications MOSFETS are used.

In high power and moderate switching frequency requirements IGBTs are used. Both MOSFET and IGBTs are voltage-controlled devices which can be easily turned off by setting the level of gate signals to zero and they do not require additional commutation circuit. IGBT used in the present work can be turned on by applying 15V between gate and emitter terminals and turned off by applying 0V. The F28069M processor used in the work gives gate pulses at a level of 3.3V. An additional driver circuit is required to shift the voltage level of gate pulses to 15V. F28069M also has an active low shutdown pin. This pin will be at 3.3 V under normal working conditions. PWM output can be forced to zero modulation index by setting voltage level at shut down pin to zero. It is important to identify the reason for shutdown of inverter, as shutdown is possible due to interruption in power supply. To confirm the turn off of the inverter due to the occurrence of fault, fault detector circuit is developed in which indicators like light emitting diodes continue to glow after shut down of inverter. Power supply for this fault detection circuit can be provided either by uninterruptible power supply or battery to ensure the operation fault indicator upon interruption in utility power supply.

II. VOLTAGE AND FREQUENCY CONTROLLED INVERTER

Stator voltage controlled three phase induction motor will not fit the requirements of applications requiring constant torque output. This type of control only suits applications with low starting torque requirement and narrow range of speed control at high speed range. By maintaining voltage to frequency ratio constant, maximum torque output can be maintained constant and slip for maximum torque varies with change in frequency. By varying voltage and frequency of inverter output both torque and speed of the motor are controlled [8]-[9]. In the present paper hardware implementation of open loop frequency and voltage controlled 3 phase induction motor drive is explained. The entire drive can be divided into power circuit and control circuit. Power circuit mainly consists of rectifier and inverter circuits. The power semiconductor devices used are power diodes and IGBTs. Uncontrolled 3 phase bridge rectifier converts available utility supply into DC voltage. A capacitor is connected to output of the rectifier in parallel to maintain the bus voltage stable. A rheostat is connected in series with capacitor to limit the initial inrush current drawn by the capacitor.

As the capacitor charges 80% of the rated DC bus voltage, rheostat is set to minimum position. DC voltage from rectifier output is applied to 3-phase full bridge inverter. A 3HP three phase induction motor is driven from the inverter. Circuit diagram of power circuit is shown in figure 1. To implement 3 phase rectifier and Inverter Semikron stack is used. Stack consists of 4 SKM75Gb12T4 IGBT modules, 4 Skyper 32 R IGBT Drivers, Electrolytic capacitor, One Fan, IGBT Snubbers, Busbar and Thermal Trip etc required in implementing the power circuit.

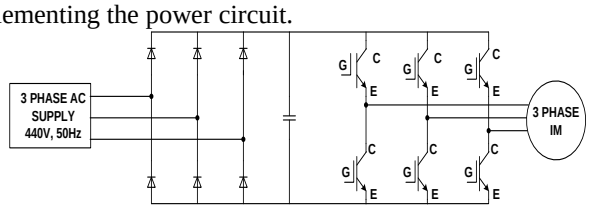

Figure 1. Circuit diagram of power circuit

Gate voltage signals required to control IGBT switches are generated. Launchxl F28069M C2000 piccolo board is used in the generation of gate signals for three phase IGBT Inverter. Generated gate signals are of 3.3V level which needs to be converted to 15V level signal. Block diagram of level shifting and fault protection circuit developed is shown in the figure 2.

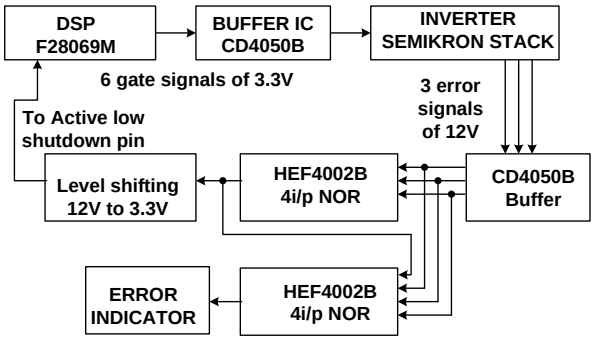

Figure 2. Block diagram of Gate drive for Semikron Stack

Figure 3 shows the board developed for gate drive of IGBT based 3 phase inverter.

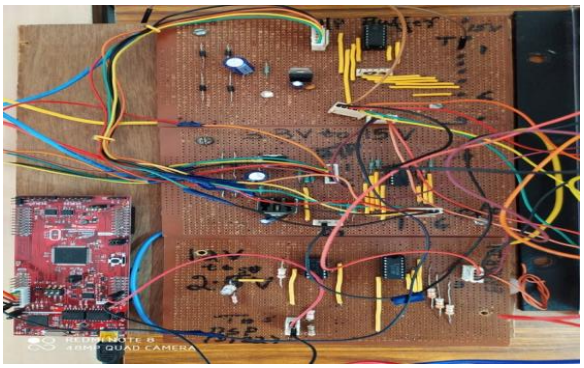

Figure 3. Hardware implementation of gate drive circuit

Non- inverting high voltage open collector buffer IC 7417N and buffer IC CD 4050B are used. Maximum power supply voltage (V_{CC}) for 7417N IC is 7V. Minimum input voltage for CD 4050B is 5V and maximum power supply voltage is 20V. So, two ICs 7417N and CD 4050B connected in cascade fashion are used to shift the input 3.3V level signal to 15V level signal. Power supply of 5V is used for 7417N IC and pull up resistors of 1kΩ are connected to 15V supply. These signals of 15V level are connected to input pins of CD4050B.Power supply voltage for this IC is 15V. Output of CD4050B is connected to IGBT gate pins and ground terminal is connected to emitter pin of IGBT. Hence this level shifting requires power supply of two different levels i.e.5V and 15V. These power supplies are built by using 230/12V, 2A single phase transformer, diode rectifier, voltage regulation ICs like 7815 and 7805. Heat sink is provided to voltage regulator 7805 as power dissipation in IC 7805 is more compared to IC 7815.

III. FAULT PROTECTION CIRCUIT

For the protection of developed drive system, it required to develop fault protection and fault indictor circuits. Logic used in these circuits is shown in figure 4.

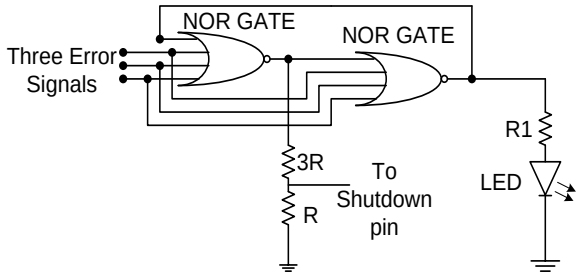

Figure 4. Logic used in Protection circuit

4 leg Semikron stack has one error pin for each leg consisting of two IGBTs. The internal Skyper driver circuit used in Semikron stack produces error signals upon occurrence of fault like short circuit, overloading and when power supply to driver circuit becomes less than 13.5V. The level of error signal is 12V. A buffer IC CD 4050B is used to isolate error signal from processor F28069M. In order to protect the power circuit and driver circuit from fault, the output of error pins passed through buffer used in shutting down of PWM signals from digital signal processor. The shutdown pin used in F28069M processor is active low pin, which will be at a voltage of 3.3V under normal operating conditions. In order to enable shutdown voltage level of shutdown pin need to be reduced to zero. This logic can be achieved by using 4 input NOR gate IC HEF 4002B IC. After buffering, the three error signals are connected to input pins of the NOR gate. Fourth input is connected to ground. Using the suitable voltage divider circuit 12V NOR gate output is reduced to 3.3V level. When fault occurs in any of the inverter leg or all inverter legs, PWM output from DSP are shutdown, resulting in total protection of drive system. To indicate the occurrence of fault to the user, a fault indicator circuit is developed. Second input of NOR gate present in IC HEF 4002B is used in implementing fault indicator circuit. Fourth input for NOR gate used in fault protection circuit is from the output of fault indictor circuit. Inputs to the NOR gate used in fault indicator circuit are output of fault protection NOR gate and three error signals from buffer IC. This NOR gate output is connected to a LED through a resistor of suitable value connected in series.

When fault indicator circuit is used along with fault protection circuit, on fault conditions PWM outputs of DSP are shut down and fault is indicated by the LED. This fault protection and indicator circuits continue to provide shutdown and fault indicator signals upon clearance of fault. To clear the signals, the entire driver circuit need to be reset. This will ensure the user that shutdown of the inverter is due to fault and not due to any other reason like interruption in the power supply to inverter. This will stop the user from turning on Inverter without clearing the fault.

IV. PWM GNERATION IN ST-EMBED

Three phase inverter requires six gate voltage signals to control six IGBT switches of Semikron stack. These PWM signals are generated in the St-Embed domain. ePWM block in St-Embed need to be properly configured to generate the required gating signals. Figure 5 shows the ePWM properties block used to configure gate signals for inverter.

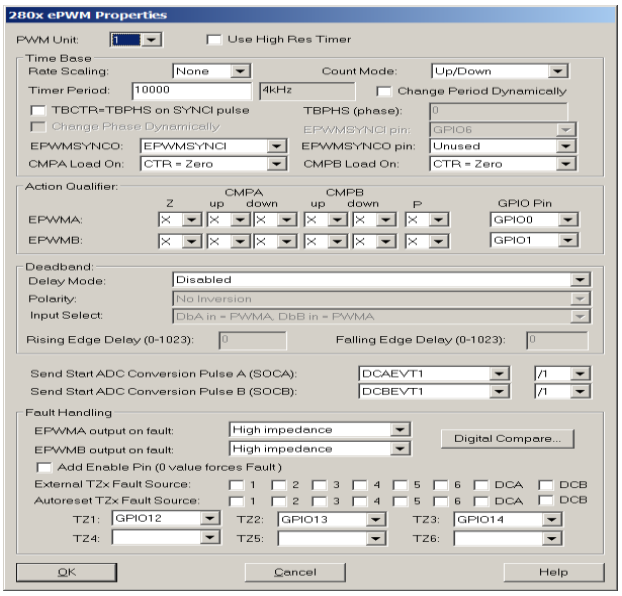

Figure 5. Properties of ePWM block [10]

Enhanced PWM block has several sub sections used to configure different aspects of PWM. Different modules used are Time-Base, Action Qualifier, Dead-Band and fault handling. By using time base sub module one can define PWM frequency, synchronize multiple ePWM modules, configure the time-base counter to count-up, down, or count-up-and-down mode. Events like CTR = PRD or CTR = Zero are used to change the state of PWM signals from both low to high and high to low. Rate of the time-base clock is set by pre scaling CPU system clock. One ePWM block can generate two gate signals. Hence three ePWM blocks which are synchronized with each other are used. For low frequency range, time base rate scaling is set to 1/16. Counter mode is set to up/down mode and change period dynamically option is enabled to change the frequency externally to the block. For synchronizing three ePWM blocks, TBCTR=TBPHS on SYNCI pulse option is enabled. Six PWM signals are generated using three ePWM blocks. Each PWM signal is set to have a phase difference of 60 degrees with respect to its previous and next PWM signals. Two EPWM signals, EPWMA and EPWMB are set to have a phase difference of 180 degrees by configuring the action qualifier. Synchronized second ePWM block EPWMA is required to produce a phase shift of 60 degrees with respect to EPWMA of first ePWM block. This can be set by enabling the option change phase dynamically. Change phase dynamically option will produce an external pin and by setting it to a fractional value 0.33 which will get multiplied with time period and gets assigned to TBPHS register producing a phase difference of 60 degrees. Third ePWM block is synchronized to second ePWM block and by setting same values for phase shifting, will produce EPWMA having phase difference of 120 degrees. EPWMB signals of ePWM1, ePWM2 and ePWM3 blocks will have a phase difference of 180,240 and 300 degrees respectively. General purpose input/output pins GPIO0 to GPIO5 are used as PWM output pins in action qualifier module. A dead time between rising and falling edges of EPWMA and EPWMB are set dead band generate module. Rising edge delay and falling edge delay on EPWMA and EPWMB signals respectively is configured. A dead time of 2 micro second is provided for the safe operation of the inverter. In fault handling module external trip zone fault source 1 is set. This signal is received from GPIO12 pin [10] - [12].

To implement voltage and frequency variation keeping their ratio constant an analog input pin in F28069M board is made use. The input to the analog input is controlled using adjustable voltage divider like potentiometer. The value of both voltage and frequency are directly proportional to analog input signal received keeping V/F ratio constant. The analog input is scaled appropriately before connecting it to input pins controlling modulation index and frequency of ePWM block output [13]-[15].

V. RESULTS AND DISCUSSION

Figure 6 shows the hardware implementation of gate drive circuit and three phase inverter. Figure 7 shows the motor drive circuit used to operate 3HP three phase induction motor. Figures 8, 9 and 10 shows the three PWM signals with different values of frequency and duty ratio. These PWM signals are generated from PWMA output of ePWM blocks. PWM signals generated from PWMB output of ePWM blocks are phase shifted by 180 degrees compared to corresponding PWMA outputs. These PWMB signals are used to drive lower switches in the inverter. Waveforms shown in figure 9 and figure 10 shows that duty ratio and frequency of ePWM outputs can be varied keeping the ratio V/F almost constant. Speed of the motor increased from 460 RPM to 1365 RPM by changing duty ratio and frequency of PWM signals as shown in figures 9 and 10.

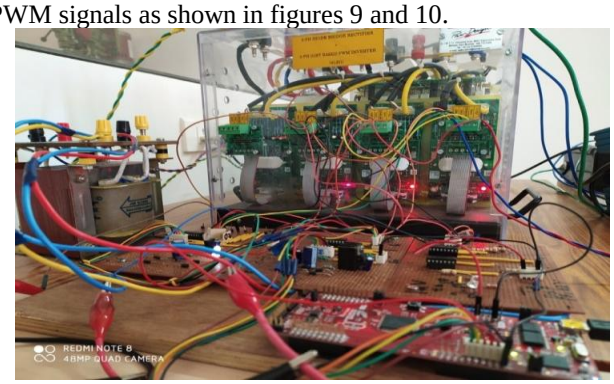

Figure 6. Hardware implementation of 3 phase inverter

Figure 7. Hardware implementation of 3 phase inverter driving 3 phase IM

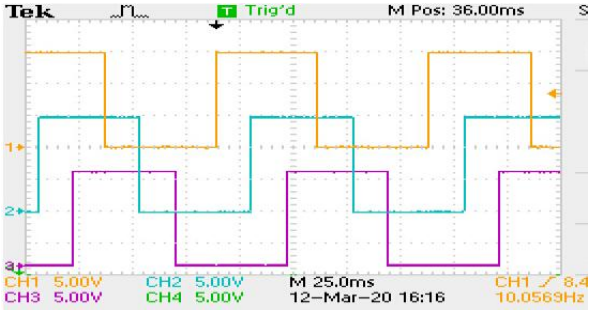

Figure 8. PWM signals for inverter upper switches with duty cycle 0.5 and frequency 10Hz

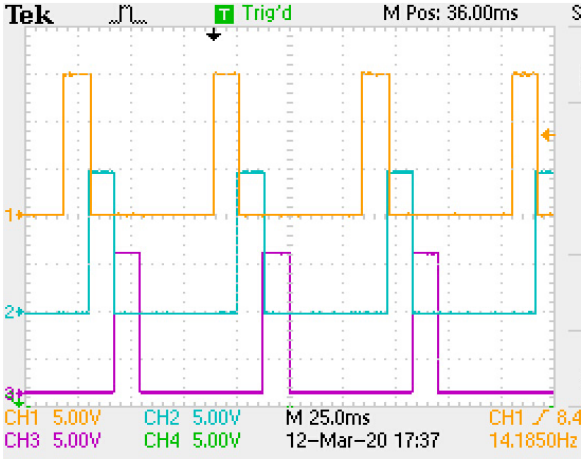

Figure 9. PWM signals for inverter upper switches with duty cycle 0.2 and frequency 10Hz.

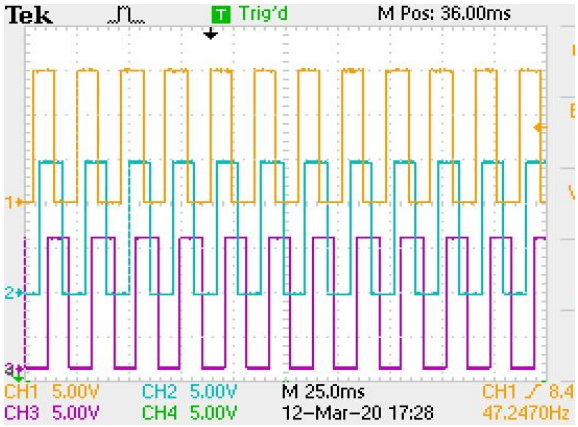

Figure 10. PWM signals for inverter upper switches with duty cycle 0.4 and frequency 47Hz.

VI. CONCLUSION

In the present paper hardware implementation voltage and frequency controlled 3 phase induction motor drive is implemented. To control the voltage and frequency a three-phase uncontrolled rectifier and pulse width modulated inverters are used. Program required controlling the inverter voltage and frequency is written in St-embed domain and embedded in Texas instrument F28069M control card. Results obtained from the hardware implementation show that speed and torque control is achieved by V/F control of induction motor. Under the fault conditions like over current or short circuit, PWM duty ratio is set to zero and shut down of PWM signals ensuring total protection against fault. Fault indicator circuit used to indicate the occurrence of fault even after the clearance of fault till the system is reset. Further as a future scope closed loop motor drive system can be implemented to maintain the performance level of the motor drive under both steady state and transient conditions.

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