International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878 (Online), Volume-8 Issue-6, March 2020

Performance Monitoring of Power Quality by using SFCL with Multilevel DVR

Prabhakara Sharma.P, SK.Shabana, M.Siva Lingam, B. Gopi, K. L. V. Sesha Sai

Abstract: ***The power distributing system based on DVR is integrated by Super conducting Fault Current Limiter gives a viable solution to attain the stabilization of voltage magnitudes where the sensitive load and voltage sag effects are minimized. Over different compensation devices, the vastly recognized multi-use dynamic voltage restorer is integrated with superconducting fault current limiter to get improved features for power quality. In this paper, novel DVR integrated with SFCL was developed effectively to improve the bus voltage as well as to suppress the fault current. It is observed that the capacity of proposed DVR along with SFCL is decreased with increased voltage at the bus when compared with single DVR method. The cost also less for this proposed method than the single DVR system. It is also observed that output power compensated and also total harmonic distortions can be reduced in this proposed method. In the proposed system by adopting the tool like MAT LAB / SIMULINK the disadvantages of single DVR method like using inverter for three level voltage source, high rating of filters, poor efficiency with respect to system performance etc., are resolved with improvised power along with reduction in total harmonic distortions.***

Keywords: DVR, SFCL, Multi-Level Inverter, Voltage Sag Compensation. Power quality Improvement.

I. INTRODUCTION

At current scenario, indemnity of voltage sag method by dynamic voltage restorer (DVR) equipped along with super conducting fault current limiter demonstrated in [2]-[5]. The over voltages and over currents is the general and undesirable power quality experience in the power distribution systems which put sensitive loads under the risk. Super Conducting Fault Current Limiter (SFCL) can provide the most commercial solution to mitigate these voltages by injecting voltage into the system. This paper presents indemnity of voltage sag method by Multi level Dynamic Voltage Restorer scheme included with Super conducting Fault Current Limiter. The principle of indemnity, regulating approaches,
specifications of components, assessment and outcome of simulation are presented with detail discussion. In this approach an overview of the multilevel DVR and SFCL with their configurations, component functions, compensating strategies and control methods are reviewed. In addition in this method improved decentralized power supply, flows of high power, high investment for equipment is needed for laying power network in the upcoming years. It is proved that the proposed control method is very effectual to identify any disturbance in power systems [4]. Therefore, the Multilevel DVR system is more feasible to control all the possible adverse impacts of voltage sag during sensitive loads. In the present study the working principle, technological description, parameters for the assessment of SFCL, regulating approach of DVR and simulations are described in detail.

II. DIODE-CLAMPED MULTI-LEVEL DVR

The characteristic features of Multi level Inverter are classified as Multi-level Inverter with Flying Capacitor, Diode-Clamped Multi-level Inverter and Multi-level Inverter with Cascade H-Bridge. Various characteristic features of multi level Inverter cascade H-bridge are predictable to be used in several applications as they don't need of any supporting components and greater-modular design, etc. When they are operated at high voltage levels it will decrease the system efficiency and loses of switching due to the generation of high switching stress. By keeping this in view we have initiated this study where DCMLI is adoptable in DVR to overcome all the issues related to voltage, current and power.
MLI-DVR is essentially integrated to SFCL to improve power quality features and it comprises of DC link capacitor, current generator, LC filters etc. The proposed DCMLI- DVR will work as device for the compensation of the issues related to power quality.

Manuscript received on March 15, 2020.
Revised Manuscript received on March 24, 2020.
Manuscript published on March 30, 2020.
* Correspondence Author
Prabhakara Sharma.P*, Associate Professor, Electrical & Electronics Engineering Department, Kallam Haranadhareddy Institute of Technology, chowdavaram, Guntur,AP,India,
S K. Shabana, B.Tech Final year Electrical and Electronics Engineering department.
M. Siva Lingam, Student of B.Tech Final year Electrical and Electronics Engineering department.
B. Gopi, Studying IV B.Tech Electrical and Electronics Engineering from Kallam Haranadhareddy Institute of Engineering & Technology, Guntur, A.P., India
K. L. V.Sesha Sai, Student of final year Electrical and Electronics Engineering from Kallam Haranadhareddy Institute of Engineering & Technology, Guntur, A.P., India

III. SYSTEM PRINCIPLE AND CONTROL STRATEGY

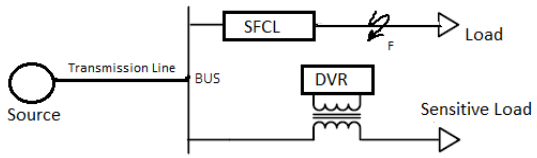

Fig.1: Schematic representation for DVR and SFCL

The above figure Shows general circuit for DVR integrated with SFCL.

At sensitive side the DVR is installed and it consist a dc link, voltage source converter, capacitor transformer and a filter. The device of SFCL is connected with other feeders in series. The SFCL limits the fault current whenever the sensitive load is not supplying to the feeders due to the occurring of three phase fault by increasing common bus voltage up to an extent.

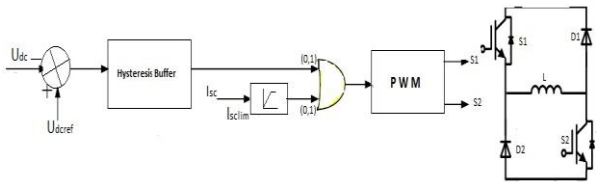

Fig (2) Schematic diagram of voltage control strategy for DC-DC converter.

The operating procedure of DVR has shown in the above figure. The regulation of dc voltage approach is for the maintenance of constant DC voltage in the DC-DC converter. The error which occurs between the actual and reference will send for a hysteresis buffer to produce control signal of PWM, where it will operate switches A1 and A2. The DC voltage can be stabilized by regulating operating position of two switches.

In this proposed method the voltage interruption can be compensated by real time locking of phase angle and voltage magnitudes for the effective power quality.

III. PARAMETERS ESTIMATION OF SFCL

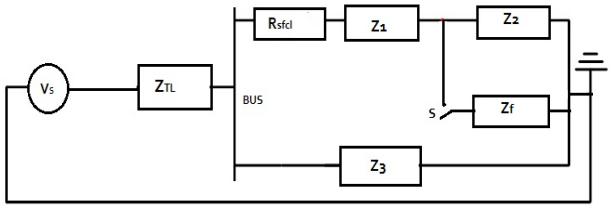

Fig. 3. Distribution system of equivalent circuit

The above figure shows occurring of three-phase fault in one feeder, by closing the respective switch. the bus voltage can be expressed as follows

$$V_{Bus} = \frac{Z_I}{Z_{tl}(Z_I + Z_3) + Z_I Z_3} V_s$$

where

$$Z_I = R_m + Z_1 + \frac{Z_2 + Z_f}{Z_2 Z_f}$$

Where Z_{tl} indicates impedance of total line; *Rm* indicates resistance of S.F.C.L; *Z*1 is the line fault location; *Z*2 is the total impedance indicating from line end point to location of fault, *Z*3 indicates impedance of load.

IV. MATLAB/SIMULINK RESULTS

The distribution system of power has shown in figure 1 representing fault under line1 where three phase fault occur which indicates drop of voltage in common bus up to 90%. The specification for the distribution system has shown in Table I.

Table I proposed operational specifications for DCMLI-DVR with S.F.C.L.

Specifications	Value
Total voltage of bus	10.77 KV
Transmission line L,R values	4.76mH,1.188ohms
Distribution line L,R values	0.4mH,0.0998ohms
Sensitive & Ordinary Loads	5MW,1MW
Resistance of Super Conducting Fault Current Limiter	1.306ohms
Inductance of S.C	1.2H
Initial current of S.C.	1500A
Critical current of S.C	1760A

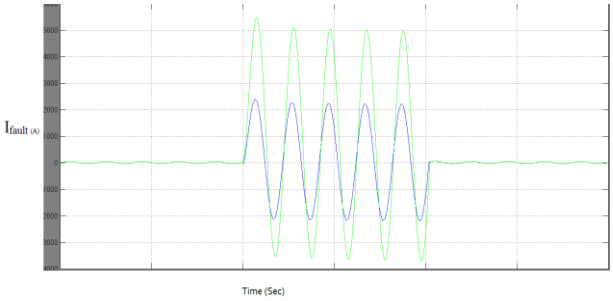

Fig. 4(a) The fault current representing in distribution line1 along with proposed DVR Integrated SFCL and single DVR.

The above figure shows that the proposed method can decrease the fault current. Where it was noticed that fault current is decreased up to 2.30 kA which is less when compared with single DVR scheme (5.40 kA). Similarly, it was also noticed that in this proposed method the steady fault current also reduced from 5.00 kA (with single DVR) to 2.10 kA (with DVR & SFCL). Moreover, the bus voltage increased from 1.0 kV (single DVR) to 5.0 kV (SFCL&DVR), as shown in the Fig. 4(b).

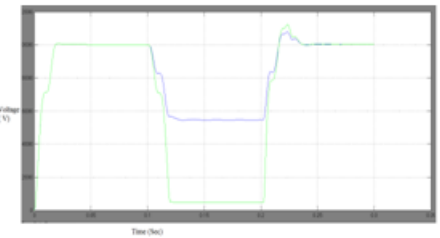

Fig 4(b) The bus voltage of the proposed DVR integrated SFCL and single DVR

The suppression of fault current leads to the reduction of loss in transmission voltage.

So it is concluded that the proposed method is not only suppress the fault current but also it can enhance the voltage of bus for improvised power quality.

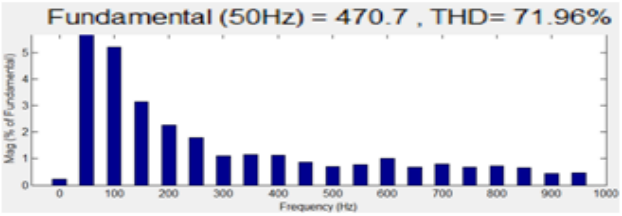

Fig.4(C): THD of source current of DVR integrated with SFCL system

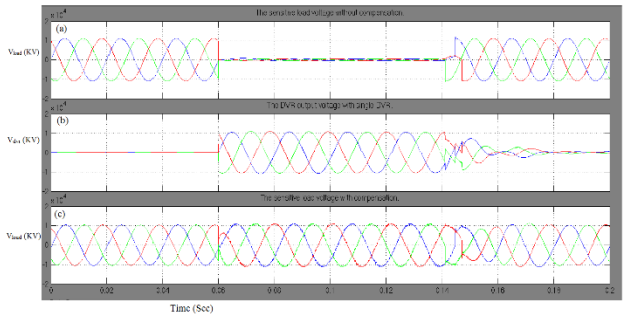

Fig.5 (a) The single DVR output voltage.

(b) The proposed DVR & SFCL output voltage
(c) The sensitive load voltage after compensation.

The above figure representing sensitive load voltage, output of DVR voltage and output voltage DVR with SFCL where the proposed method can increase the sensitive load voltage which can be adopted for power quality.

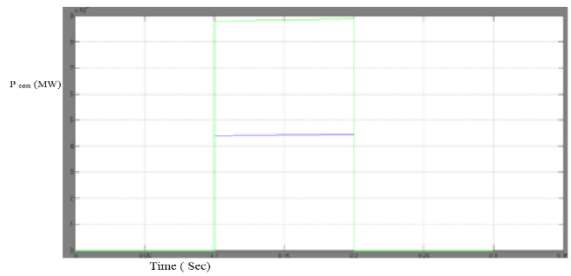

Fig. 6: The output compensated power of proposed DVR & SFCL and single DVR system.

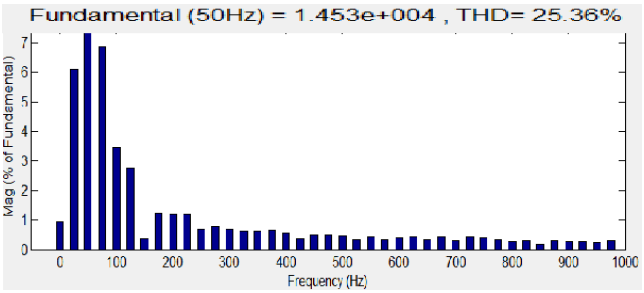

Fig.7 THD of source current of MLI-DVR integrated with SFCL system

When it is compared with the output power compensation in single DVR with the proposed DVR & SFCL it is observed that power compensation is reduced to 0.52MWwhich is 1.61 times less than the single DVR method (0.84 MW).

Table II: THD Comparison of Source Current under Several Control Functions

THD (%)	Without Compensator	Proposed DVR & SFCL
Source Current	71.96%	25.36%

Over the VSI based DVR, the proposed DCMLI-DVR integrated with SFCL has better reduction in distortions of source current.

V. CONCLUSIONS

- This proposed method is very much accurate and efficient than the single DVR method to regulate sensitive load voltage in common bus.
- Due to its high resistance it suppresses the fault current and increases voltage of common bus.
- The capacity requirement also reduced when compared with single DVR method which leads to cost reduction.
- The multi level DVR with SFCL improves the voltage quality in distribution of power.

REFERENCES

1. Zheng et al.., “Enhancing transient voltage quality in a distribution power system with smes based dvr and sfcl,” IEEE trans., appld supercondvty. Volume 29, number 02, mar., 2019.
2. S Nagaya et al.., “ Field test results of the 5MVASMESsystem for bridging instaneous voltagedips, ” IEEE trans., on appldsupercondvty., volume 16, number 02,page numbers 632-635, june 2006.
3. F Balabjerg “ Comparison of system topologies for dynamicvoltage restorers” in confer..re., IEEE volume 04, page numbers 2397-2403 in 2001.
4. Jon Fi Moon, “ Voltage quality analysis in power distribution system with super conducting fault currentlimiter at grounding line ” in kieep., volume 62p, number 04, page numbers 159-163 in 2013.
5. J S Kim, “ Study on selection of sfcl’s impedance for protection coordination with overcurrent relay in a distribution system ” in IEEE Trans., and distbtion confe., page numbers 1-4 in 2009.
6. Li Y, “ Behavior investigations of super conducting fault current limiters in power systems” IEEE trans., on appld supercondvty., volume 16, number 02, page numbers 662-665 in june 2006.

AUTHORS PROFILE

Prabhakara Sharma Pidatala obtained his B.Tech in EEE from KLCE,AP, India. He completed his Master of Technology in High Voltage Engineering from University College of Engineering, JNTU-Kakinada. AP, India and pursing Ph.D in Andhra University . He is currently working as Associate Professor in Electrical & Electronics Engineering Department in Kallam Haranadhareddy Institute of Technology, chowdavaram, Guntur,AP,India, since 2013. His area of interest includes Electrical Machines, Hvdc, AC-DC Power Flows and FACTS devices.

Sk.Shabana Student of B.Tech Final year Electrical and Electronics Engineering department. She is department topper and is placed in department excellence outstanding merit scholarship one time. During his B.Tech course , she has done three technical research paper at national level and his area of interest includes Power systems, Renewable energy sources and FACTS devices.

M. Siva Lingam student of B.Tech Final year Electrical and Electronics Engineering department. During his B.Tech course, he has done 1 technical paper at national level. His interest area are Power Electronics, Control Systems and Power Systems.

B Gopi is an Under Graduate student studying IV B.Tech Electrical and Electronics Engineering from Kallam Haranadhareddy Institute of Engineering & Technology, Guntur, A.P., India. He is one of the topper in the college who got meritorious scholarship and won many prizes in the technical events held at intra and inter college level. His research interests include HVDC, Electrical Machines and Electrical distribution systems.

K L V Sesha Sai is student of final year Electrical and Electronics Engineering from Kallam Haranadhareddy Institute of Engineering & Technology, Guntur, A.P., India. He has done 2 technical paper at national level. His interest area are Networks, Electrical Measurements and Power system analysis.