



# A Power Efficient Improved NOR-Type TCAM Design using OR-Type Match-Line Segment

Rahul Nigam, Santosh Pawar

**Abstract:** This paper presents the novel way to deal with diminish power utilization in a ternary content addressable memory (TCAM) designed in current innovation. The main aim of this TCAM design is to reduce the dynamic power consumption. In TCAM large amount of the power consumption happens during search operation, so we focussed on this area. Here right now give pragmatic plan of a TCAM which is arranged for low-power applications. Simulation of this design has done in Tanned EDA V.16 tool. For simulations of Low power TCAM designs we used predictive technology model (PTM) 45nm for high-performance applications which include metal gate, high-k and stress impact of CMOS technology.

**Keywords:** TCAM, low power, high performance, EDP, NOR type CAM, OR type cascade Match-line.

## I. INTRODUCTION

In a computer network, the main role of a switch is to think about the target address of a packet to every single imaginable path and pick the suitable IP address on its system. System switches forward frames and packet at wire speed by utilizing Application Specific Integrated Circuit (ASIC) equipment. These switches stored routing tables in a high-speed memory so that it can take decisions to forward or restrict these packets in high speed hardware. Switches has to perform lookups operation by using these tables to confirm whether a packet with a particular target IP address must be dropped by a routing table or not. A switch that perform this type of task which incorporate these memory tables referred to as Associative Memory or TCAM. To implement this lookup operation a CAM is best device because of its fast search capability. The primary business utilization of CAMs as of late is to group and forward IP packets in system switches [1].

Because of its high pursuit speed, CAM can be utilized in different applications, for example, extract parametric curves [2], Image Transforms/Hough Transform [3], Huffman Encoding and Decoding [4], Source coding or Bit-rate reduction [5] and picture coding [6]. Beside these applications other use of CAM is to perform searching and sorting operation on data [7-8].

A CAM search data address by its contents rather than its location. A CAM operates on three different modes i.e.

READ, WRITE and SEARCH. "SEARCH" is the main operation of CAM on which we focussed. During the search operation, input search data compared simultaneously with all the previously loaded information in memory. This ability makes CAM a fastest device compared to any other conventional device used for searching data.

## II. CAM CELL TYPES

CAMs based on storing and searching of data can be classified into two essential classifications for example (1) Binary CAMs (BCAMs) and (2) Ternary CAMs (TCAMs). A BCAM is a sort of memory which can store and search words in binary system, which uses only two symbols i.e. "0" and "1". Thus, binary CAMs are suitable for applications that require only exact match on the other hand a TCAM in addition utilizes don't care condition "X" regard that means to both "0" and "1" sometimes called wild bit [9]. Wild bit implies that a "X" regard put away in a cell causes a match whether input search bit is "0" or "1". With this feature TCAM suitable for routers because it can store data in form of routing table [10]. TCAM is very important component to make IP routing tables for searching on longest matches in an address [11]. In TCAM design also has ability to insert new entry location i.e. allows complete flexibility. This is done by a longest prefix match (LPM) determination circuit, where in that circuit delay increases logarithmically as the number of bits increase [12].

### A. Binary Cell

Here 10T BCAM is shown in Fig. 1. The storage part has implemented by a SRAM cell circuit (P1, P2, N6-N9 transistors) and to compare data it is implemented by an XNOR function (N1-N4 transistors).

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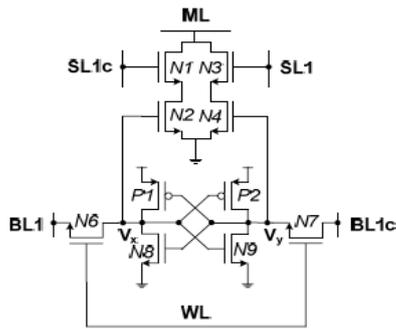
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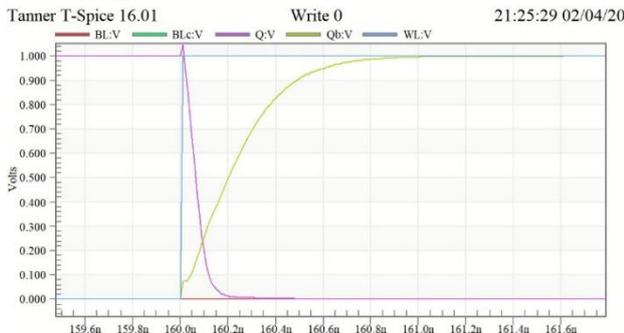
# A Power Efficient Improved NOR-Type TCAM Design using OR-Type Match-Line Segment



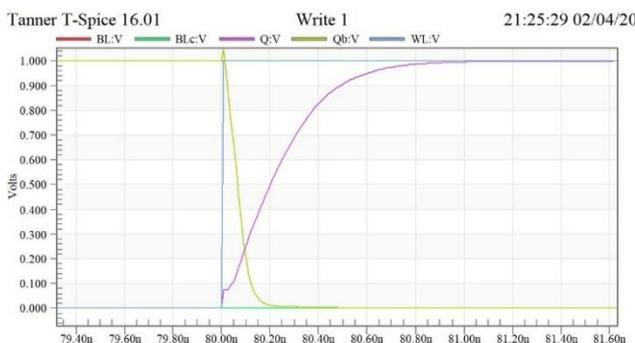
**Fig. 1. 10T BCAM**

- **Write Operation:** To do the WRITE activity, we place the information on the bit-line (BL) which we need to store and empowers the word-line (WL). When WL is made

high it turns on the entrance transistors (N6-N7) as appeared in Fig. 1, with the goal that the inner hubs of the inverters  $V_X$  and  $V_Y$  are store the information gave by BL. In the event that we take  $V_X = 0$  and  $V_Y = 1$  condition then P2 and N8 transistors were "ON" and P1 and N9 transistors were "OFF" and "0" value is stored in cell. Now we need to store "1" then we put  $BL1 = "1"$  and  $BL1c = "0"$  values in bit-lines. At this point when WL is empowered ( $WL = "1"$ ) then it gets transistors (N6-N7) to turn "ON" which stream BL current and store "1" value in cell. To overwhelm the feedback inverters, we need large size access transistors contrast with PMOS transistors P1 and P2. Fig. 2 show simulated result for write 0 in TCAM cell. Similarly, Fig. 3 show simulated result for write 1 in TCAM cell. In both plot BL represent bit-line waveform, Q represent output waveform and WL represent WL waveform.



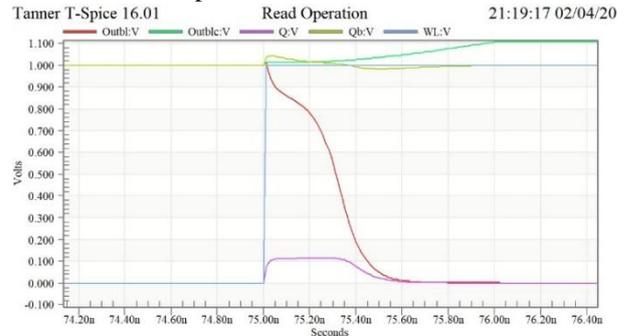
**Fig. 2. Write 0 activity in TCAM cell**



**Fig. 3. Write 1 activity in TCAM cell**

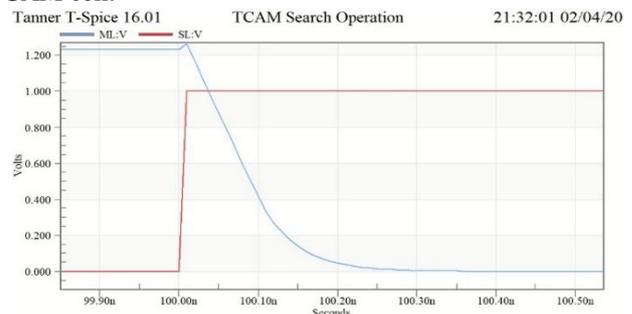
- **Read Operation:** The READ activity is done by pre-charging the BL1 and BL1c to  $V_{DD}$  and empowers the word line (WL). We take situation when  $V_X = 1$  and  $V_Y = 0$ , at that point current  $I_{READ}$  releases BL1c (through N7

and N9). BL1 stays at  $V_{DD}$  for the reason that  $V_X = "1"$ . In this way, there is a little voltage distinction created between BL1 and BL1c. The current  $I_{READ}$  brings the voltage  $V_X$  up in very little quantity. Along these lines, we structure the driver transistors (N8-N9) such that  $V_X$  stays beneath the inverter threshold voltage and henceforth the cell doesn't accidentally write "1" information at the time of the read activity. Generally, as a rule, the driver transistors (N8-N9) are estimated 1.5 times broader than the entrance transistors (N6-N7). Fig. 4 show simulated result for read operation in TCAM cell.



**Fig. 4. READ activity in TCAM cell**

- **Search Operation:** The SEARCH activity is done in three stages. In initial step we pre-charge SL1 and SL1c to GND. Pre-charging SL1 and SL1c to GND during the ML pre-charge guarantees that both pulldown ways are "OFF". At that point in second stage we pre-charged ML to  $V_{DD}$ . At last in third stage, the pursuit information bits are applied on search-lines SL1 and SL1c. In the event that search information bit is indistinguishable from the put away worth ( $SL1=BL1$ ,  $SL1c=BL1c$ ) both ML to GND pull-down ways stay "OFF" and the ML stays at  $V_{DD}$  demonstrating a "match" case. Else one of the draws down ways directs and releases the ML to GND demonstrating a "mismatch" case. Fig. 5 show simulated result for search operation (mis-match) in TCAM cell.



**Fig. 5. Search activity in TCAM cell**

## B. TCAM Cell

A normal 16T static TCAM cell is appeared in Fig. 6. The TCAM memory cell consists of two parts one is storing part and other is comparison part. Storing part made of 6T Static Random-Access Memory (SRAM) cell which is utilized for keep the information and to compare data an XNOR logic is used. WRITE, READ and SEARCH activities right now done similarly as depicted before. For the masking activity we should be turn off both ways of pulldown ML to GND. For instance, global masking is settled by making  $SL1 = SL2 = "0"$  and local masking is settled by making  $V_X = V_Y = "0"$ .

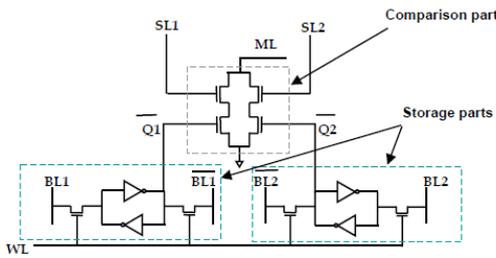


Fig. 6. 16T TCAM

III. CONVENTIONAL CAM ARRAY STRUCTURE

A CAM word with n number of bits is accomplished by interfaces n CAM cells in line up. All the CAM cell in a word have same match-line (ML) however they have diverse Search-lines (SLs). The ML is associated with a match-line sense amplifier (MLSA), which decides if in a word all bits matches with the search bits or not. During search activity the ML voltage stays at V<sub>DD</sub> just if all the bits in a word are similar and gives a "match" case. As it were, regardless of whether a single piece of discrepancy bring about a release of ML voltage to ground and shows a word "mismatch" condition. A CAM structure (M × N) is realized by link M number of CAM words with a similar arrangement of SLs. The search bits (N bits) are written in SLs, which are compared in all the M words simultaneously [13].

Fig. 7 presents the functional block diagram of M-words × N-bit CAM. Information put away in the CAM cells depends upon the row and column decoder outputs. The activity is separated into three stages: SL pre-charge, ML pre-charge and ML evaluation. First all the SLs are pre-charged to GND using slpre signal, so in this way the entire pulldown path from ML to GND is disconnected. Then pre-charging all the match-lines (ML<sub>1</sub>, ML<sub>2</sub>.....ML<sub>M</sub>) to V<sub>DD</sub>. The required information is given through the SL driver and when the SL esteems (SL1 to SLN) coordinate with all CAM cells in a row, the corresponding ML remain charged at V<sub>DD</sub> and the corresponding state is called as a HIT. In the other state (MISS), the MLs are discharged to GND. The sense amplifier (SA) detects the ML charge variation and provides a match-line sense output (MLSO<sub>1</sub>, MLSO<sub>2</sub>... MLSO<sub>k</sub>).

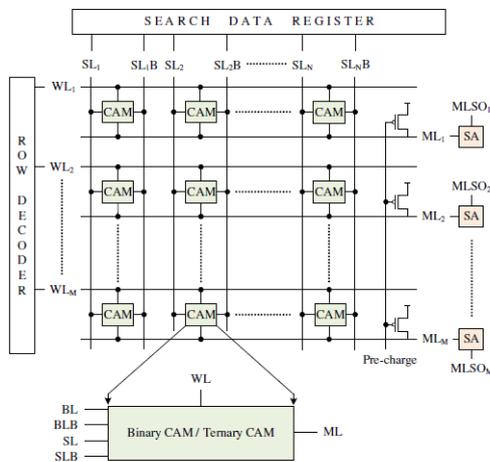


Fig. 7. A content addressable memory array structure

A. Match-line model

The model for the match condition of the ML is a capacitor C<sub>ML</sub> and the model for the miss condition of the ML is a capacitor C<sub>ML</sub> parallel with a pulldown resistor R<sub>ML/m</sub> where m is the quantity of bits that miss on the ML appeared in Fig. 8. The ML capacitance C<sub>ML</sub>, comprises of the ML wiring capacitance, the NOR cell diffusion capacitance, the diffusion capacitance of pre-charge transistors and the input capacitance of the MLSA. ML resistance changes with the quantity of bits mismatch.

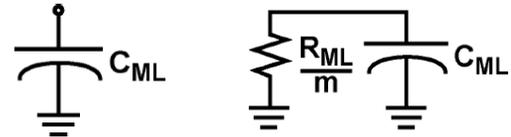


Fig. 8. (a) the match case (b) the mismatch case Match-line model [14]

The ML capacitance can be given by condition

$$C_{ML} = [2g+4(n-g)] C_{DRAIN} + C_{INT} + C_{MLSA} \quad (1)$$

Where "g" is the quantity of globally masked bits, n is the number of bits per word, C<sub>DRAIN</sub> is the drain capacitance of each transistor in the comparison logic part of TCAM cell, C<sub>INT</sub> is the interconnect capacitance of each ML and C<sub>MLSA</sub> is the MLSA input capacitance. At the point when an information bit is globally masked (SL1 = SL2 = "0") just the drain capacitances of SL transistors add to C<sub>ML</sub>. On the other hand, C<sub>ML</sub> additionally incorporates the capacitance of the inner nodes. Along these lines, C<sub>ML</sub> esteem in worst case is the point at which no global masking i.e. g = 0 and the best case C<sub>ML</sub> when all bits have globally covering i.e. g = n [14].

B. Match-line delay

The time required to pre-charge the match-line (from 10% to 90% i.e. rise time of ML) is given by

$$T_{MLpre} = 2.2 * R_{EQpre} C_{ML} \quad (2)$$

where R<sub>EQpre</sub> is the equivalent resistance of the pre-charge transistor [14].

The time required to evaluate the match-line which can be defined as the time require for the ML to fall to 50% is given by

$$T_{MLEval} = 0.69 R_{ML} C_{ML} \quad (3)$$

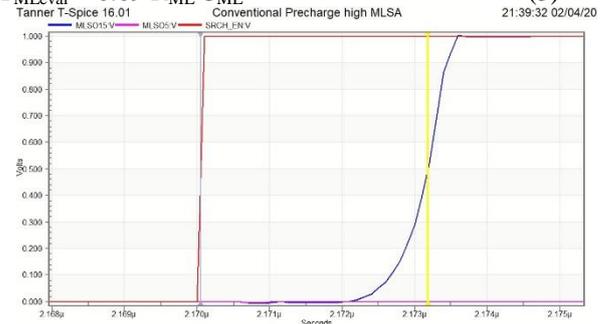


Fig. 9. TCAM with conventional MLSA worst case (one-bit mismatch) search time analysis

Above Fig. 9 show worst case search delay time. MLSO 15 show case of one-bit mismatch output of MLSA goes high whereas MLSO 5 match case output remains low.

IV. TECHNIQUES TO REDUCE POWER CONSUMPTION

Recently, the arrangement of internet protocol version 6 (IPv6) has speed up the interest for higher the limit of TCAMs, while the interest of web surfing increase continuously requests speedy TCAMs. Because of its simultaneous search nature TCAM's search activity comes at the expense of high-power request [15]. As CAM applications increment, requesting bigger size CAM holds this issue is additionally expanded.

There are a number of techniques which can be utilized to lessen the power utilization in TCAM.

In TCAM power is consumed mainly in frequent parallel SEARCH operations. MLSA is the part of CAM which is used in the search operation, so most of the power reduction techniques are based on these circuits. The match-line power draining during search activity is one of the significant vital source of power utilization in CAM. The other significant key source is the SLs. Numerous works are going on to the plan of the ML structure of CAM to speed up and to decrease the power utilization.

In our design we examined the issues with TCAM in a modern technology. This design has a keen focus on issues related to power consumption and increase in data search speed. In this design we started with design of a NOR type TCAM, which is able to perform storing and searching operation on data. In the next step design and analysis carried out using OR-type cascaded match-line structure [16]. This structure sequentially connects rapid OR-type coordinate line sections. With this design we reduce power consumption as compared to conventional design.

V. THE OR TYPE CASCADED MLSA SCHEME

Match-line scheme as appeared in Fig. 10 each stage is like an OR gate, which is made out of a NOR gate and a NOT gate. The NOR gate is made out of an examination unit and CAM cell. The whole memory structure is partitioned into different stages which are connected by this MLSA. There are no delicate segments in the circuit which will increase the power of the circuit. The equal portions can be sequentially associated naturally. The activity of this design is partitioned into two stages i.e. pre-charge stage and assessment stage. To begin with the pre-charge stage, SEN1 is stated to high from the outset. At that point all the pre-charge (P1-Pn) junctions and the outputs of each stage are charged to V<sub>DD</sub> and the local match-lines (ML1-MLn) are released to ground. Simultaneously, the search information is sent into SLs. Next, During the assessment stage, SEN1 is pulled down to ground, and afterward the outcome can be separated into two conditions to be talked about.

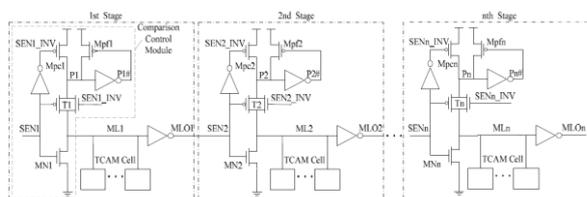


Fig. 10. OR type match-line TCAM with n stages [16]

First condition is mismatch, in this condition the TCAM cells equivalent to a resistor associating with ground. The

pre-charged node P1 will be pulled down to ground and P1# will become high, this action turns off the feedback transistor Mpf1, which is appeared in Fig. 11. At that point the output of the first stage match-line sense amplifier (MLO1) will stay high, which won't actuate the assessment of the following stages because mismatch condition is detected.

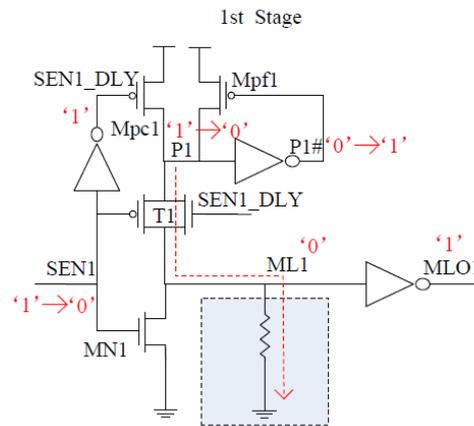


Fig. 11. The equivalent circuit of first stage in case of mismatch [16]

Second condition is match state, in this state the TCAM cells equivalent to a capacitance interfacing with ground. The match-line of this stage ML1 will be charged to V<sub>DD</sub> and the output of this stage match-line sense amplifier (MLO1) will be pulled down to ground, which will continue actuate the assessment of the following stage as appeared in Fig. 12 because this stage is match.

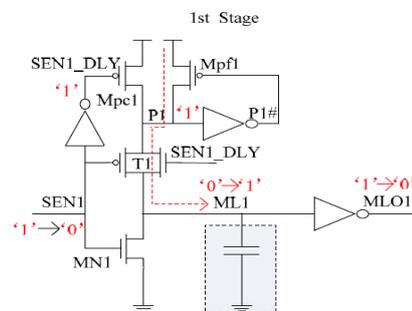


Fig. 12. The circuit OF first stage in case of match [16]

Fig. 13 show simulated result waveform for point P voltage in different cases i.e. Match stage case (XMLSA\_OR\_type\_cacaded\_42. N\_1: V) and Mismatch stage case (XMLSA\_OR\_type\_cacaded\_77. N\_1: V).

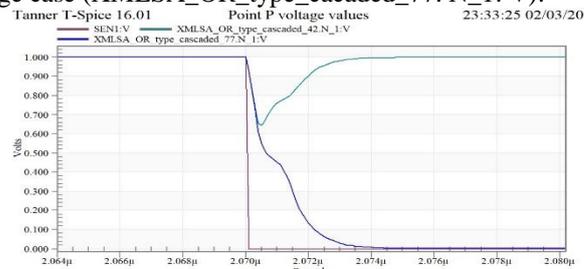


Fig. 13. Point P voltage waveform in Match case (XMLSA\_OR\_type\_cacaded\_42. N\_1: V) and Mismatchcase (XMLSA\_OR\_type\_cacaded\_77. N\_1: V)

The basic task which we have to focus is on the condition when all the stages in a word are matched and in this condition the circuit is analogous to a series of inverters, as appeared in

Fig. 14, here a good design will improve the assessment speed.

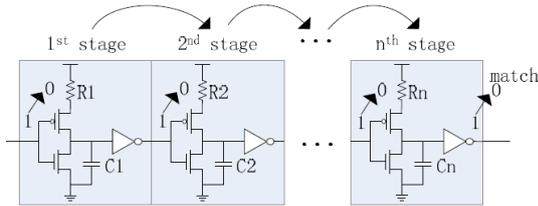


Fig. 14. The equivalent circuit in the case of match [16]

Fig. 15 show MLSO delay for different stages (First stage: N\_6, Second stage: N\_5, Third stage: N\_45 and Final output MLSO5d) in case of word match.

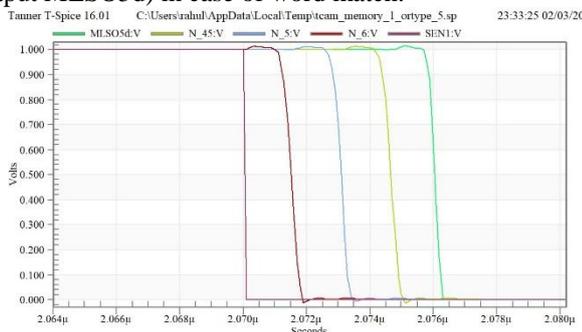


Fig. 15. OR type cascaded Match-line different stages output

## VI. RESULT AND DISCUSSION

The most part of design performance is depending on the total stages we used in memory. The circuit will show signs of improvement in the event when it embraces less stages. if there are such a large number of TCAM cells in a single stage the word circuit may show wrong result on account of the charge sharing issue between the huge ML and pre-charge node Pn in case of match. Along these lines, there will be a trade-off between the speed and the quantity of stages. The presentation of the structure additionally relies upon the size of the transmission gate and the feedback transistor. In case that when the size of transmission gate is large, the resistance in the pull-down system will be smaller, which implies more grounded pull-down capacity. when in a stage mismatch will detect then it increases the pull-down capacity that will make it quicker to pull down the pre-charge node (Pn) to ground. Likewise, when in a stage all bits are match then large size transmission gate will make it simple to charge match-line to high. But drawback of large size transmission gate is that it will prompt a bigger capacitance of the pre-charge node Pn, which will responsible for more power wastage. Thus, there will be a tradeoff between the power utilization and the searching speed.

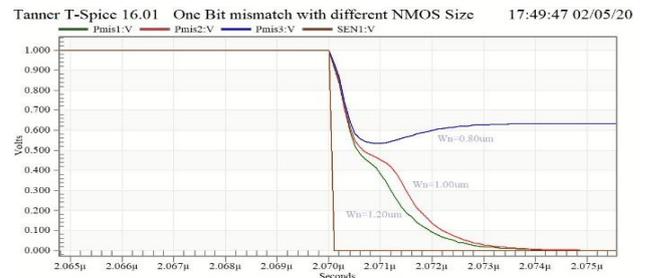


Fig. 16. P point voltage in case of one-bit mis-match with different NMOS (transmission gate) size

Fig. 16 are showing simulated result for different values of point P voltage waveform for different NMOS size. With NMOS size  $W_n = 0.80\mu m$  ( $P_{mis3}$ ) it gives incorrect output in simulated result.

Fig. 17 are showing simulated result for different values of point P voltage waveform for different PMOS size. With PMOS size  $W_p = 0.85\mu m$  ( $P_{mis2}$ ) it gives incorrect output in simulated result.

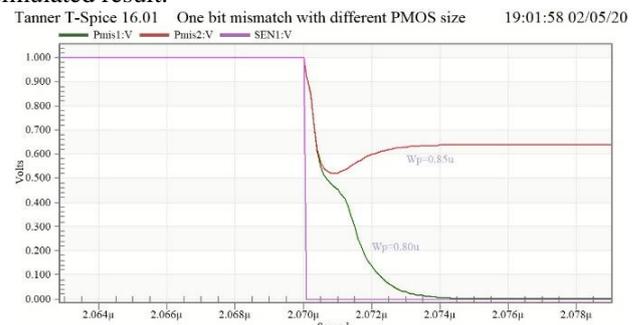


Fig. 17. P point voltage in case of one-bit mis-match with different PMOS (feedback transistor) size

Table I shows the performance comparison of different TCAM designs and we got best result for 32\*72 size OR type cascaded TCAM with 3 stages.

Table- I: Performance comparison of TCAM types

	Conventional MLSA		OR type cascade MLSA	
	32*32 Size	32*72 Size	32*32 Size (4 stage)	32*72 Size (3 stage)
Search delay(ns)	3.132	4.261	6.003	7.606
Energy (fJ/bit/search)	3.869	4.738	1.059	0.722
EDP	12.118	20.187	6.356	5.489

Table- I results clearly shows that as TCAM memory increase its word size by the use of OR type cascade MLSA result get improved in comparison to conventional MLSA. We get best performance for 32\*72 size TCAM design with OR type cascade MLSA when number of stages are three in 45nm technology.

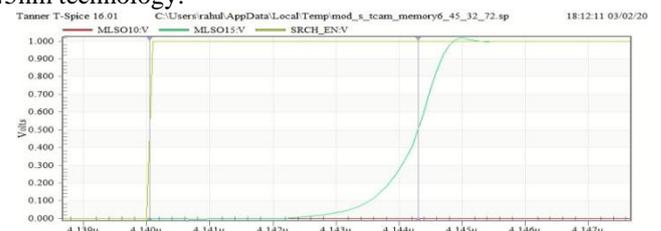
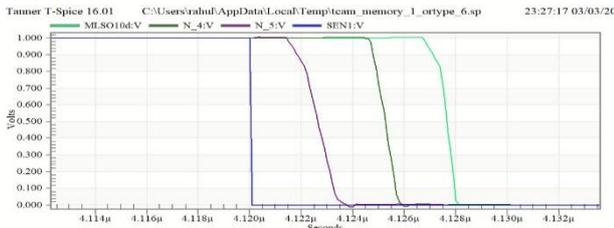


Fig. 18. Search operation on 32\*72 TCAM with conventional MLSA

Fig. 18 shows conventional MLSA output where MLSO 10 is match case and MLSO 15 is one-bit mismatch (worst delay) case.

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**Fig. 19. Search operation on 32\*72 TCAM with OR type cascade match-line for 3 stages.**

## VII. CONCLUSION

This paper presents an OR-type match-line conspire for elite with effective TCAM memory in 45nm technology with 250nm Library files. For this memory with 45nm PTM HP model: V2.1, simulated result shows that in this design as compared to conventional scheme during search operation dynamic power consumption in OR type cascade MLSA happened only when if a stage are matched. Generally, in a memory most of the word are in mismatch condition, so because of this reason this technique reduces more power consumption. If any stage mismatch is detected it inactivate the remaining stages. This power reduction come with little increase in search time. So, we conclude that this OR type cascade match-line design provided reduction in energy consumption during search operation compared to conventional MLSA with little penalty in search time and this result got improved as we gone towards a memory have large word size.

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