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Validation of Hybrid Network-on-Chip Architecture for Optimized Performance using BookSim Simulator

Talla Vamshi, T. Satya Savithri

Abstract: ***Various complex integrated circuits suffer from the issues like poor connectivity, higher energy consumption and design productivity. One of the best solutions could be Network-on-Chip architecture which could solve the above issues. The Network-on-Chip architecture should be modelled and simulated well to evaluate the performance and analyse the cost. This paper presents a method to validate the proposed Network-on-Chip architecture with direct sequence spread spectrum using BookSim simulator. This simulation aims at validating the network parameters like packet latency and network latency. The detailed architectural parameters are compared and presented in this paper.***

Keywords: Central Key Scheduler, Network-on-Chip, Processing Element, Ring Key Scheduler, System-on-Chip.

I. INTRODUCTION

Network-on-Chip architecture has emerged as the viable alternative for the design of modular and scalable on chip communication architectures. Current System-on-Chips are built by integrating Intellectual Property (IP) blocks, each one of which having separate communication requirements. The earliest work on Network-on-Chip architecture as a new System-on-Chip paradigm was attempted by Benini and Micheli, who have rightly quoted – "On-chip micronetworks, designed with a layered methodology, will meet the distinctive challenges of providing functionally correct, reliable operation of interacting system-on-chip components" [1]. Bahn, Lee and Bagherzadeh [2] in the literature presented a design on the Network-on-Chip architecture which adopts a minimal adaptive routing algorithm. This design complexity is which also offers nearly optimal performance compared to 2D mesh algorithms that could be implemented to various System-on-Chip developments.

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* Correspondence Author
Talla Vamshi*, Department of ECE, Talla Padmavathi College of Engineering, Warangal, India. Email: vamshi22g@gmail.com
Dr. T. Satya Savithri, Department of ECE, Jawaharlal Nehru Technological University, Hyderabad, India. Email: tirumalasatya@gmail.com

In [3], Ogras, Hu and Marculescu have sketched out the research problems associated with Network-on-Chip architectures under the broad heads of communication infrastructure synthesis, application mapping optimization and communication paradigm selection. Some of the major issues discussed in [3] are the sizing problem of the buffer, problem of floor planning, switching and topology synthesis problem. Kumar et. al. [4] has presented a reconfigurable Network-on-Chip architecture where both of the networking and processing nodes are configured. The same has been showcased with a mapping to FPGA. Kumar et. al. in [5] have addressed the problem of design and instantiation of a Network-on-Chip architecture based System-on-Chip platform in a systematic and automated manner using AEthereal Network-on-Chip and Silicoon Hive processing cores, both of them configurable at run-time and design. The similar thing has been verified on a Celoxia RC300E development board.

A comprehensive survey and comparison of Network-on-Chip architecture tools based on the parameters – network size, buffer size, packet distribution, routing algorithm, packet injection ratio, selection strategy and traffic distribution was presented by Achballah and Saoud in [6]. The same kind of work is done by Agarwal et. al. [7], who has presented GALS – Globally Asynchronous Locally Synchronous strategy and the contributions to Network-on-Chip architecture tried to include, but not rein topology, router architecture and protocol, switching techniques, flow control, virtual channel, buffer implementation, error coding and decoding. This paper also looks at various Network-on-Chip architecture implementations such as XPIPES, QNOC, Ethereal Network-on-Chip architecture, and SPIN. Some Network-on-Chip architecture challenges were also addressed, such as QoS and system-level simulation environments.

A perfect example of Network-on-Chip architecture – the AEthereal Network-on-Chip architecture with two components – routers and network interfaces and implementing GS-BE distributed architecture was explained by Goossens, Dielson and Radulescu [7]. The programming model used in this paper is centralized.

Murali et. al [8] addressed the design issues of synthesizing power efficient Network-on-Chip architecture interconnect for CMPs, providing guaranteed optimum throughput and predictable performance for specific application to be executed in 25-core chip multi-processors (CMPs) which is applicable in practice to Network-on-Chip architectures.

Liu, Li, Chen and Liu [9] has discussed about the stacked onchip architecture so as to improve the efficiency and reliability of system onchip communication. This is obtained using control schemes named delay insensitive asynchronous physical channel and reserved virtual channel which assure the quality of service of the on-chip network.

Mesidis and Indrusiak in [10] uses schedulability analysis as a ranking function in a genetic algorithm allowing tasks and communication flows to meet deadlines in all possible scenarios. Wormhole Network-on-Chip architecture is adopted with 33 priority pre-emptive virtual channels using mesh topology and Y deterministic routing.

This paper presents the validation of various Network-on-Chip architectures which are predefined in the BookSim simulator and compared to the proposed topology. The BookSim simulator is very flexible high-level tool from the standpoint of a system simulation. In addition, from the standpoint of network design, the BookSim simulator gives detailed modeling of all the key parameters of the network router. This simulator holds modular design which facilitates changes in the network features also allows the addition of new features. The unique feature of the BookSim simulator is the communication between the neighbouring routers which occur through the channel, but not through the data structure or a global variable, this facilitates the actual network design.

II. NETWORK-ON-CHIP ARCHITECTURES

Two different scheduler architectures are considered viz. Central Key Scheduler architecture and Ring Key Scheduler Architecture. The comparison of central key and ring key scheduler architectures is presented in Fig. 1. The other Network-on-Chip architectures are discussed below.

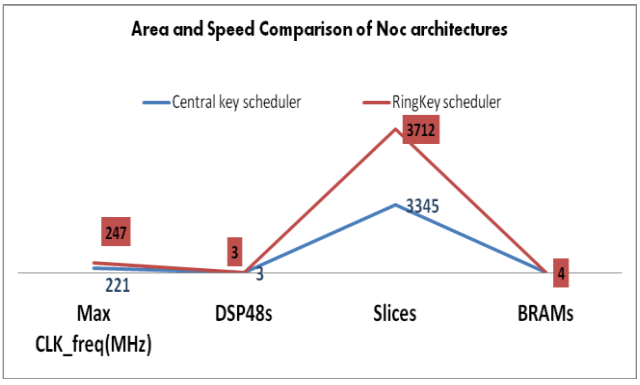

Fig. 1. Comparison of Network-on-Chip architectures.

A. Torus Network-on-Chip architecture

The torus network architecture was proposed in [11]. Each processing element is placed as a tile and connected by the torus network. The tiles may represent Processing Elements or Storage elements. Packet Switching is applied for inter tile communication. NIs are placed are located on the peripherals of each tile. The packets are exchanged between adjacent neighbours.

B. Fat-Tree Network-on-Chip architecture

The SPIN network was proposed and presented in [12]. The SPIN network utilizes a Fat-Tree topology where each processor is located at the leaf node of the fat tree. Messages are exchanged between processing elements by travelling up and down. Packet header has address and other routing information. Packet Trailer contains no data but a check sum for error detection.

C. CLICHÈ Network-on-Chip architecture

Kumar et al. [4] proposed Chip Level Integration of Communicating Heterogeneous Elements (CLICHÈ) topology. It is a 2D mesh consisting of m x n mesh of switches; interconnecting Intellectual Property (IP) Elements. CLICHE topology is being widely used in Network-on-Chip architecture designs because of its simplicity, regular structure and shorter inter switch wires, thus making it more suitable for tile based architectures. In this topology, under utilization of links may result in the event of localized traffic, because in some particular cases not all PEs may have the same communication requirement. This leads to mapping inefficiencies and wastage of resources.

III. IMPLEMENTATION FLOW OF NETWORK-ON-CHIP WITH AUDIO DECODERS

PCM, CVSD and ADPCM encoded data is generated and written to ROMs in simulation reading audio encoders data from individual ROMs, parallel to serial conversion, encoded serial data is applied as input to IP Nodes: PCM encoded serial data to IP Node 0, CVSD encoded serial data to IP Node 2, ADPCM encoded serial data to IP Node 4. The same data will be received at the Nodes 1, 3 and 5. Serial to parallel conversion at IP Node 1, 3 and 5. Encoded parallel data is applied as input to three Decoders. Finally decoded output can be observed at the three decoders.

PCM encoding of ramp signal is done in MATLAB. This encoded signal is converted as .Coe file. The .Coe file is given to IP core generator, then stored in the ROM as .Mif file. Fig. 2. show the PCM encoding of ramp signal using MATLAB. Wherein, first plot show the analog ramp signal with the magnitude varying from -1 to 1, the second plot consists of sampled data from the first plot and the third plot gives the quantized signal. The second part of the Fig. 2 show the signal encoded from the above mentioned ramp signal.

CVSD encoding of sinusoidal signal is done in MATLAB. This encoded signal is converted as .Coe file. The .Coe file is given to IP core generator, then stored in the ROM as a .Mif file. Fig. 3. show the CVSD encoding of sinusoidal signal using MATLAB. Wherein, first plot show the analog sinusoidal signal with the magnitude varying between -10 and 10, the second plot consists of sampled data from the first plot and the third plot give its quantized signal.

Similarly, the second part of the Fig. 3 show the signal encoded from the above mentioned sinusoidal signal. From both of the Figs. 2 and 3, the difference in encoded signals can be observed clearly.

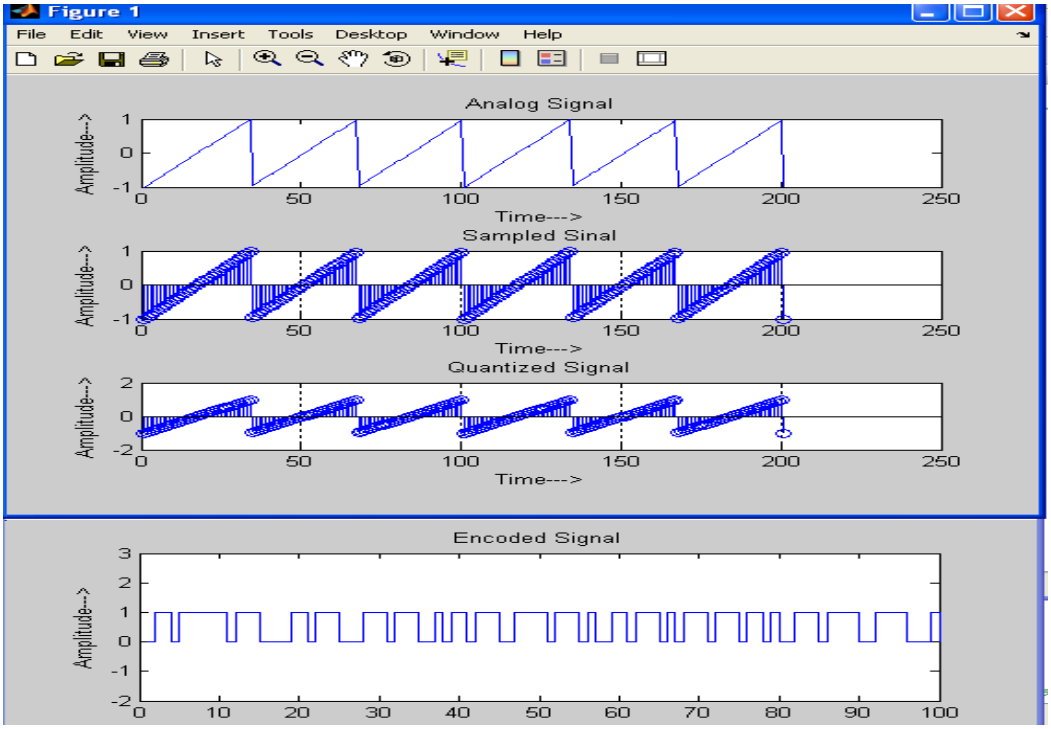

Fig. 2.PCM encoding of ramp signal.

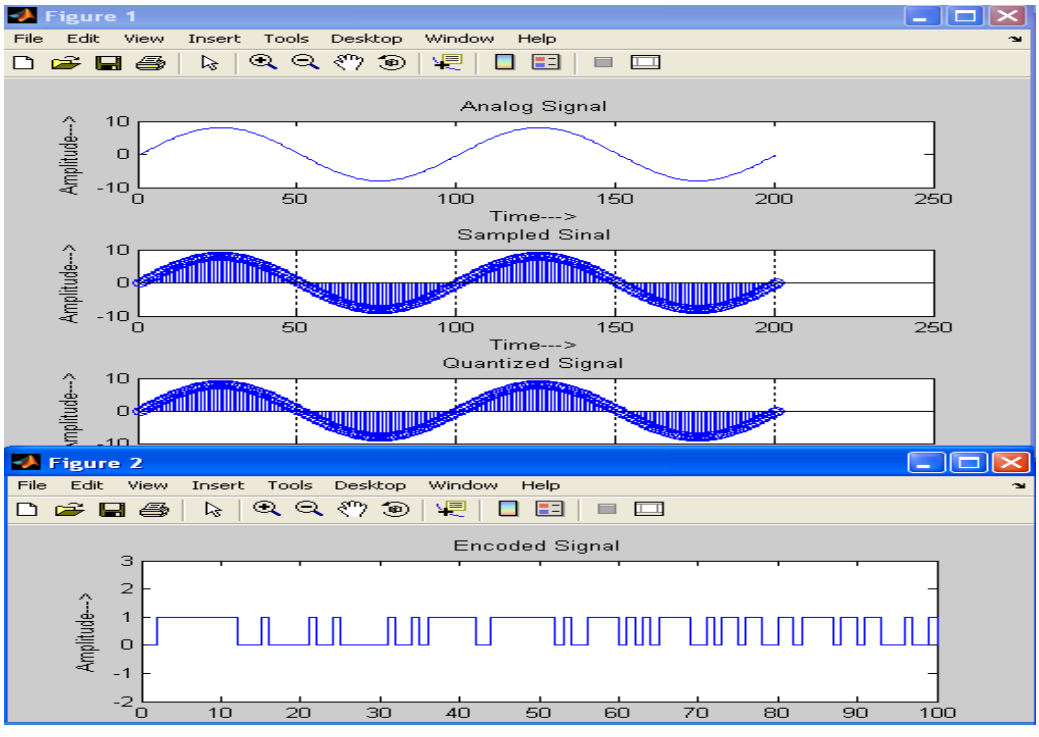

Fig. 3.CVSD encoding of Sinusoidal signal.

IV. RESULTS FROM BOOKSIM

Highly modular level implementation makes BookSim more flexible. The proposed hybrid star mesh topology is simulated using BookSim considering various nodes *viz.* 4, 6, 16, 32, 64, and 128. The results are obtained for packet latency average, network latency average and the injected packet rate average as given in Table 1. Also, the results are compared with the predefined topologies of the BookSim which are: Torus topology with 8^2, 9^2, 10^2, and 11^2 nodes; and fat-tree topology with 4^3, 5^3, and 6^3 nodes. The comparative results are shown in Fig. 4, 5 and 6.

Table- I: Comparative results from BookSim

Type of Topology	Packet latency average	Network latency average	Injected packet rate average
HYBRID STAR MESH 4	15.7427	15.0581	0.01015
HYBRID STAR MESH 6	18.0833	17.245	0.009825
HYBRID STAR MESH 16	23.479	21.4913	0.00992292
HYBRID STAR MESH 32	28.1152	23.9512	0.0100406
HYBRID STAR MESH 64	31.1759	25.3845	0.0100281
HYBRID STAR MESH 128	33.6657	26.3218	0.00999766
TORUSK8N2	46.9979	46.9979	0.150281
TORUSK9N2	41.2111	41.2111	0.149173
TORUSK10N2	51.3173	51.1791	0.14959
TORUSK11N2	83.037	82.825	0.149512
FATTREEK4N3	19.9886	19.9886	0.599383
FATTREEK5N3	20.6517	20.6517	0.600148
FATTREEK6N3	21.0778	21.0778	0.599946

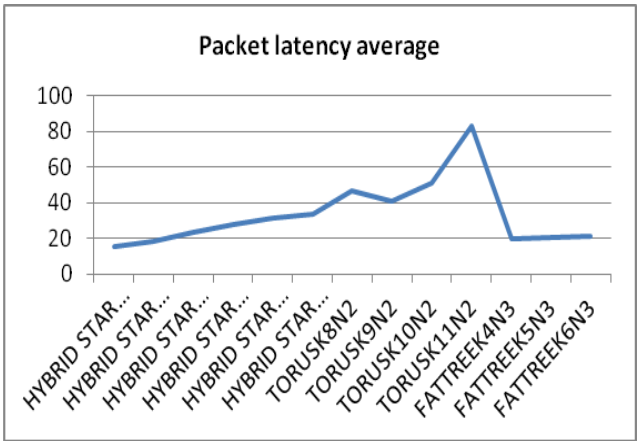

Fig. 4. Comparison of packet latency average using BookSim.

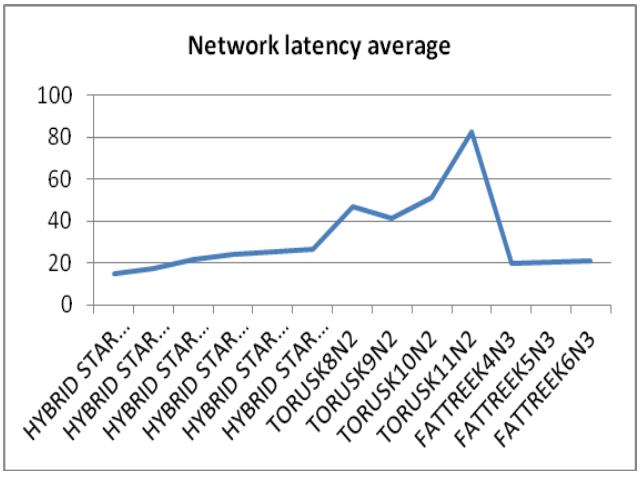

Fig. 5. Comparison of network latency average using BookSim.

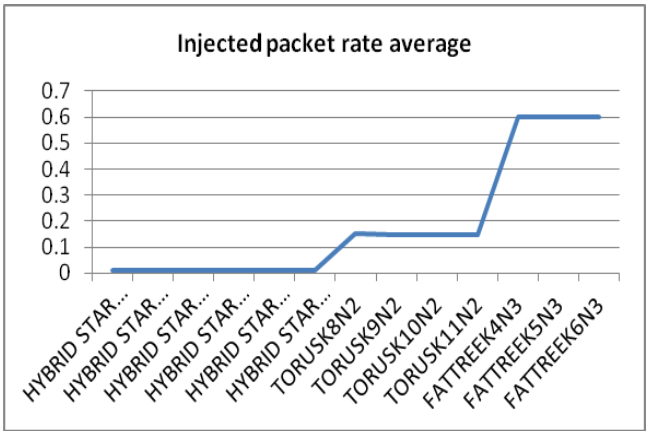

Fig. 6. Comparison of injected packet rate average using BookSim.

V. CONCLUSION

In this work, the BookSim a flexible and detailed simulator specialized for Network-on-Chip architectures is used to validate the proposed topology. The simulator offers a large degree of network customization and numerous network component designs. The Network parameters tested using BookSim simulator. Previously, the proposed topology was simulated on real time data (using CVSD, PCM, ADPCM decoded data) and synthesized on various FPGAs. For better validation of network parameters like network latency and packet latency proposed topology is tested using BookSim simulator and it can be concluded that the proposed hybrid topology of Network-on-Chip architecture is better compared to the other prebuilt topologies of BookSim.

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AUTHORS PROFILE

Vamshi Talla, is a Research Scholar in the departement of ECE at JNTU Hyderabad and working as Assistant professor at Talla Padmavathi College of Engineering, Warangal. He secured B.Tech degree in ECE in 2004 and MTech in VLSI system Design in 2006 from JNT University Hyderabad. He has 4 publications out of which two papers got best paper award, he is a member of IEEE,IETE and CSI. His area of research include VLSI, particularly NOC architectures.He has received various awards like Appreciation award at SMARTCOMM international conference in courtesy with CSI and Pune College of Engineering. He was part of three Indian Higher Education Delegation of AICTE to visit USA, UK and Canada.

Dr. T. Satya Savithri, is a Professor in the Department of ECE at JNTU Hyderabad.She has completed her Ph.D in Digital Image Restoration Techniques, JNTU in 2006,M.E in Microwave and Radar Engineering, Osmania Uiversity in 1997, B.Tech in Electronics and Communication Engineering, NIT Warangal (REC) in 1992.She has worked as R & D Engineer, Co ordinator R&D cell JNTUH, Head of Department ECE , JNTUH, officer in charge Examinations JNTUH College of Engineering.
She has a total of 110 publications, 50 Inter National Journals, 5 National Journals, 2 Patents and 9 Ph.Ds under her guidance.Her areas of Research include Digital Image processing, VLSI Design, Antenna design, Satellite communications, Robotics, channel and propagation models.