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An Area Efficient Wallace Tree Multiplier using Modified Full Adder

Abdul Bari M., Baskaran M., Siva Nandini B.

Abstract: ***Multipliers play a significant task in digital signal processing applications and application-specific integrated circuits. Wallace tree multipliers provide a high-speed multiplication process with an area-efficient strategy. It is realized in hardware using full adders and half adders. The optimization of adders can further improve the performance of multipliers. Wallace tree multiplier with modified full adder using NAND gate is proposed to achieve reduced silicon area, high speed and low power consumption. The conventional full adder implemented by XOR, AND, OR gates is replaced by the modified full adder realized using NAND gate. The proposed Wallace tree multiplier includes 544 transistors, while the conventional Wallace tree multiplier has 584 transistors for 4-bit multiplication.***

Keywords: Wallace tree multiplier, application - specific integrated circuits, area-efficient strategy, transistors.

I. INTRODUCTION

Multipliers have significant importance with the development of digital computers. Adding and multiplying two numbers is elemental in most systems. It considered as frequently used arithmetic operations. These operations consume maximum execution time. Hence it creates a demand for a fast multiplier. The need for fast processing has been rising due to the effect of intensifying signal processing applications. Power consumption is a major problem in the multipliers. It is good to lessen the number of operations involved to minimize power consumption, thus diminishing the dynamic power. This reduces the total power consumption. Thus the demand for low power and high-speed multiplier has improved.

The types of multipliers are Sequential multiplier, Booth multiplier, Array multiplier, combinational multiplier, Wallace tree multiplier. An efficient multiplier must include good accuracy, reduced area, low power consumption, high speed. The Booth multiplier uses an algorithm for the multiplication of signed-2's complement integers. Combinational Multipliers performs multiplication of two unsigned binary numbers as well as signed numbers. The product is allied with the bit position in the multiplier after multiplying all the bits. The final result is formed by adding the resulting products. An array multiplier is based on repeated accumulation and shifting method. All the bits are multiplied to obtain the partial product. The partial products are shifted by bit sequences and summed up. The addition is done by carry propagation adder. To multiply a multiplicand of n bit and a multiplier of m bit using an n-bit adder, a sequential circuit is developed to process a partial product and it is reiterated m times. It is known as the sequential multiplier. It is widely used for reduced area applications. The multiplication process is separated into different sequential stages. In each stage, some partial products are acquired and summed to a collected partial sum. This sum is subjected to shift operation to line up the collected sum with the obtained partial product of the subsequent stages. Thus each stage of a sequential multiplier includes three operations such as partial product generation, the addition of partial products to obtain the collected partial sum and partial sum shifting. A Wallace tree multiplier is a proficient hardware implementation used for multiplying two numbers. The partial products are reduced and a carry select adder is used for the accumulation of the partial product.

Based on the analysis, it is well-known that the Wallace tree multiplier is a high-speed multiplier employed to do signed multiplication. But it has complex circuitry. Hence in the proposed system, the Wallace tree multiplier is designed by modified full adder realized by NAND gate. NAND gate is used to ease the fabrication System.

II. LITERATURE SURVEY

Kokila Bharti Jaiswal et al proposed a modified full adder by multiplexer [6]. Here a multiplexer is used in the place of XOR gate as in the conventional full adder. In Wallace tree multiplier the obtained partial products are separated into different stages. On every stage, three bits are added using a full adder. Of all inputs, an input and its complement are given as input to the first multiplexer. The left behind inputs is provided to the XOR gate. The output will be the select line of the two multiplexers from the XOR gate. The second multiplexer's inputs are the bits excluding the carry bit.

Waters et al proposed a Reduced Complexity Wallace Multiplier Reduction technique [8]. The half adders in the multiplier are minimized by the multiplier reduction method. It includes the customized Wallace structure by diminishing the partial product array.

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* Correspondence Author
Abdul Bari M*., Department of Electronics and Communication Engineering, National Engineering College, Kovilpatti, Tamil Nadu, India. Email: bariabdhul17@gmail.com
Baskaran M., Department of Electronics and Communication Engineering, National Engineering College, Kovilpatti, Tamil Nadu, India. Email: mbaskar1121998@gmail.com
Siva Nandini B., Assistant Professor, Department of Electronics and Communication Engineering, National Engineering College, Kovilpatti, Tamil Nadu, India. Email: sivanandinima@gmail.com

The matrix is divided into a set of three rows. All the set of three bits in each column is summed using full adders like the conventional reduction. A set of two bits in each column is passed to the next stage without processing. Any available single bits are also given to the subsequent stage like the conventional reduction technique.

Dakupati et al proposed Wallace tree multiplier using compressor and divide and conquer tree adder (Sklansky adder) [1].

In the proposed structure of full adders is replaced by compressors, and Sklansky tree adder is used instead of the final carry propagate stage. The first stage consists of a full adder. The second stage has 4:2 compressors which group two full adders. In the third stage, 5:2 compressor is used to combine 3 full adders and so on. In this way, compressors are used to implement the grouped full adders in the original structure.

Shahebaj Khan et al proposed Energy Efficient CMOS Full Adder for customized reduced complexity Wallace Multiplier [10]. The Multiplication of two numbers giving partial products obtained by multiplying two numbers is placed in a tree structure and a group of two bits is reduced using half adder in the first stage. The second stage includes a set of three bits which is reduced by a full adder. The final adder is used to sum up the result of the second stage to get the final product. The system uses an energy-efficient full adder instead of a conventional full adder.

Kartikeya Bhardwaj et al proposed Approximate Wallace Tree Multiplier which can be used for error-tolerant applications [4]. The design of the multiplier is optimized by bit-width aware approximate multiplication algorithm. The horizontal critical path is minimized to half using the carry-in prediction technique. Jagadeshwar Rao M et al proposed a Wallace tree multiplier by means of Booth Recoder [7]. It is implemented with the help of the Booth recoders and compressor adders. The compressors are used in place of full adders in the design. The carry select adder is used to replace the final carry propagate stage.

III. PROPOSED SYSTEM

The proposed system includes the Wallace tree multiplier implemented with a modified full adder realized by NAND gates. It has the following three stages: (i) Partial Products generation (ii) Partial Products addition (iii) Final addition as given in fig.1.

The first step is the generation of partial products. Every bit of multiplier is multiplied with multiplicand to generate the partial product.

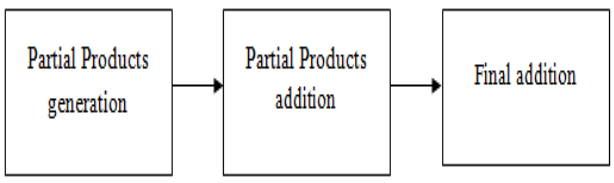

Fig. 1.Block diagram of Wallace Tree Multiplier

Consider 4x4 multiplication of multiplicand $a_3a_2a_1a_0$ and multiplier $b_3b_2b_1b_0$, the partial products a_3b_3, a_3b_2, a_2b_3, a_2b_2, a_1b_3, a_3b_1, a_1b_2, a_0b_3, a_3b_0, a_2b_1, a_1b_1, a_0b_2, a_2b_0, a_1b_0, a_0b_1, a_0b_0 are generated using AND gate. The generated partial products have diverse weights depending on the place of multiplier bits.

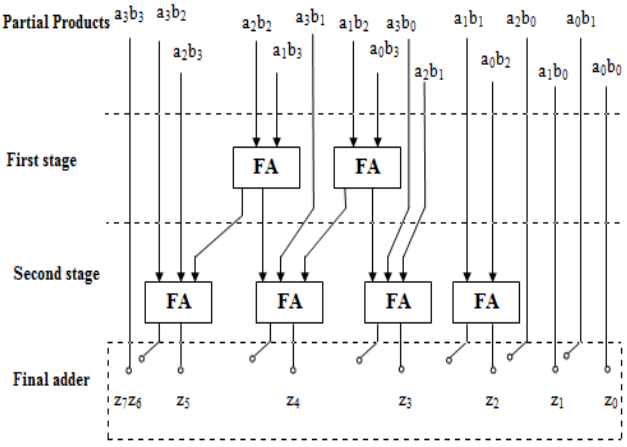

Fig. 2.Proposed Wallace tree multiplier using modified full adder

The second step includes the grouping of three adjacent rows and it is reduced by using full adders only. The conventional Wallace tree multipliers use full adders and half adders for reduction. In the proposed system, the half adders are replaced by full adders. A set of three or two bits in each column is summed by full adders. A single bit in any column is not processed and moved to the successive stage in the identical column. Until only two rows remain the reduction process is iterated in the consecutive stages. The final step includes the addition of the remaining two rows by the full adder. For 4x4 multiplication, the accumulation of partial products in different stages is given in fig. 2.

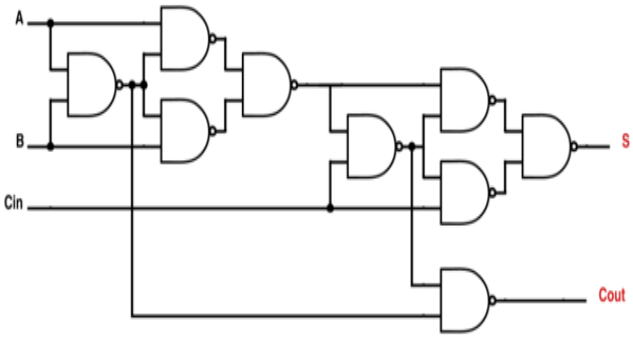

Fig. 3.Full adder realization using NAND gate

Full adder using XOR, AND, OR gates have circuit complexity. Since the XOR gate employs the majority of the power consumption in the adder circuit, XOR gates are replaced by NAND gates as in fig. 3. So the proposed system uses the modified full adder implemented by NAND gate.

IV. EXPERIMENTAL RESULT ANALYSIS

The proposed 4x4 Wallace tree multiplier implemented by modified full adder is simulated in Microwind DSCH tool. The schematic diagram of the partial product generation is given in fig. 4.

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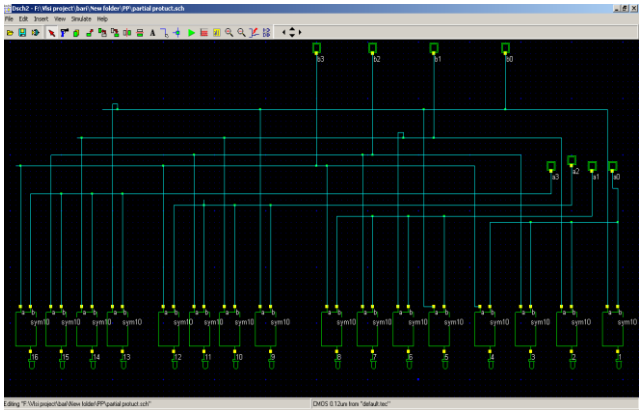

Fig. 4.Schematic diagram of Partial Product Generation

The schematic diagram of NAND gate simulated in Microwind DSCH tool is provided in fig. 5.

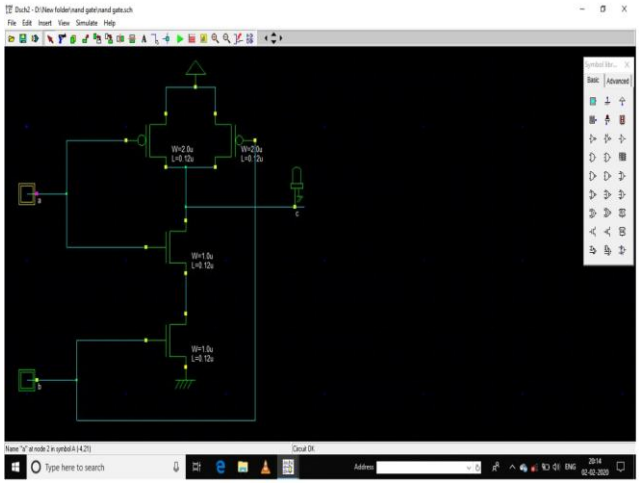

Fig. 5.Schematic diagram of NAND gate

The schematic diagram of modified full adder using NAND gate simulation in Microwind DSCH tool is presented in the fig. 6.

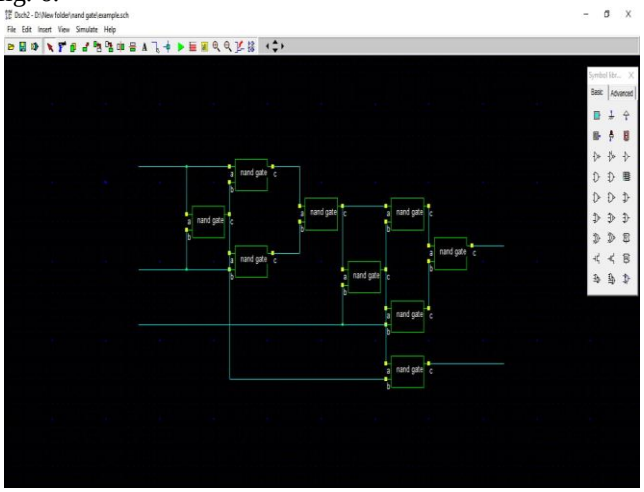

Fig. 6.Schematic diagram of modified full adder using NAND gate

The schematic diagram of the proposed 4x4 multiplier by modified full adder is given in fig. 7.

The comparison between the number of transistors used for designing 4- bit conventional Wallace tree multiplier and 4-bit proposed Wallace tree multiplier using modified full adder is provided in table 1.

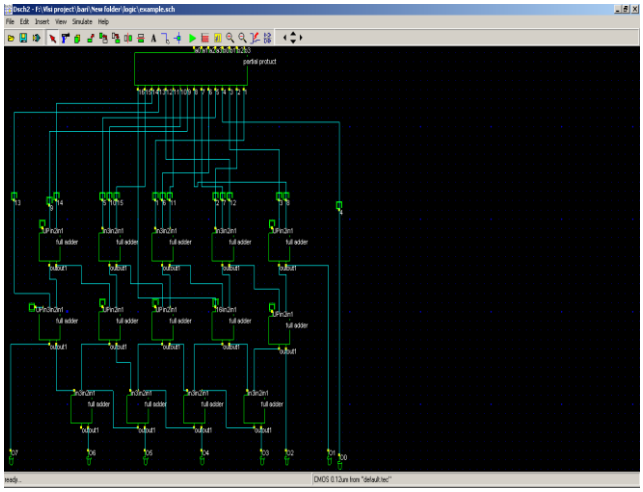

Fig. 7.Schematic diagram of proposed Wallace tree multiplier

Both the conventional and proposed Wallace tree multiplier uses AND gates for partial product generation. Each AND gate includes 6 transistors for its implementation. Here 4-bit multiplication is considered for comparison. Hence 96 transistors are used for partial product generation.

Table 1: Comparison between conventional Wallace tree multiplier and proposed Wallace tree multiplier

Conventional Wallace tree multiplier	**Transistor Count**
AND gate	96
Half adders	120
Full adders	368
Total count	584
Proposed Wallace tree multiplier	**Transistor Count**
AND gate	96
Half adders	-
Full adders using NAND gate	448
Total count	544

In the conventional Wallace structure, 6 half adders are used. Each half adders requires 20 transistors; 120 transistors are used for its implementing 6 half adders. Eight full adders are used in the conventional Wallace tree technique. Full adders are realized using XOR, AND, OR gates. It requires 46 transistors; eight full adders are implemented by 368 transistors. Thus a total of 584 transistors are used in conventional Wallace tree multiplier. In the proposed system half adders are replaced by full adders. Thus it uses 14 full adders. In the proposed system, the full adder is realized by NAND gates. Each NAND gate is implemented by 4 transistors. A full adder includes 8 NAND gates, so 448 transistors are used for its implementation. Including the partial product generation, the proposed system is implemented by a total of 544 transistors. Thus this technique reduces 40 transistors for 4-bit multiplication.

V. CONCLUSION

An area-efficient Wallace tree multiplier implemented by modified full adder is proposed. The power utilization of the full adder is minimized by replacing XOR, AND, OR gates using NAND gate. Wallace tree multiplier is used because it reduces steps in the multiplication process. The reduction of multiplication steps leads to area reduction and increase in speed of multiplication process. In conventional full adder, the transistor count is high compared to the full adder modified using NAND gate. So the area essential for the proposed multiplier is comparatively low. The transistor count of conventional 4x4 Wallace tree multiplier is 584 whereas for the proposed Wallace tree multiplier the transistor count is 544. Thus the proposed system reduces 40 transistors in comparison with the conventional Wallace tree multiplier.

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AUTHORS PROFILE

Abdul Bari.M, is an undergraduate student in department of Electronics and Communication Engineering at National Engineering College, Tuticorin, Tamil Nadu, India. His research interest is CMOS VLSI design.

Baskaran.M, is an undergraduate student in department of Electronics and Communication Engineering at National Engineering College, Tuticorin, Tamil Nadu, India. His research interest is CMOS VLSI design.

Siva Nandini .B, is an Assistant Professor in the Department of Electronics and Communication Engineering at National Engineering College, Tuticorin, Tamil Nadu, India. She received her B.E. Electronics and Communication Engineering degree from Government College of Engineering College, Tirunelveli, Tamil Nadu in the year 2014. She completed her M.E. Embedded System Technologies from Anna University Regional Campus, Coimbatore, Tamil Nadu in 2016. She has 2 years of teaching experience. Her research interest is Embedded networking, IoT.