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Design and Implementation of Vedic Multiplier

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Abstract: ***The ancient vedic mathematics has a set of 16 sutras and 13 subsutras. These sutras give suitable method for arithmetic calculations. The vedic formulas requires less time than the regular formulas or method of calculations [1].***

Multiplier is an important block in many digital systems. This paper presents a 32-bit vedic multiplier using Urdhva Tiryagbhyam sutra of ancient vedic mathematics. The 32-bit vedic multiplier is implemented using 16-bit multipliers and adders. The 16-bit multipliers are basic blocks in the design by which the input bits are multiplied and their result are added by using the adders. The vedic multiplier can be used in many fast computing processors because of their less time delay and less number of slice LUTs. The result discusses the delay and number of slice LUTs for the implemented 32-bit multiplier. The paper also discusses the methodology of implementation.

Index Term: Urdhva Tiryagbhyam, Vedic Mathematics, Vedic Multiplier, VHDL, Xilinx Spartan-6 FPGA.

I. INTRODUCTION

The multiplication is an important process in mathematics. The multiplication process is carried out in many digital processors like microprocessors, microcontroller and many processors. Multiplication requires number of clock cycles, that results in increasing time consumption. The regular methods for multiplication may require more area or delay. The ancient vedic mathematical formulas can be used in order to achieve less area and delay [7]. In literature there are many architectures based on vedic algorithms and from that it can be concluded that vedic algorithms requires less time than the conventional methods. The architectures are based on different implementation methods such as carry select adders, ripple carry adder, multiplexers, compressors [1], [3], [4], [6], [10]. The paper is organized as follows. Section II deals with literature review of vedic multiplier. Section III gives the methodology for vedic multiplication using Urdhva Tiryagbhyam sutra, based on ancient vedic mathematics. Section IV deals with proposed architectural work in which each block in the proposed design is explained. Section V is Result and it explains the result of the proposed design. Section VI is conclusion and section VII comprises of references.

multiplication with sign bit and exponent calculations.

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II. EXISTING THEORY

Multiplication of floating point numbers is greatly significant in many DSP applications Urdhva Tiryagbhyam sutra of vedic mathematics is used for the design and implementation of single precision floating point multiplier using Verilog. This design implements floating point

The results show different parameters in Xilinx ISE 10.1 [2].

Full adders are designed for a 16-bit vedic multiplier to decrease number of slices and delay. The results obtained are compared and it is found that the reformed full adders have less delay. The design is implemented using four adders of different techniques such as full adder using two half adders and an OR gate. Second modified full adder is designed by using XOR gate and 2:1 multiplexer, third modified full adder by using two 4:1 multiplexer and fourth modified full adder using a combination of XOR gate, XNOR gate and a 2:1 multiplexer. After comparing the results, they concluded that the third modified full adder has better performance [3].

Gate diffusion input (GDI) is a method used for describing the structure of low-power digital combinatorial circuit. Consumption of power, delay that is produced and complexity of the circuit are reduced using this technique; thereby it maintains less complexity in logical layout. The GDI technique is implemented using two transistors for a deep range of complex logic design [4].

A high speed 32-bit vedic multiplier is designed. For addition of partial products in a 32-bit vedic multiplier Kogge stone adder and a ripple carry adder is used. Two multipliers are implemented using these two methods and results are compared with these two multipliers [5].

In 8-bit multiplier which is implemented using Urdhva Tiryagbhyam sutra, the partial product addition is realized using carry skip technique. A digital processor requires a multiplier as it is a basic block in the processor [6].

A 32-bit vedic multiplier is proposed using one carry save adder. The input of multiplier is arranged in two 16-bit numbers to apply it stepwise using Urdhva Tiryagbhyam sutra and the partial product is added using one carry save adder thus reducing the hardware blocks in the circuit [7].

The processors are integrated into one chip as demand of complex processors is increased. But the load on the processor is not reduced. To reduce this load, the main processor is equipped with co-processors [8].

Design of a hybrid FIR filters using vedic multipliers and fast adders is todays need in many DSP processors. FIR filters play a significant role in the field of digital signal processors to eliminate noise suppression in electro cardio graph, imaging devices and the signal stored in analog media. So filter evaluation is accomplished to reduce the noise level.

Multipliers and adders play a vital role in determining the performance of FIR filter. They have proposed modified Annuprya vedic multiplier methods with Kogge Stone fast adder for implementation in the direct form FIR filter [9]. Multipliers play a major role in today's digital signal processing and various other applications. Both signed and unsigned multiplications are required in many computing applications. This work proposes the design of efficient signed multiplier using vedic mathematics [10].

III. METHODOLOGY

The ancient vedic mathematics consists of a set of 16 sutras or main formulas and their 13 corollaries which can be efficiently used to solve mathematical calculations. One of the sutra is Urdhva Tiryagbhyam which means vertically and crosswise. This sutra can be used to perform a multiplication. The process of multiplication by using Urdhva Tiryagbhyam sutra is as follows, First step is to multiply the first digit that is left hand most digit of multiplicand with first digit of multiplier. The product is written as first digit in the answer. In second step multiply second digit of multiplicand with first digit of the multiplier and first digit of the multiplicand with second digit of multiplier, add the product. The result is written as second digit in the answer. Third step is to multiply second digit of multiplicand with second digit of multiplier, write the product as third digit in the answer.

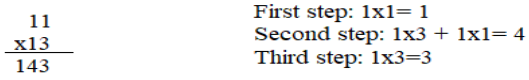


Fig. 1. Multiplication using Urdhva Tiryagbhyam sutra

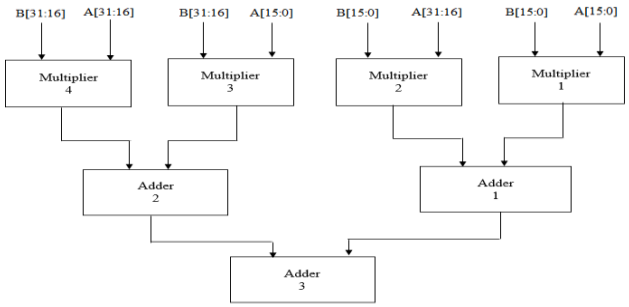
Figure 1 show an example of multiplication of two numbers using Urdhva Tiryagbhyam sutra from vedic mathematics.

IV. PROPOSED WORK

A. Design Steps

1. Apply multiplicand and multiplier each of sixteen bits to the multiplier.
2. Add the output of multiplier 1 and multiplier 2 by using adder 1, add output of multiplier 3 and multiplier 4 using adder 2.
3. Add result of adder 1 and adder 2 using adder 3.

The block diagram of proposed work is as shown in figure 2. For a 32-bit vedic multiplier there are four 16-bit



multipliers, one 32-bit adder and two 48-bit adders are used.

The input multiplier and multiplicand are divided into two 16-bit numbers. The process starts with assigning inputs to the four multipliers. For multiplier 1, the first and second input will be A [15:0] and B [15:0].

For multiplier 2, the first and second input will be A [31:16] and B [15:0]. For multiplier 3, the first and second input will be A [15:0] and B [31:16]. For multiplier 4, the first and second input will be A [31:16] and B [31:16].

Fig. 2. Block Diagram of Proposed Work

The output of multiplier 1 will be of 32-bit in which the least 16 bits are carried out directly to the output. The remaining 16 bits are concatenated with 16 zeros in order to add the result.

The adder 1 which is of 32-bit will have input from multiplier 1 and multiplier 2. Adder 2 is of 48 bit, the input to the adder is zero concatenated output of multiplier 3 and multiplier 4.

In last step, the adder 3 will add the result of adder 1 and adder 2.

B. Multiplier Design

For the proposed design we are using four multipliers. The initial steps in the procedure requires four multipliers in order to apply the inputs multiplicand and multiplier. Each multiplier in the design is of sixteen bits.

C. Adder Design

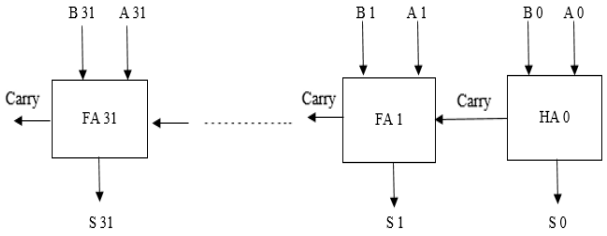


Fig. 3. Block Diagram of 32-bit Adder

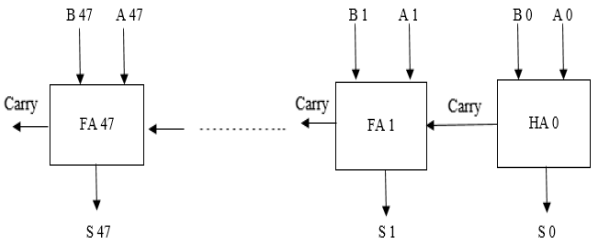


Fig. 4. Block Diagram of 48-bit Adder

Fig. 5.

The figure 3 and figure 4 shown above are block diagram of 32-bit adder and 48-bit adder respectively. The proposed 32-bit multiplier requires one 32-bit adder and two 48-bit adders for partial addition. Each adder is implemented by using a combination of half adder and full adder.

Figure 3 show a 32-bit adder in which there are one half adder and thirty-one full adders. Similarly, for 48-bit adder there are one half adder and forty-seven full adders.

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V. RESULT

A. RTL Schematic

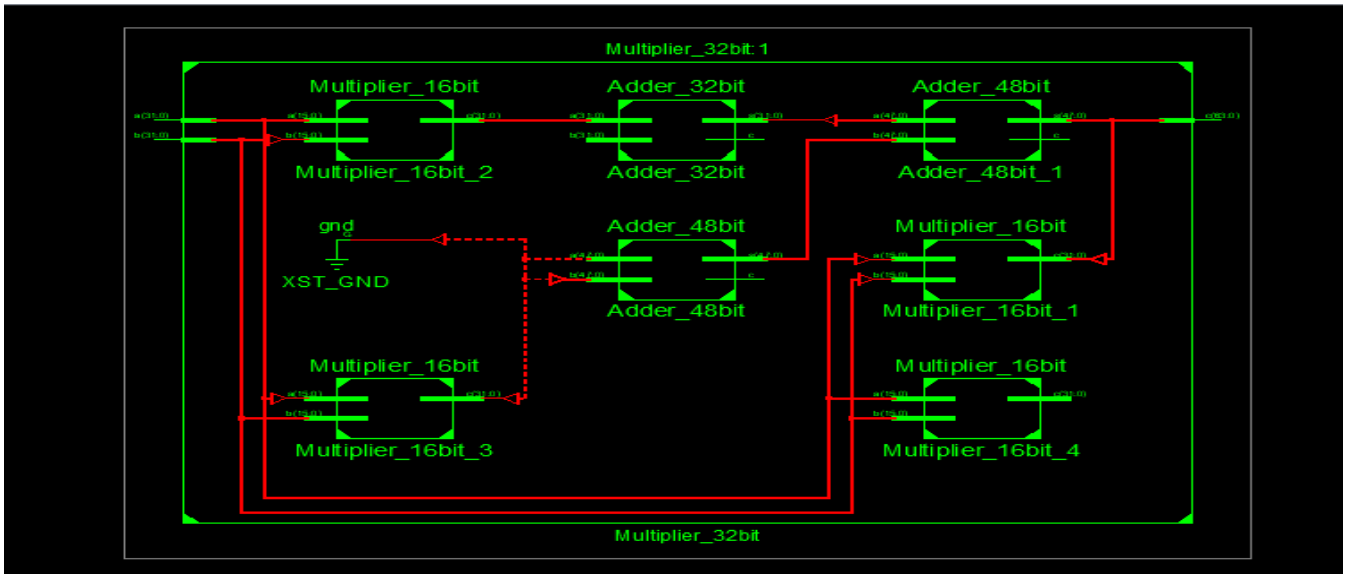

Fig. 6. RTL Schematic

B. Simulated Result

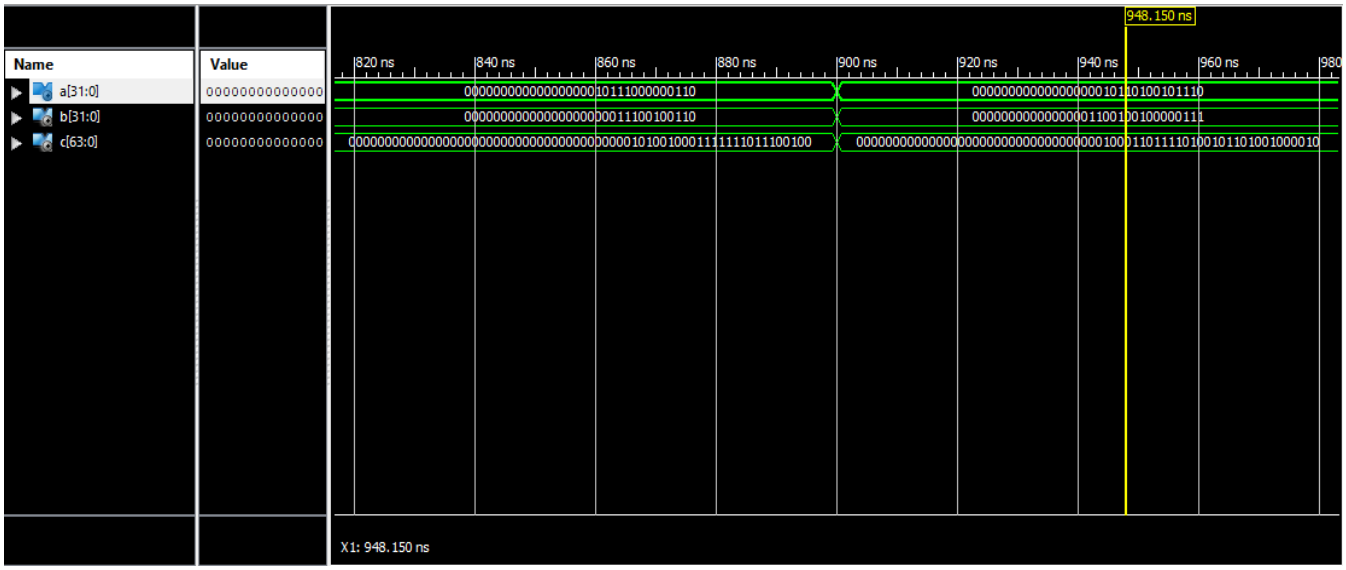

Fig. 7. Output of Proposed Design

The proposed 32-bit vedic multiplier is implemented by using VHDL language and simulated on Xilinx ISE 14.7 software.

The figure 5 and figure 6 show the RTL schematic and output of the proposed design respectively. Figure 6 shown above is the output of proposed 32-bit vedic multiplier in which it shows that 32-bit multiplicand and 32-bit multiplier as input and output is of 64 bits.

C. Performance Parameter Analysis

Table I below describes the different parameters in the proposed design.

The number of slice LUTs used are 1758 out of 27288, number of bounded IOBs are 128. The combinational path delay is 54.037 ns.

Table I. Performance Analysis

Parameter	Used	Available
Number of Slice LUTs	1758	27288
Number of bounded IOBs	128	218
Combinational Delay	54.037 ns	

VI. CONCLUSION

A 32-bit vedic multiplier is designed by using Urdhva Tiryagbhyam Sutra of ancient vedic mathematics using VHDL and simulated on Xilinx ISE 14.7.

The performance parameters like number of slice LUTs, number of bounded IOBs and combinational delay are analyzed and it is found that the number of slice LUTs used are 1758 out of 27288, number of bounded IOBs used are 128 and combinational delay is 54.037ns.

The multiplier is designed using four 16-bit multiplier, one 32-bit full adder and two 48-bit full adders. The hardware requirement is large thus increasing the time delay. The basic building blocks should be reduced to achieve less time delay. The work can be extended to 64-bit. The adders used can be remodified using basic gates and multiplexer.

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