

Memory Arbitration in DDR3



S. V. Vijayalakshmi, A. Apsara, K. Preetha, S. Cammillus

Abstract: Modern applications need expeditious, speed parallel processing elements with desired output within the stipulated time. As sundry applications increase demands expeditious processing, low power consumption, truncated deadlock of recollection. Hence, memory deadlock, memory starvation, and allocation of memory for genuine-time applications are the real challenges of the desired real world. The work fixates on abbreviated power consumption, deadlock for the inputs onto the output. DVFS (Dynamic Voltage and Frequency Shifting) and CoC (Cloud of chips) are acclimated to abbreviate the deadlock and to utilize the recollection efficaciously for input onto output. The results show the potency consumption as truncated compared to the antecedent results.

Keywords: Arbitration, Deadlock, Memory Starvation, Multi processor System on Chip

I. INTRODUCTION

A CPU is also kenneed as the main processor. The processor is an electronic circuit that executes all the commands of the utilizer and provides the desired output. The evolution of microprocessors commenced in the 1970s. The very first microprocessor introduced is Intel 4004 designed by Federico Faggin of the Intel Company. It is a single-chip 4-bit microprocessor which consisted of 2300 transistors. Very-Large -Scale-Integration (VLSI) plays a vital role in designing integrated circuits amalgamating several chips of different functions. Different logical transistors are integrated over the same board which perform different processes. Cellphones, Digital Televisions, Video Games require intricate parallel processing systems. General computer architecture may not provide the required efficiency for such systems. Nowadays, we prefer Multi Processor System on Chips to perform parallel processing. An MPSoC is a system-on-chip- a VLSI system which encompasses virtually all the components required for an embedded

application. It uses multiple programmable processors as system components. All the system components are combined with each other by on-chip interconnect. It is either bus-based communication or Networks-on-Chips. The addition of many processing cores on a single chip needs an efficient on-chip communication MPSocs are widely classified as homogeneous and heterogeneous.

MP So Cs mainly focus on parallel processing. Embedded computing applications typically require genuine concurrency, not just the ostensible concurrency of a multitasking operating system running on a uniprocessor. Task-level parallelism is very consequential in embedded computing. Most of the systems that rely on SoCs perform intricate tasks that are composed of multiple phases. Sharing tightly coupled recollection in MPSoCs is a promising approach to ameliorate program flexibility and to facilitate the constraints led by area and potency. TCM (Tightly Coupled Memory) avails in maintaining low latency (the time between initiating a request for recollection until it is retrieved by a processor). The exponential increase in involution in MPSoCs lead to increment in chip temperature which results in chip wear-out effects. With the growing System on Chip technology, MPSoC's had many constraints that were left unresolved. The constraints include recollection starvation, access latency, incremented deadlock, power consumption and memory shortage. Most of the microprocessor architecture today, aims for highest possible performance, additionally concentrating the constraints of area and power consumption.

II. LITERATURE SURVEY

Many systems are been proposed on MPSoCs on consideration with deadlocks, recollection starvation, incremented latency and power consumption. But there exists no system focusing on zero SRT (Switching Response Time) in a video processing unit.

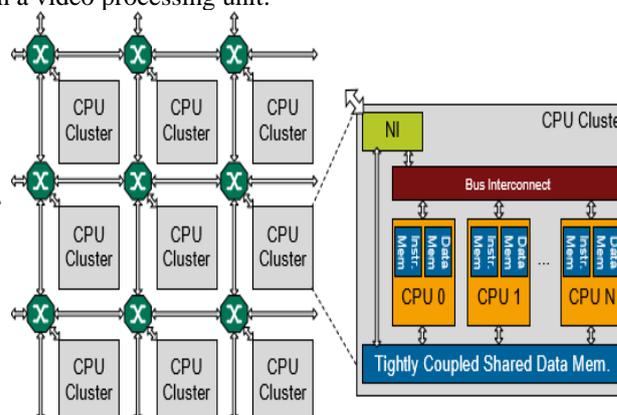


Fig. 1. Shared data memory using Bus Interconnect

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In [1] different memory architectures and their connection to NoC are compared. Concerning the comparison, the analysis of energy consumption on both cluster and NoC level utilizing different recollection architectures are performed. Core VA - MpSoC is utilized in streaming applications embedded systems like signal and video processing.

The hierarchical interconnect sanctions for different recollection architectures to tightly couple scratchpad recollections to CPUs. In first recollection architecture within a cluster, CPUs can access each other's local scratchpad recollection in a Non-Uniform Memory Access (NUMA) fashion via a bus interconnect, which increases the access latency (Refer fig. 1). In second recollection architecture, due to the uniform memory access (UMA) within a CPU cluster, replicating data can be omitted, which results in high performance and high resource efficiency.

In [2] HyHeMPS (Hybrid Hermes Multi-Processor System on chip) is proposed to concentrate on efficient communication over immensely colossal distances. It provides a balance over the on-chip communication constraints since it maintains the performance of a 4*4 NoC preserving up to 25% of the chip area.

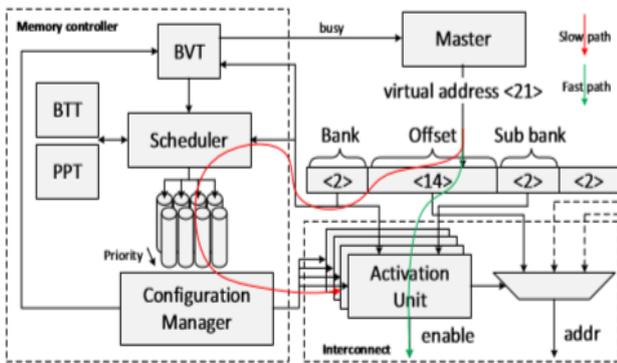


Fig. 2. Queue based Memory Management Unit

In [3] a queue-based memory management unit which cumulates the low latency access of shared tightly coupled recollection with the flexibility of a traditional recollection management unit. Memory banks are introduced in Q-MMU (Queue-based Memory Management Unit) (Refer fig 2). Each recollection bank is accessed with the same delay regardless of the specific data width of programming.

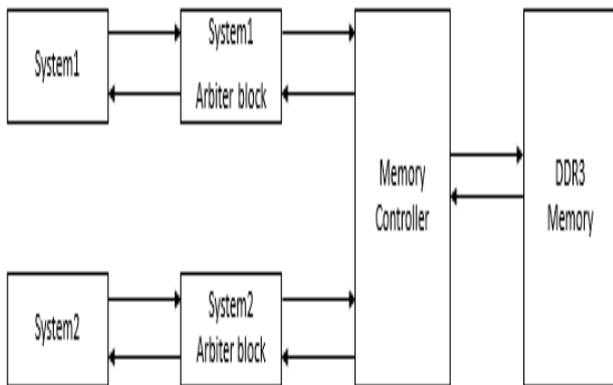


Fig. 3. Arbitrer blocks for individual systems

In [4] an arbitrer is designed to eschew collisions that transpire when two systems directly access the memory. The arbitrer directs the flow of read/indite commands from/to the

memory. In this architecture, each system is provided with an arbitrer that is connected to a recollection controller followed by the DDR3 recollection unit (Refer fig 3). The transfer of data from the system to recollection has switching branches and data is read/inscribe following FIFO (First In First Out) scheduling algorithm.

In [5] various arbitration algorithms are discussed which include Static Fine-tuned Priority Algorithm, Variable Priority Algorithm, Round-Robin, and lottery bus architecture. In the Static Fine-tuned Priority Algorithm, each master is assigned a fine-tuned priority value. When several masters request simultaneously, master with the highest priority will be granted access and is achieved by a centralized arbitrer. A variable priority algorithm is one which divides the execution time on the bus into time slots and allocates the time slots to adapters requesting the utilization of buses. In the Round-Robin algorithm, each cycle has one master with the highest priority. The Lottery arbitration algorithm is predicated on probability, the lottery manager accumulates the requests of bus access from all the masters. Each master is assigned several lottery tickets, the respective master with lottery proximate to the number is most likely granted access.

III. PROPOSED WORK

The NOC (Network on-chip) is widely used to maintain an opportune communication between the networks which plays a vital role in the parallel processing of a processor. In this paper, we consider any MPSoC been built for a video processing application. In such a case, the channel, the user lay eyes on is provided with the highest resolution and the other channels which run in the backend will be provided with the lowest resolution. We aim to provide zero SRT (Switching Response Time) when there is a change in the choice of channels. The components in the MPSoCs includes components that initiate transactions called masters and those who respond to transactions called slaves (recollection and peripheral contrivances) and a common shared bus. The proposed single-arbitrer architecture avails in the minimization of the chip area, power consumption, and critical path. The arbitrer avails in sharing the resource efficaciously and is employed in such a way that only one master accesses the bus at a time. We compare the fixed and variable priority algorithm in this paper. In variable priority algorithm, each master is availed with time slots. When one master carries on read /indite operation and the slot ends then it has to wait again for its turn. During the mean time if the DDR3 memory reached its maximum storage the data indited at first gets effaced. In fixed priority algorithm the master with highest priority is granted access and once it gets over the master with next highest priority is granted access and the process goes on. When the DDR3 recollection storage is plenary, the information indited first gets expunged.

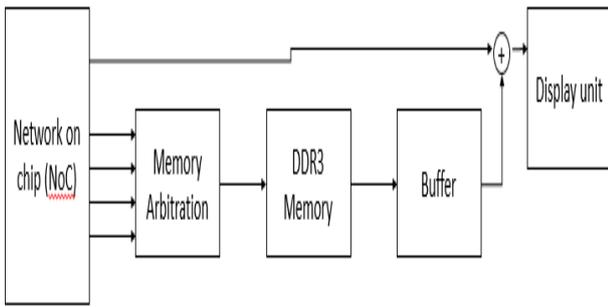


Fig. 4. Block Diagram for proposed work

Here in our model, a multimedia video or image processing signal as input from where the 'n' number of channel arises. The first channel is given directly to the exhibit unit and the remaining channels are given as an input in the memory arbitration block predicated on their priority. The arbitration plays a major role in this proposed system because it regulates the traffic and sequentially eschews deadlock. Then the regulated data will get stored in the DDR3 memory. A buffer is utilized in this process as a timer, once the time terminates the data stored and maintained in the DDR3 memory will get expunged. For example, if there is no space in DDR3 memory for the incoming new data, in such a case after the buffer limit is attained it will lead to eradication of previous data. In this paper, a single memory arbiter is proposed to connect 'n' number of channels the arbitration process takes place predicated on the priority given to the channels. Here, the number of channels used is considered as systems in antecedent discussions. Predicated on the priorities given to the channel, the arbitration process takes place as different states and gets stored in the memory controller of the arbiter block. The communication between the arbiter and DDR3 memory is maintained by the memory controller which is combined with the arbiter block. The main channel will be given in the exhibit unit and the other channel data are inscribed in the DDR3 memory simultaneously. Later, the data may be arbitrarily culled and given into the exhibit unit predicated on the priority given to the task. The high priority tasks are given to the exhibit unit and the low priority waits until the high priority task gets over. If there is an equal priority the data get transferred in FIFO or round-robin arbitration. In this paper we compare the round-robin arbitration and static fixed algorithm.

IV. RESULTS AND DISCUSSION

A. Memory Arbitration results using round robin algorithm

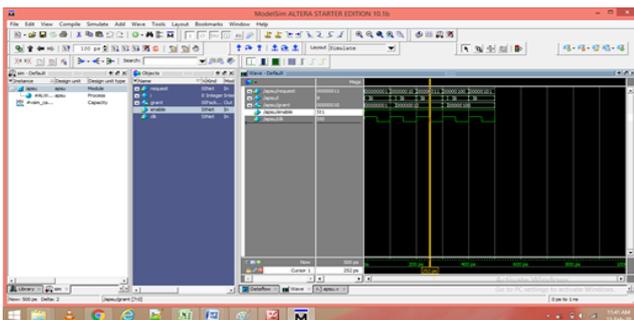


Fig. 5. Modelsim output of round robin algorithm

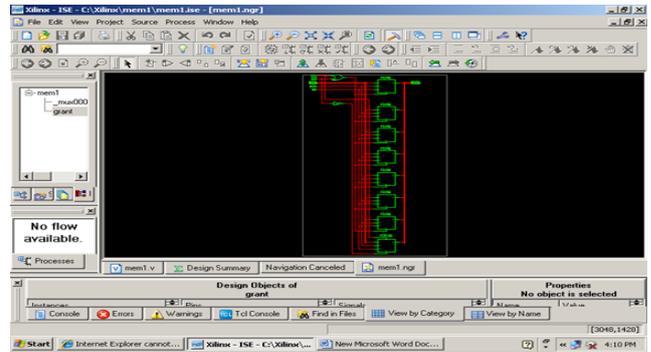


Fig. 6. RTL Synthesis for round robin algorithm

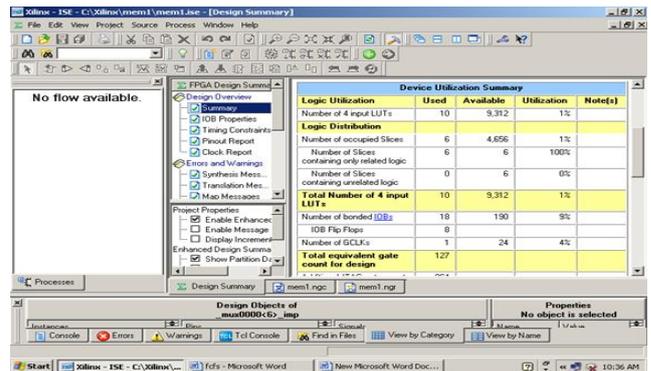


Fig. 7. Device Utilisation Summary for round robin algorithm

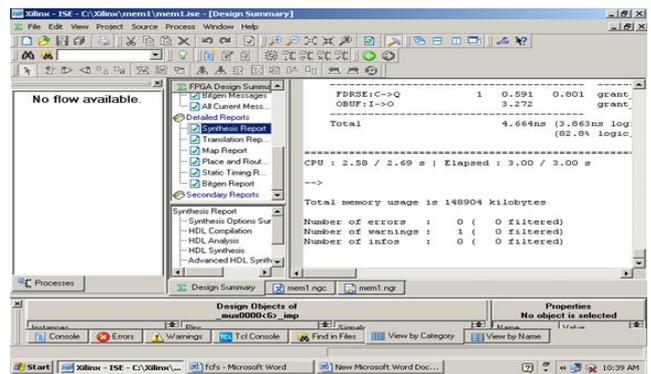


Fig. 8. Memory Usage for round robin algorithm

B. Memory Arbitration results using Static Fixed Priority algorithm

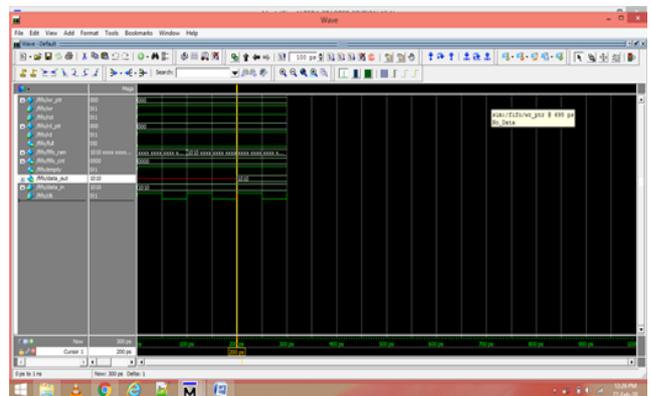


Fig. 9. Modelsim output of static fixed priority algorithm

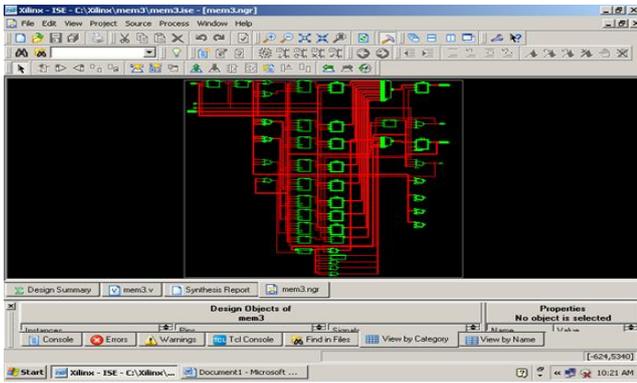


Fig. 10. RTL Synthesis for static fixed priority algorithm

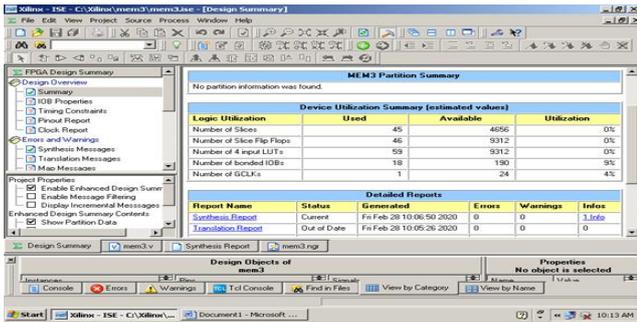


Fig. 11. Device Utilisation Summary for static fixed priority algorithm

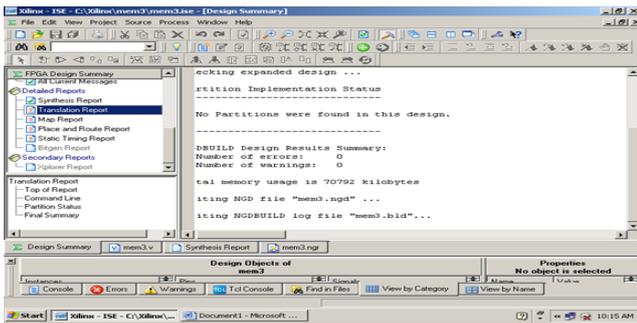


Fig. 12. Memory usage for static fixed priority algorithm

Memory arbitration using round-robin and static fixed priority algorithms are processed, analyzed and the simulation results are taken. By comparing the ModelSim waveform, RTL synthesis output of round-robin and static fixed priority algorithm we conclude that Static fixed priority algorithm has occupied less memory compared to round-robin algorithm. The quandaries in the round-robin algorithm get rectified in Static Fixed Priority algorithm. The summary results of RTL synthesis shows different parameters in which we have compared the flipflops, inputs, gates and also size of the memory. In round robin 148904 kilobytes memory get priority algorithm .So, as per our analysis better results are obtained in static fixed priority algorithm compared to round robin algorithm.

V. CONCLUSION

Incrementing the authoritative ordinance in processing leads to memory starvation, deadlock, conjunction in the network, etc.,. In this paper we proposed a design that abbreviates and rectifies the above issues by utilizing the arbitration method which evades the traffic that occurs during parallel processing. Here we compare the result like chip area, the number of slices, logic gates, size of the memory, etc, of

two different algorithms and have verified that Static fixed priority algorithm is better than Roundrobin algorithm and it gives precise results in rectifying the quandaries without consuming more memory space.

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