Design and Implementation of Reversible Vedic Multiplier with Trlic

Hridya.S, S.Bhavani, G.R Mahendra Babu, K.G Dharani

Abstract: ***The 'Vedic Mathematics' is the name given to the ancient system of mathematics with a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved with the help of arithmetic, algebra, geometry or trigonometry. In any of the fastest ALU, multiplier play an inevitable role. There is always a demand on high speed multiplier due to the raising limitation on delay. Increasing the speed of a multiplier there are number of new techniques have been implemented in which multiplier using Vedic mathematics are foremost one. The system performance and delay depend on the performance of multiplier used in it. Multiplier are used in different area such as cryptography, image processing application, embedded system application, programmable filter application etc .One of the major techniques to scale back the power dissipation is Reversible logic. There is no loss of data therefore power dissipation is reduced producing distinctive output for fixed input and vice-versa. The main objective of the project is to scale back the TRLIC of the multiplier factor by exploitation of Vedic arithmetic.The proposed methods are designed using VHDL Programming language, simulation and synthesis are done using Cadence RTL compiler in 180nm technology.***

Keywords: Urdhva Tiryakbhayam, Reversible gates, Vedic multiplier, TRLIC, Quantum cost

I. INTRODUCTION

In ancient days Aryans were performing arithmetic operation by using Vedic mathematics. [1-2]. Vedic mathematics comprises numbers of algorithm which will reduce the massive mathematical function to easy mental calculation. The above-mentioned Vedic mathematical method

is entirely different from a normal method, and it works the same way a human mind does. In most of the multiplication rules, the UT is the algorithm that decreases the calculation concerned. With the large change in VLSI area, there is always increasing demand for movable and advanced embedded systems [12]. Digital signal processing is most prominent discipline in engineering. Speedy multiplications and additions are the order of the day [13]. Multiplication is used for scaling application and it converts scaling one function by another. Addition and multiplication are basic operations for all complex functions such as FFT, DFT, convolution, MAC etc. [11]. DSP engineers are always searching for advanced algorithms and hardware technology to achieve faster clock frequency. Speedy clock frequency can only be achieved by faster arithmetic and logic units so that high speed arithmetic units are always needed. Vedic mathematics is one of the methods for accelerating multiplication. Another region where DSP technicians can concentrate more is power dissipation, the first one being speed. There is all the time a tradeoff between the dissipated power and operating speed. Reversible computing methodology will assure the zero-power dissipation compared to different computing technologies. Therefore, design of reversible circuit solely thought about the delay [14]. In this paper a reversible' UT' Multiplier has been proposed. The proposed work is arranged thus: Section II explains the basics concept of reversible logic and its parameters, Section III briefs the Vedic mathematics and UT algorithm, Section IV explains the proposed methodology, Section V analyzes the result of different methods and Section VI concludes the work.

II. REVERSIBLE GATES

Reversible logic is one of the prominent methods for zero heat dissipation in constructing computers [3]. Reversible logic is the advanced technology used to reduce heat generation due to the information loss. In reversible logic the computation process is reversible, i.e. time-invertible. An n×n reversible circuit comprises n data source and n data destination with mapping of every input pattern to a singular output pattern assignment and contrariwise [7-8]. Performance and optimization the characteristics of reversible logic are GO, QC, NG, GC, CI, TRLIC. Features and design constraints of reversible logic. [4-5]

- Reversible logic has unique number of outputs and inputs.
- Fan-out is restricted.
- Feedback paths are not allowed.
- Reduce the garbage signal.
- The quantity of constants at the input ought to be kept as low as possible.

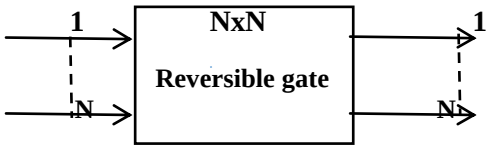

Fig: 1 Basic reversible gate

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A Parameters used for reversible gates

The following are important parameters of reversible gates [6], which can be used for designing an optimized reversible circuit.

- Constants inputs (CI): For getting the given logic function in a circuit some of the input should be kept as constant 0 and it is known as the constant input.
- Garbage output (GO): The output which is not utilized in processing a given function, but without which this output circuit cannot obtain reversibility is known as GO.
- Gate count (NG): The function can be realized using a certain number of reversible gates is known as gate count
- Quantum cost (QC): QC is the cost of the primitive gate used for realizing the function.
- Gate levels: The given function can be realized using a certain number of levels. It is known as gate level
- Total Reversible Logic Implementation Cost (TRLIC) [12]. For a given reversible circuit TRLIC can be calculated using sum of quantum cost, garbage output, constant input and gate count of that circuit [6]

III. URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM (UT ALGORITHM)

UT is the third sutra of Vedic arithmetic. Generally Vedic mathematics comprises sutras within which UT is the general equation pertinent to all or any instances of multiplication. Using UT algorithm all partial products are generated and then added parallelly, the parallelism in partial product generation and their summation is acquired. Unlike other multipliers, with a rise in the amount of bits and /or multipliers, the time limit in product computation does not increase. Due to this reason computational time is not dependent on the processor clock frequency.Thus, the clock frequency can be limited to a lesse r value. In like manner, since low-frequency processors dissipate lesser energy, it is economical in terms of power factor to use low frequency processor using fast algorithms and quick calculations, for example, those recorded previously. Compared to conventional multipliers the multiplier using UT algorithm has an advantage over their area and gate delay.

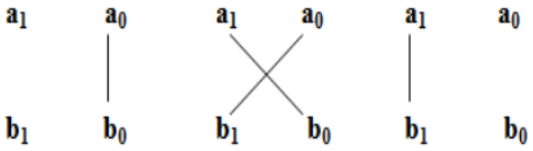
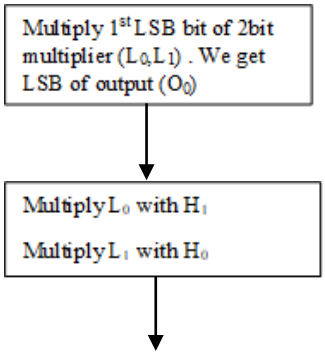


Fig:2 (a) Line diagram representation of basic 2 x 2 Multiplier using UT Algorithm



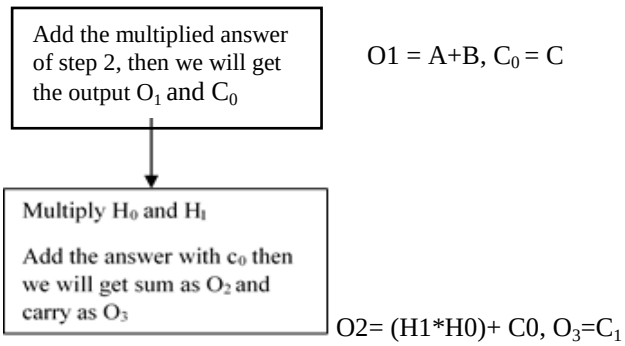


Fig: 2 (b) Flow Chart representation of UT Algorithm

IV. PROPOSED METHODOLOGY

Basic reversible gates used in design are listed below

A Feynman Gate (FG) [4]

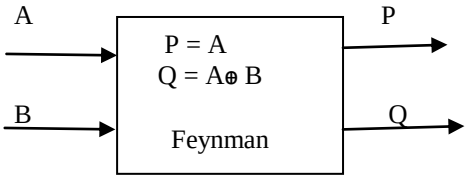


Fig.3. Feynman Gate

Figure shows the circuit diagram of 2*2 Feynman gate. It shows the reversibility by using two input and two output (A,B and P,Q) vectors. The QC for the Feynman Gate is 1 [4].

B BME Gate

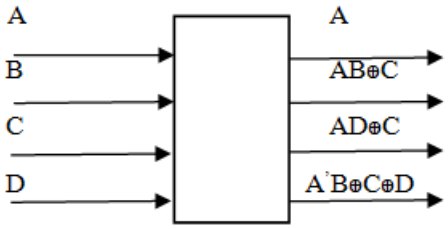


Fig.4. BME Gate

The BME Gate comprises four input and four output vectors to maintain reversibility. BME 4*4 gate shown in Fig.2. BME gate has a QC of 5. It is used to perform AND and XOR function [7].

C PERES GATE

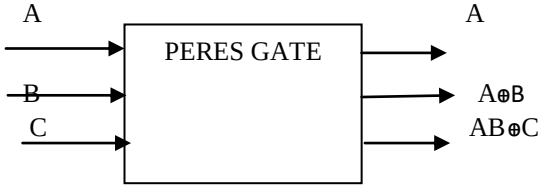


Fig.5. Peres Gate

Peres gate, consists of 3 input vectors and 3 output vectors for maintaining the reversibility.
QC of a Peres gate is 4.

It is used to perform Half adder, AND and XOR functions. [4]

D IG GATE

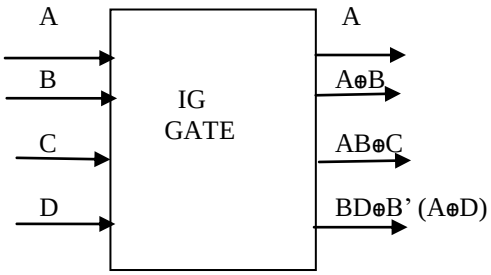


Fig.6. IG Gate

Its four output and input vectors maintain IG gate reversibility. It has a QC of seven. ISLAM gate is another name of IG gate. [10]

E Method 1

In First method circuit was designed using two BME, one IG and one CNOT reversible gate. In this design partial products are generated using BME reversible gates. The process of copying the required outputs and EX-OR operations are performed by CNOT reversible gates. IG gate is used for interconnection of BME and CNOT gates. This design requires four CI, number of gates used here is four and it generates seven GO. The quantum cost of this circuit is 18. The TRLIC value of the proposed circuit is 32, which is smaller compared to the existing circuit. Logical expression of 2x2 UT algorithm as shown below

Out0 = p0&q0
Out1 = (p1&q0) xor (p0&q1)
Out2 = (p0&p1&q0&q1) xor (p1&q1)
Out3 = p0&p1&q0&q1
(p and q are the 2 bit number used for multiplication.)

Figure 7 shows the design of 2x2 Vedic multiplier proposed method 1. Out 0 is obtained from the 2nd output of first BME gate. Out1 is obtained from 2nd output of the IG gate (out1= A xor B).Here A is the 3rd output of first BME gate and B is the 2nd output of the 2nd BME gate.Out2 is obtained from first output of the CNOT gate, it is A input of CNOT gate . A input is derived from 3rd input of IG gate. 4th output Out3 is derived from (Out3=A xor B). A is first input of CNOT gate and B is the 2nd input of the CNOT, it's from 3rd output of 2nd BME gate.

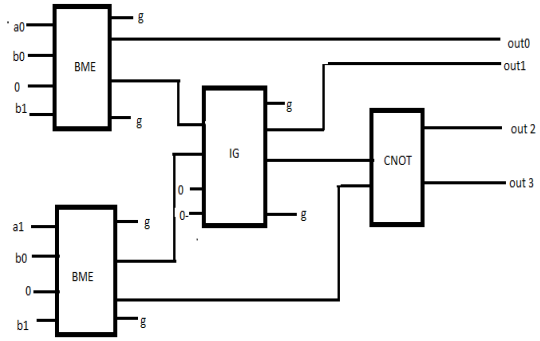


Fig.7. Design of Proposed Method I

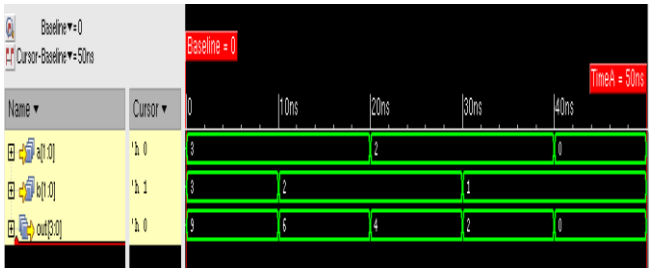


Fig.8. Simulation result of method 1

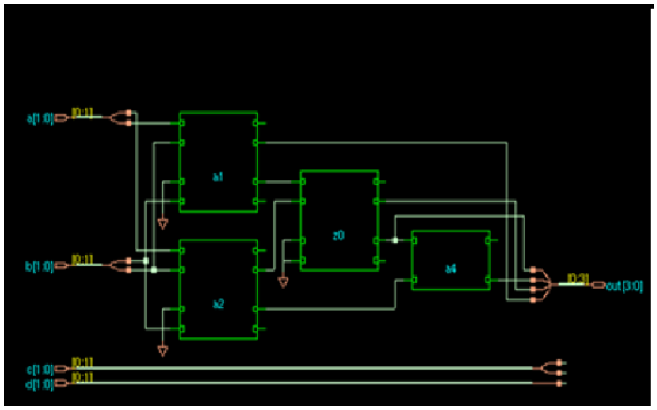


Fig.9. Synthesise result of method 1

F Method 2

In second method circuit is designed using two BME, one Peres and one CNOT reversible gate. In this design partial products are generated using BME reversible gates. The process of copying the required outputs and EX-OR operations are performed by CNOT reversible gates. Second design requires three CI, and the number of gates used here is four and it generates six GO. The quantum cost of this circuit is 15. The TRLIC value of this proposed circuit is 28, which is smaller compared to the existing circuit.

Figure 10 shows the design of the proposed method two. Out0 is obtained from the first BME second output (Out0= AB xor C). Out 1 is obtained from the 2nd output of Peres gate (Out1= A xor B) A is derived from 3rd output of first BME and B is derived from 2nd output of 2nd BME. Out2 and Out3 are obtained from 1st and 2nd output of the CNOT gate. CNOT gate input is obtained from 3rd output of peres gate and 3rd output of 2nd BME gate.

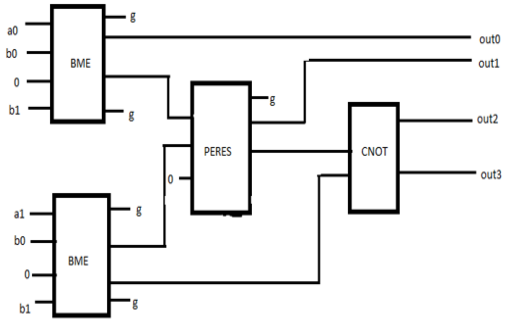


Fig.10. Design of Proposed Method 11

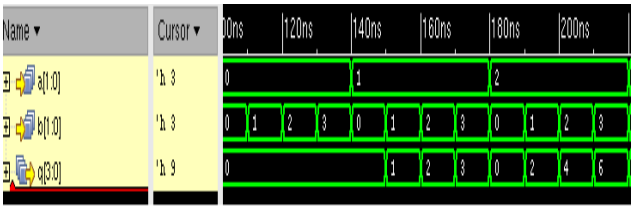


Fig.11. Simulation result of method 11

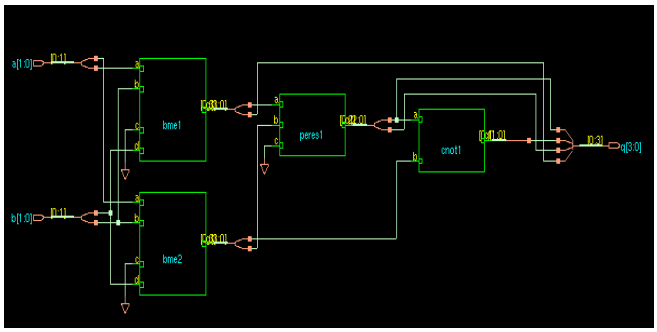


Fig.12. Synthesise result of method 11

V. RESULTS AND DISCUSSION

Tables shows the comparison results of Garbage Outputs Constant inputs (CI) Gate Counts (GC), Quantum cost (QC), area and power of various existing and proposed methods

TRLIC is calculated based on the equation (1),

$$TRLIC = \sum (NG, QC, CI, GO) \ldots . (1)$$

Existing Method 1= (QC+ GO+CI+NG) = (21+9+4+6) = 40.
Existing Method 2= (QC+ GO+CI+NG) = (17+5+5+5) = 32.
Proposed Method 1= (QC+ GO+CI+NG) = (18+6+4+4) = 32.
Proposed Method 2= (QC+ GO+CI+NG) = (15+6+3+4) = 28.

TABLE. I COMPARISON RESULT OF EXISTING AND PROPOSED TECHNIQUE WITH TRLIC PARAMETER

Types	QC	GO	CI	GC	TRLIC
EM1[9]	21	9	4	6	40
EM2[7]	17	5	5	5	32
PM1	18	6	4	4	32
PM2	15	6	3	4	28

Compile, simulate, synthesize and power estimation can done using cadence 180nm EDA tool using NC Verilog, Simvision, Encounter RTL compiler and TCF file generation (early power estimation of design done using Simvision and RTL compiler).Compare to other EDA tool Cadence generates a GDS tape out of design and easily fabricate IC chip of the design in FAB lab using this tape out.

Table. 2 Comparison Result of Existing and Proposed Technique with power and area of 2x2 multiplier

TYPES	POWER(nW)	AREA(nm^2)
EM1	537.96	28
EM2	575.81	30
PM1	575.81	30
PM2	575.81	30

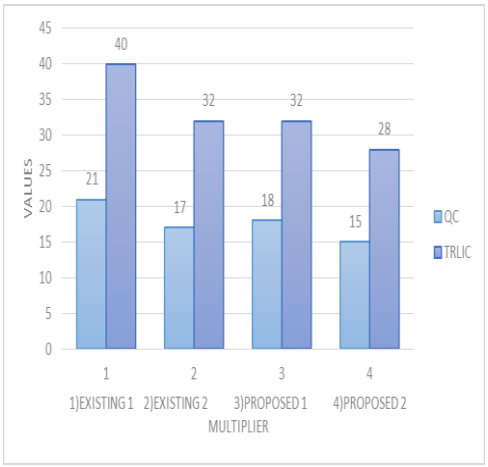


Fig.13. QC and TRLIC Comparison of Existing and Proposed Methods

VI. CONCLUSION

In this paper an optimized design of reversible 2x2 UT multiplier is proposed. Optimization of the proposed design is done in terms of GO, QC, NG and TRLIC. Design is more effective at lowering the value of design limitation. The fast, low-power reversible logic and Vedic multiplier with lower hardware complexity have been integrated and have resulted in a reduction in TRLIC of the proposed design compared to the other designs. The proposed method two has lowest number of gates, QC, GO and CI compared to existing and proposed one circuit, so this circuit has lower hardware complexity and also quantum cost of the reversible circuit is directly affect the delay of the circuit .Here TRLIC value of the second circuit is reduced due to reduction in QC so there must be reduction in delay of the proposed method two. So this Vedic multiplier can used in the application where speed has an important parameter.

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