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Design & Verification of Serial Peripheral Interface (SPI) Protocol

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Abstract: ***SPI (Serial Peripheral Interface), which was introduced by the company Motorola, and it is a protocol for communication of serial synchronous about the communication among the master and slave device, which is also used to provide communiqué between microcontroller and many devices which are additional and similar to external Analog to the Digital Converters, Digital to Analog Converters, and EEPROMs. Now a days, communication protocols are at low end. There are two different Protocols: 1) Inter-I2C and 2) SPI. Both of these protocols are well designed for the communications between the Integrated Circuits for communication with On-Board Peripherals. SPI is most commonly used protocol for both intra-chip and inter-chip, and is used at low or medium speed of data-stream transfer. This paper introduces about the quality of SPI Interface Protocol with Single Master and Single Slave configuration, which involves 8-bit of the data transfer and all necessary incorporates features that required for modern applications such as ASIC or SOC (System on Chip). The SPI design is verified and implemented by using System Verilog to show their coverage code and their functional correctness, the entire RTL was written using Verilog for Synthesis and then the Verification architecture is written using System Verilog. The implementation is done using Spartan 3E.***

Keywords:Serial Peripheral Interface, System on Chip, System Verilog, Xilinx ISE Design Suite 14.7, Spartan 3E.

I. INTRODUCTION

There are many communication protocols for both long and short distance communication purpose. Universal Serial Bus (USB), Serial Advanced Technology Attachment(SATA), Peripheral Component Interconnect- EXPRESS & ETHERNET are basically used for long distance, while Inter Integrated Circuits and SPI protocols are used for shorter distance communications. SPI has high transmission speed compared to other protocols, and it is simple to use. Standard Serial Peripheral Interface protocol requires at least 4 interfaces. The devices that are based upon SPI protocol, it is divided into two, one is master device and another one is slave device. The chip contains a select signal such as clock signal, which is provided from the master when exchange of data has been processed, it is often considered as the "little" protocol communication which is used for an On-Board communication. This paper attempts to implement design of protocol and this design methodology can be reused. We first make a study of significant commercial SPI devices (datasheets) from dissimilar sellers to look at the necessities and then include the requirements features that satisfy ASIC/SoC applications.

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II. SPI PROTOCOL

SPI has high-speed with full-duplex and synchronous communication bus, which is used for information transmission between microcontrollers and peripherals. SPI is mainly used for saving the chip ports and gap on Printed Circuit Boards(PCB) layout. It works with Master-Slave configuration, in full duplex mode there will be single master device and single slave device. It requires only four lines, and the components used are Serial Data Input, Serial Data Output, Serial Clock (SCK), and Slave Select (SS). When the master of SPI wants to send data to slave, then SS line will get low for selecting slave, the clock signal will be activated, so that both master and slave can use it at the same time. Master sends data to MOSI line (master's Serial Data Out and Slave's Serial Data Input) and itreceives the data from MISO line(master's Serial Data Input and slave's Serial Data Output). Clock pulse was provided by Serial Clock and Serial Data Input, Serial Data Output, these all are based on the pulse to make the information transmission., Data output is done through the SD Oline of master's either by rising or falling edge of the clock, and it is read by the slave in falling or rising edge followed. So, eight-bit data transfer needs at least eight times the clock signal changes.

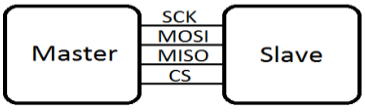


Fig 1: SPI with Single Master& Single Slave

SPI Signal Descriptions:

(A) Master In Slave Out (MISO):

Input of master and output of slave was configured as MISO line. It transfers serial data in only one direction, wherein msb is sent first. If the slave was not selected, then the MISO line will be placed in high impedance state.

Table 1 SPI Interface Signals

Pin Name	Master	Slave
SCK	Serial clock output from the master [SCK]	Input to the slave [SCK]
SDO	Serial data output from the master [MOSI]	Input to the slave [MOSI]
SDI	Serial data input from the slave [MISO]	Output from the slave [MISO]
SS	Optional slave select [SS]	Slave Select [SS]

(B) Master Out Slave In (MOSI)

Input to slave and output to master is done by MOSI line. Data is transmitted in single direction serially, with the msb.

(C) Serial Clock (SCK)

The synchronization of data to and from the device is done using the serial clock, through MOSI & MISO signals. The duration of eight clock cycles, slave and master device are capable in exchanging the data a byte. The master device generates SCK, hence, it be an input to the device of slave.

(D) Slave Select (SS Bar)

The device of slave is selected using the select input line of slave, which is active low during data transfer and must stay low throughout the data transfer.

III. SPI DATA TRANSMISSION

There are four modes of operation, they are from 0 through 3, they are used to control the data way which is clocked in or out of SPI device. SPI control register (SPCR) manages the configuration using two bits. The CPOL control bit specifies the clock polarity. Different transfer formats are selected using the clock phase CPHA control bit. Same mode has to be maintained to ensure better communication between both master devices and slave devices, which can provide the required reconfiguration of master and to match the requirements of slaves with different peripheral.

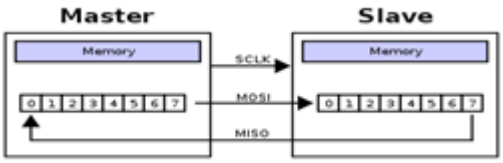
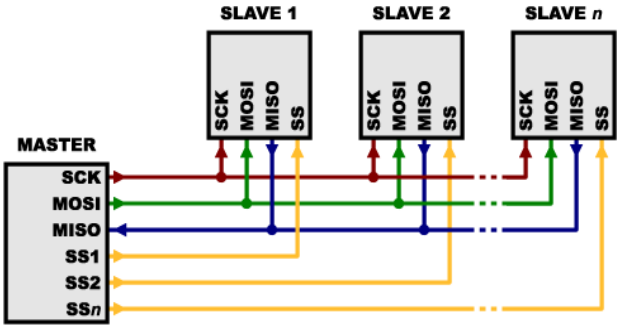


Fig 2: SPI Data Transmission of 8-bit from Master to slave

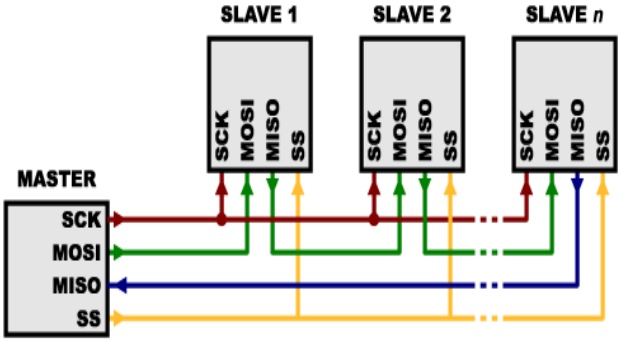
Communication is always initiated by master, and will configure the clock first using that configure frequency that which must be less than or equal to frequency which is maximum then the slave device. The master will select a desired slave for communication by pulling a chip through SS line of aslave-peripheral that is particular to low state. Shift register will organize for usage of data transfer with the given word sizes such as 8-bits in master device and slave device and they will connect in a ring. MOSI line is used by the master to shift the register value, then slave shifts the data in to shift register and then the data is sent to master by slave through the line MISO.

IV. MASTER WITH MULTIPLE SLAVES

1. Independent Slave Configuration



2. Daisy Chain Configuration



V. VERIFICATION ENVIRONMENT

Verification Environment is based upon HVL i.e. System Verilog, which is used for Verification of Constraint random with the coverage driven, Verification is principle point to define precise what need to be tested, then that is used to determine the improvement and conclusion for the verification phase. This paper verifies functionality of the design with completely possibility cases and advances the verification environment. Based on necessities of the project, the subsequent points will be taken into consideration.

- Code Reusability.
- Stimulus generation.
- Build the Verification is the Next Phase.
- Verify the DUT using the environment.

System Verilog Verification architecture:

Generator: Generates the Stimulus by Randomizing the input Values and sends it to the Driver through mailbox.
Driver: It receives the randomized Values from the generator and Converts the signals from Packet to pin level.
Monitor: Monitor receives output from the DUT and converts if from level of Pin to Packet level. It then sends it to scoreboard through Mailbox.
Scoreboard: It Receives the Packets from both generator and Monitor and Compares them.

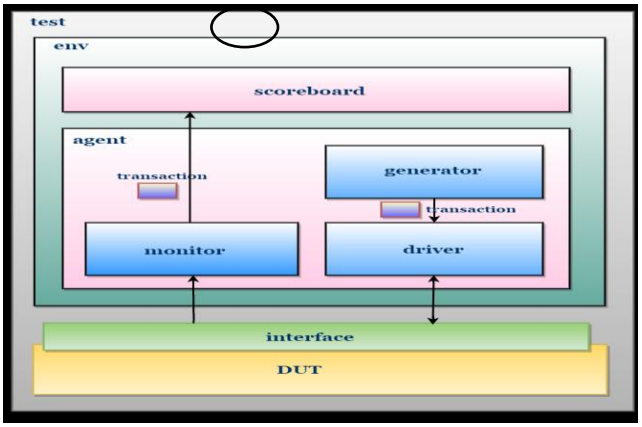


Figure 3: Verification Environment

Transaction is created by generator, which randomizes the inputs and they will mention them in to driver from mailbox. Driver generates packets and then drives them to the interface DUT. Itwill push packet into mailbox, Receiver will collect the data bytes from the signal interface. These bytes are unpacked into packet and push it into mailbox. Two mailboxes are present in the Scoreboard. One receives packets from generator while the other from monitor. They compare the packets, and an error will be asserted if there is a mismatch.

Coverage of the design has been exercised. The process of estimating functional and code consist of several steps for coverage. Firstly, they add code for the test bench and for the monitor and the stimulus will enter into the device and then it will respond and react to determine the functionality and that will be progressed then verified. After that they undergo simulation, the results of coverage are analyzed, scenarios of those test which are not been exercised are observed, and theyneed to be exercised.

VI. RESULTS

A. Simulation Results

They implement the whole design in Verilog 2005 (IEEE 1364). The Xilinx XST synthesize tool generates the RTL netlist, which is the hardware design. This was simulated in RTL as well as gate level using QuestaSim 10.4e and is mapped onto Xilinx Spartan 3E FPGA using Xilinx ISE 14.7 tool.

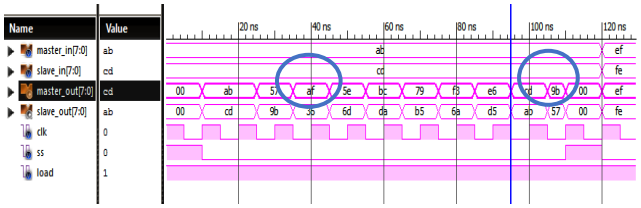


Figure 4: Waveform Of SPI – Single Master Single Slave Configuration

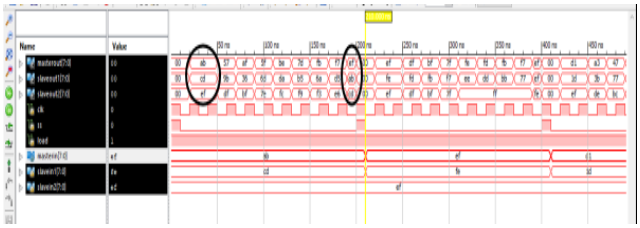


Figure 5: SPI – Daisy Chain Configuration

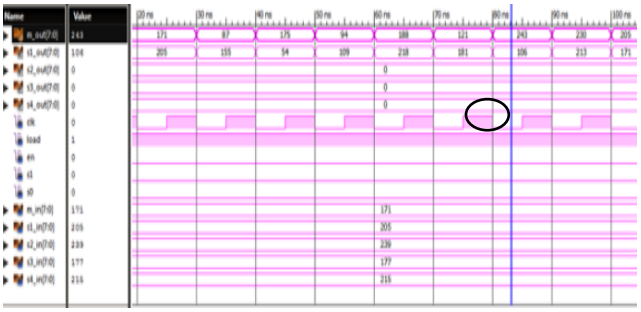


Figure 6: SPI with Multiple Slaves

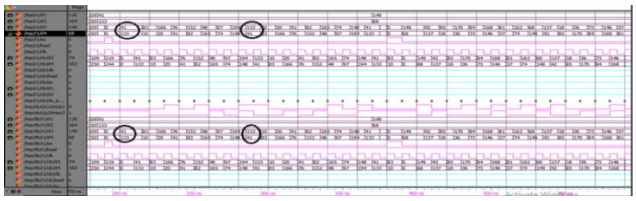


Figure 7: Verification Result of SPI Single Master Single Slave

B. Verification Results:

Coverage Report:

Using SV (System Verilog), the environment verification is verified the synthesized RTL code. There port of functional coverage is obtained using QuestaSim 10.4e. Figure8 shows the functional coverage.

The entire design of SPI using One Master &One Slave configuration will be completed and verified successfully using System Verilog along with Randomization methods which are constraint based. Code coverage and functional coverage of 100% has been observed.

Design of the SPI using One Master and multiple Slaves configuration has been successfully completed. Hence, we can show that it can operate in Full Duplex Mode.

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...
List of global attributes included in report...
List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
sv_test_sv_unit	100.00%	100.00%
coverage11	100.00%	100.00%

Coverage Summary by Type:

Total Coverage:					100.00%	100.00%
Coverage Type	Bins	Hits	Misses	Weight	% Hit	Coverage
Covergroups	2	2	0	1	100.00%	100.00%

C. Synthesis Reportdevice Utilization Summary

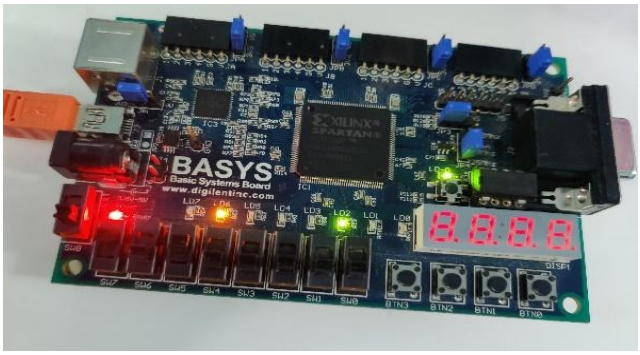
Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	17	960	1%
Number of Slice Flip Flops	19	1920	0%
Number of 4 input LUTs	32	1920	1%
Number of bonded IOBs	35	108	32%
Number of GCLKs	1	24	4%

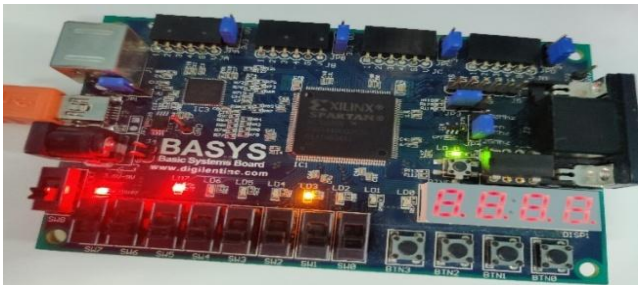
```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 3.090ns (Maximum Frequency: 323.625MHz)
   Minimum input arrival time before clock: 4.233ns
   Maximum output required time after clock: 4.394ns
   Maximum combinational path delay: No path found
```

D. Fpga Implementation

The Programming file(i.e.Bit File) which is generated by Using HDL (Hardware Description Language) Xilinx' ISE 14.7 is dumped Onto FPGA i.e. SPARTAN 3E by using Mini USB port. The frequency that the SPARTAN 3Ewith internal clock frequency 100MHZ. It has eightLight Emitting Diode (LED)outputs and eight switches.





VII. CONCLUSION

Serial Peripheral Interface with single master and single slave, single master with multiple slaves is designed and implemented by Using Xilinx14.7. The Functionality of Single master with single slave is verif ied using System Verilog.

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