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Giga-Scale Integration System-On-A-Chip Design: Challenges and Noteworthy Solutions

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Abstract: ***In all respects of the last five decades, integrated circuit technology has advanced at exponential rates in both productivity and performance. Giga-Scale Integration (GSI) System-On-A-Chip (SoC) designs have become one of the main drivers of the integrated circuit technology in recent years. The objective of this work is to understand the challenges of Giga-scale SoC integration in nanometer technologies, and identify promising conveniences for innovation. Physical designs are crucial for SoC integration and in our work we identify them with details. In future the couplings and interactions among system components will increase as we put more of the system on a silicon die. Therefore the system designers will face challenges in several areas and we describe these future challenges briefly. Developing a design driver for GSI SoC design is important. With the help of this design driver we provide the design methodology, which ensures the high performance of the design. We present two noteworthy solutions which overcome the challenges of GSI SoC design. One is reuse and integration and another is efficient bus architecture. We also provide the challenges for verification of GSI SoC and methods to overcome these challenges.***

Keywords: ***Noteworthy Solution, integrated circuits, Giga-Scale Integration, System-On-A-Chip.***

I. INTRODUCTION

Giga-scale Integration is a designation in microprocessor designs where integrated circuits (IC) contain more than one billion transistor gates [1]. System-on-Chip is the integrated system which integrates all of the system circuits on the single chip (SoC); is the most advanced form which uses powerful processors and various peripherals for running Windows and Linux [2]. The propulsion force behind the progression of integration technology is Moore's Law. Moore's Law suggests the exponential growth. The challenge is to keep up the exponential growth to acquire GSI SoC. A study by SEMATECH showed that, the number of transistors per chip increases at an approximate 58% annual compound growth rate, whereas the design productivity grows only at a 21% annual compound rate [3]. This mismatch between silicon capacity and design productivity should be solved to maintain the pace of Moore's Law. Therefore requires innovation in design of GSI SoC. There is a pressing need to explore circuit design ideas in new emerging technologies in deep-submicron in order to exploit their full potential during the early stages of their development [4]. But limited work had done in this area. An International Workshop on Challenges and Opportunities in Giga-Scale Integration for System-On-A-Chip was organized by Cong, et al. The goal of this international workshop was to understand the challenges and critical research needs of design and verification technologies for Giga-scale system-on-a-chip integration in nanometer technologies and identify promising opportunities for innovation [3]. In 1995, Meindl and Pettit describes what will be the 21st Century Giga-scale Integration and what challenges will they face [5]. The Interconnect Limits on Giga-scale Integration in the 21st Century describes by Davis, et al [6]. All of them focus only a part of the GSI SoC, mainly the challenges. Some focuses only the design and verification challenges, some focuses the interconnect limits and some focuses the future challenges. But there is no work that describes the overall challenges and how to overcome them. Because it's a new trend and, therefore, there is lacking of required resources and expertise researchers. Our work focuses on the overall challenges that might face GSI SoC designers and the resolutions by which the challenges might be overcome. Hence the objectives of this work are: A. Identify the areas of challenges related to physical design and future design. B. Provide efficient design Methodology to ensure high performance of the design. C. Present few Noteworthy Solutions of design.

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II. DESIGN CHALLENGES

2.1 Physical Design Challenges

Aggressive feature size scaling of IC over last five decades enables the design of more powerful chips. Aggressive scaling has introduced designers numerous challenges on interconnection and physical design. The interconnection is mainly depends over the physical design of the chip. That's why the physical design challenges of GSI SoC chip is given below:

Wire delay: In past, when semiconductor manufacturing technologies were in micrometer or greater than 100 nm; the wire delay was high. This was a principle concern which lessens the speed of the processor. The gate delay scale down with improvement of the semiconductor technology but the wire delay either increase or remain constant. For recent 14nm or 10nm technology, by reducing the distance travelled by a signal; the wire delay is kept in tolerable limit. However, still it's a principle concern for any chip design.

Power consumption: In micrometer or larger nanometer semiconductor technology, the distance between the transistors was higher. Therefore data transfer requires much time and the resistance between the connectors were high. So the CPU were consumes much power and the system were power inefficient. Power closure is becoming an important design concern in almost all applications, including battery-powered microelectronics where maximizing the battery service life is one primary driver, and high-end systems where excessive power dissipation limits the number of devices that can be integrated on the same chip [3].

Timing termination: Timing termination is the key challenge facing today's GSI circuits and SoC systems designers. This means we need to complete the physical design in time to meet the rapid market need. For this, we have to study and understand the fields of chips and for design, we may have developed some new technology or have to upgrade or reuse the old one.

Routability: Routability is becoming more and more important and difficult challenge since unroutable design is not useful even it finalizes all other design metrics. Because of significant mismatch between circuit capacity and design productivity, rack of routability during placement is especially meaningful for modern designs. The pace at which the number of transistor per chip increases, the design productivity does not increase at the same pace. Hence we have concern about the routability issue.

Mixed-signal design: Mixed-signal design challenges are critical in GSI SoC system design. Mixed-signal includes several types of noise signals to our original signals and we have to get rid of it to gain high performance.

2.2 Future Design Challenges

In future, the GSI SoC architecture design must face several challenging design issues, as shown below:

Reusable Architecture: The recent pace of multimedia application increases rapidly and becoming complex. For example, the audio coding standard has been resulted from MPEG-1 to DVD-Audio and the resolution of image has been increased from (320X240) pixels to (2048X1536) pixels. To meet with these pace and complexity, highly scalable architecture is required. From past few years to recent, we use IP reuse and it may keep pace with the increased complexity. But in future, IP reuse will not be appropriate and we must have to shift to the reusable architecture. This will be very challenging task to reuse architecture and increase its computational capability to keep pace with the complexity.

IP Integration: Integration doesn't mean just placing the component on the chip. It must have been done in an appropriate way so that it can perform better. In GSI SoC, where we put billions of transistors and logic gates on a single chip, the integration must be a major task. Also when we use Intellectual Property and to integrate it with the other component of the same chip, then it become a very challenging task. In IP integration, the IPs uses are different. So it will be a hard task to make it perform in a timely scheme and find out a way to test the whole system.

Network-on-Chip: SoC integrate all required component for a system. As time goes, it is becoming difficult to put more components on SoC. When we can't put more component in SoC, its computational power and efficiency will not be increased. As applications require more Computational power in the next few years, it is clear that we need multiple processors, processing elements, and function units [7]. Also the pace at which the transistors and ICs are scale down, the wire delays doesn't. These challenges rise the term Network-on-Chip (NoC). As this NoC is a new technology to come, chip designers must face several challenges to design using this technology.

Embedded Memory: The amount of memory integrated into an ASIC-type SoC design has increased from 20% in 1999 to 70% in 2005 [8].As today's and future SoC require more computational power, high-efficiency and less power consumption; more high-speed memory must be placed. For this reason, embedded memories are used. But all embedded memories don't provide the same type of efficiency and power consumption. SRAM provides high performance, while flash memory is the best solution for power consumption. Shortly, we have to select those embedded memories for GSI SoC which provides us high performance and lesser power consumption. But that's a great challenging task to perform.

III. METHODOLOGY

The GSI SoC is still developing and therefore the component required for a system is not fully clear. So we have to use a design driver by which we can define the detailed requirement of various systems. A Network Processor (NP) can be functioned as a design driver. Below Fig.1 shown sample architecture of NP.

A NP specifically targeted on networking application which is similar to CPU. In near future the routers will not keep pace with demand and therefore NP takes place. A NP must be easily programmable, have to support multiple protocol and high-bandwidth connections and have to take his own decision based on pre-program.
In Fig.1, the NP contains several cores (such as CPU, DSP, FPGA, PROM, SRAM, DRAM etc.). These cores are used to develop any GSI SoC. So if we provide a Methodology by which we can select these cores for a SoC, then we can easily perform the design.

Developing a Methodology for GSI SoC design is highly complex and can't be easily perform. From NP, (used as a design driver) we can define the design topics related to GSI SoC design. The topics that needed to understand the required component for a system and to select the appropriate one is given by below Fig.2:

Design Specification: A SoC contain the entire component required for a system including: CPU, DSP, Memory, Programmable logic, Mixed-signal circuits and so on. So in first step of the design, we must have to define the system-level design. For specification, the designers have to find efficient way and convenient environment. Several co-design systems or tools have been developed in recent years, such as Polis [8], Ptolemy [10], COSMOS [10] etc. Some of the recent designers use standard C or extended C to specify the system-level design. The C is specifically for software specification. So for hardware specification, the designers use VHDL. Together C and VHDL are used by the designers to specify overall system-level design.

Design Partitioning: GSI SoC implement all required hardware and software components. The function depends upon the software components of SoC which running in the processor. The function also depends upon the hardware components. The system-level design specification must have to translate into targeted system. So we have to translate hardware and software specification into target system architecture. This translation can be described as design partitioning. For this partition, the designers develop specific algorithms for specific system.

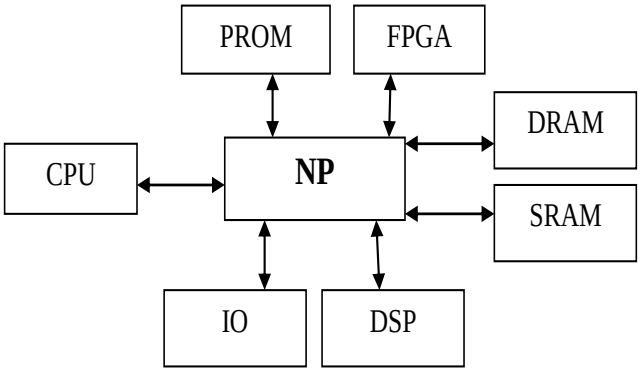

Fig.1. NP Architecture

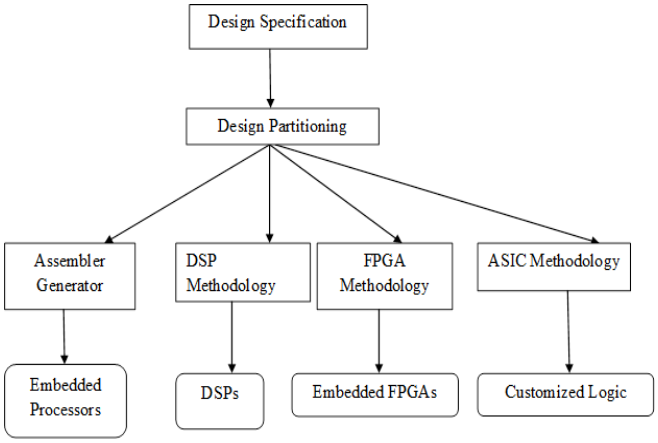

Fig.2. GSI SoC Design Methodology

Assembler Generator: Once targeted system architecture is acquired, corresponding assembler for this targeted system has to be developed and implemented. The assembler developers need to develop the assembler with lower cost and reduced time-to-market. But make complete use of all characteristics of the targeted system, so that it can provide accurate and better performance. Instead of developing a new assembler, a retargetable assembler can be used and it will both time and cost friendly. However the difficulty for this is to efficiently describe the targeted system features. In that case the NCI can be helpful with a complete and convenient compiler-developing platform. Also if we want to increase the efficiency, than efficient hash algorithm can be used.

DSP Methodology: While designing a SoC, the designers emphasize mostly on the power consumption. The main target is always to consume less power. In SoC, the power consumption is fully characterized by DSP cores. The design of the DSP cores for lower power consumption is done at the physical logical level. But it's a difficult task. One solution is, all inactive sub-circuits during machine cycles have to be turned off. Another solution is coupled controllers. While a general purpose controller decode all instructions at once, the coupled controller activated one of the sub-controller at a time.

FPGA Methodology: During the past decade, embedded FPGAs have been largely progressed. The efficient embedded FPGAs are the outcome of the FPGA Methodology. Whenever we need to done a FPGA Methodology, we must perform an incremental FPGA Methodology. Because incremental FPGA Methodology supports the design change and can perform design iteration. The design iteration is a must metric for any chip design. Because the market is rapidly changing and the complexity of the design is increasing. For both of these cases, the design iteration is the best solution.

ASIC Methodology: The systems are being complex day by day. So the design of SoC is also being complex. Therefore the traditional high-level Methodology methods are no more able to meet the complexity. Data-paths of various bit-widths square measure of needed in terribly giant scale integrated (VLSI) circuits from processors to application specific integrated circuits (ASICs) [12]. We have to shift to the interconnect-driven high-level Methodology.

Because in today's chip design, the interconnect delay is the domination factor. In silicon capacity and design productivity, there is a gap between them. To reduce the gap, we can make use of the platform, reuse or Methodology approach. In platform approach, a universal SoC platform along with few core processors and many peripheral processors has been developed. In reuse, a new SoC is developed by integrating many different IP blocks. In Methodology, the SoC is synthesized for particular application. Depend on the SoC we develop, the best one approach is selected.

IV. NOTEWORTHY SOLUTIONS AND VERIFICATION

4.1 Noteworthy Solutions

4.1.1 Reuse and Integration

In recent years, the design of GSI is being complex as the ICs are being complex. That's why the chip industry began to fastening new design and in that case the reuse methodologies arise. The Intellectual Property cores or blocks are known as reusable components and they are synthesizable. The reuse concept can be used at either platform or chip or block levels and make the IP both configurable and programmable. That's why the IP blocks can be reused in a comprehensive range of application. The reusable components include processors, memory blocks, analog and digital blocks and other parts required for a specific application. This approach solves the productivity gap problem as it provides large productivity gain. Today's notion of SoC is defined in terms of overall productivity gains through reusable design and integration of components [13].

In reuse approach, the designers don't need to implement all the components separately. They exactly need to implement all the components on a chip, in order that, they can perform complex function. This kind of design and implementation gives several facilities including reduced power consumption, smaller form factor, removes productivity gap problem, overall lower system cost, reduced volume of time to perform functions, helps to maintain the pace of Moore's Law

4.1.2 Design and Implementation of Efficient Bus Architecture

In GSI SoC, multiple systems are fabricated on a single chip. The interconnection between these multiple systems i.e. the communication between the systems is done by buses. That's why different bus architecture was developed based on different future goal [14]. As the architecture of SoC is being complex and rapidly changing, therefore the bus architecture is also being complex and changing day by day. Since the bus architecture connecting systems of SoC, so it significantly impact overall system performance. Therefore the designers need to design and implement bus architecture efficiently and quickly. Whenever we can design and implement efficient bus architecture, it provides us both flexibility and robustness. These two are the most significant functions in today's chip design.

For interconnecting processor cores, memory blocks, library macros, and custom logics, the IBM Core Connect architecture provides the following buses:

a) Processor Local Bus (PLB)
b) On-Chip Peripheral Bus (OPB)
c) Device Control Register (DCR) Bus

PLB is planned to interface directly with the processor cores. The goal is to give a standard interface between processor cores and the bus architecture. The PLB supports read and write data transfers between master and slave devices equipped with a PLB bus interface and connected through PLB signals [15]. PLB provides high performance and flexibility.

Table I. Noteworthy Solutions and Their Solved Challenges

Noteworthy Solution	Challenges Solved
Reuse and Integration	i. Reusable Architecture ii. IP Integration iii. Power Consumption iv. Timing Termination v. Network-On-Chip
Efficient Bus Architecture	vi. Wire Delay vii. Routability viii. Mixed-Signal Design

The OPB is secondary bus architecture to lessening capacitive loading on the PLB. The main features are:

a) Supports byte, half-word and word transfers
b) Provides support for 8-bit, 16-bit, 32-bit, and 64-bit slaves and for 32-bit and 64-bit masters [16]
c) Support sequential address protocol
d) Parking of bus for reduced latency
e) Synchronous

DCR controls the communication between the bus architecture and the hardware devices (for example, a peripheral or an expansion card). The DCR provides a maximum latency so huge volume of data can be transferred within the system. The two Noteworthy Solutions described in this section solve several design challenges. This is shown in Table 4.

4.2 Verification

Design complexity of SoC is increasing rapidly and time-to-market makes it even more complex. Therefore a lot of effort has to be takes place in SoC verification to overcome challenges and improving the performance of verification. Innovation is still needed, as the existing solution won't be able to handle efficiently of the increasing design size [17]. Our goal is to find the method for improving verification performance that also can solves the challenges. Verification is becoming bottleneck for complex GSI SoC design. The major challenges to GSI SoC verification can be termed as:

a) Reused IP blocks
b) Lower power design
c) Time-to-market

In today's SoC, hundreds of IP blocks from different sources are reused. The design team spends a great amount of time in lower power design since it's unavoidable. Another significant factor is time-to-market as every industry wants to have their product to be first in market.

Therefore our verification should be solves all the above challenges and provide better performance. The verification methods can be accustomed to defeat the challenges are given below with the help of Fig.3.

Plan based Metrics Driven Verification: Plan based Metrics Driven Verification helps to defeat the time-to-market challenge. Verification's purpose is to find as many bugs as possible. In traditional method, the team performs the verification only on two metrics. These are code coverage and functional coverage.

It's very difficult to gain 100% code coverage and also time consuming. Even though we can achieve code coverage, there is no guarantee that the function will be working properly i.e. the function coverage is not guaranteed. To achieve both code coverage and function coverage, traditional method requires huge amount of time. Therefore we have to move to based Metrics Driven Verification. By using this method, we find the following advantages:

a) Performs executable verification plan that saves 10% to 40% project cycle
b) Provide regression management which is 25% more efficient than traditional
c) Closure automation of verification which can achieve up to 60% time reduction

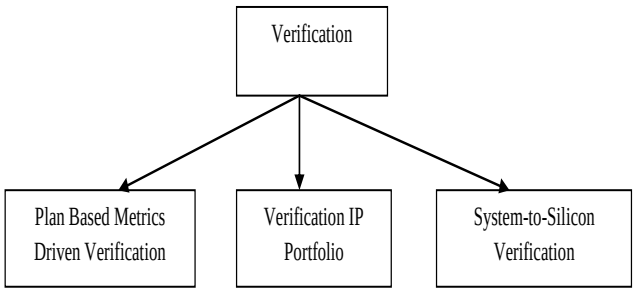

Fig.3. Verification Methods to Overcome Challenges

Verification IP portfolio: When hundreds of IP blocks are integrated in SoC, each component contain different interface and protocol. If we perform in-house development then it would be time swallowing and complex. Therefore verification IP takes place and plays a significant role for protocol compliance and interface obedience.

System-to-silicon Verification: This method focuses on lower-power solution. As SoC verification becomes complex so remove the bugs also becomes complex especially for power design. Because of lower power, the chip sizes shrinks. Therefore we have to perform System-to-Silicon verification which provides the following advantages:

a) Achieve dynamic power analysis
b) Automatically generate verification plan for lower power
c) Unique debug environment

V. RESULT AND DISCUSSION

The success of GSI SoC relies on a well concerted integrated approach from design discipline. We get the overall view of the challenges in physical design that might face Giga-scale integration system-on-a chip design. The future design challenges have also be shown as in future the couplings and interactions among system components will increase. Now to defeat these challenges with our today's technology, we need to perform Methodology. Methodology works as a bridge between the challenges and how they can overcome. Therefore we have shown the overall Methodology mechanism. We provide two Noteworthy Solutions by which we can overcome the maximum challenges that face today's GSI SoC design. We have shown the challenges in verification and how to overcome them.
The overall analysis, from basic Propulsion force to design challenges, from Methodology to verification all are served by the Fig.4.

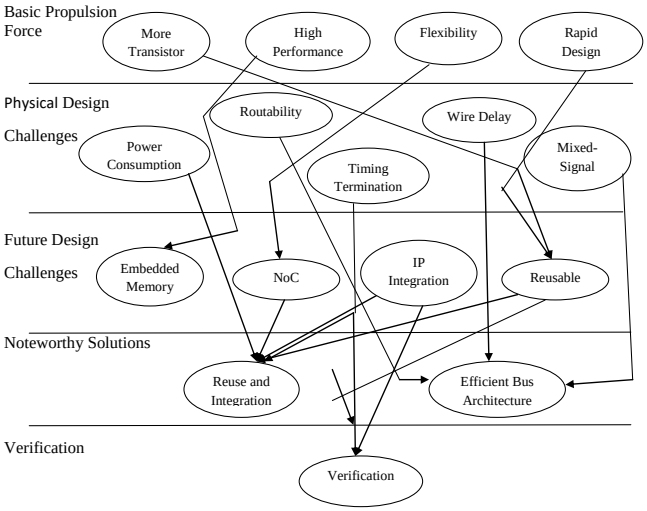

Fig.4. Overall topics related to GSI SoC design.

Fig.4 serves as an outline of our work. The links between boxes reflects the cause-effect relationship. The relationship between the cause-nodes (Power Consumption) and the effect node (Reuse and Integration) can be termed as an example.

So after analytical study of the above section and full description of the previous sections, one can easily understand what is GSI SoC? What is its challenges and lacking and what is its solution. By following the path we described in Fig.4, one can easily perform an efficient design of GSI SoC.

VI. CONCLUSION

The integrated circuit technology revolves very fast and has a deep impact in our routine life. More and more new applications are ready to dressing the IC technology revolution. According to Research and Market, “The global home appliances market was valued at USD 174.07 billion in 2017 and is projected to reach a value of USD 203.37 billion by the end of 2023, at a CAGR of 2.6% over the forecast period 2018-2023”[18]. The annual growth rate is about twice than general-purpose microprocessors. This change is because of advance in both device and design technologies, which allow us to put billion of transistors and logic gates on a single chip.

The exponential scaling of GSI SoC results in the integration of more than billions of transistors and logic gates on a chip, which provides the possibility of integration to a highly complex electronic system. To achieve this, it demands significant innovation in both design and verification technologies and to overcome the challenges.

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