

# Implementation of Dual Stage Multi-rate Filter

Latha R, Sharmila.M, P.T.Vanathi

**Abstract**— In this work, an effort is made towards the design and implementation of dual stage multi-rate digital filter architecture which is suitable for digital receivers and satellite applications with reduced VLSI cost function. The proposed dual stage decimation filter architecture consists of Higher Order Filter (HDF) as first section. To remove the droops created by the HDF section in the pass band and to get the smooth pass band frequency response characteristics, HDF filter is followed by a Corrector/Compensating Finite Impulse Response (FIR) filter network. The compensating FIR is designed using conventional Multiplier and Accumulator (MAC) unit. Initially, the filter architectures frequency response are obtained as per the given specifications using MATLAB. Then, Field Programmable Gate Array (FPGA) based performance metrics are captured and analyzed with respect to area, dynamic power dissipation, delay and power delay product. Based on the FPGA performance metrics, it is observed that the proposed dual stage filter leads to 22% of area saving and 9.5 % reduction in dynamic power dissipation. Mainly these filters are best suited for Digital Signal Processing applications in wireless receivers.

**Keywords**—Digital Receiver, Multirate Filter, Frequency Characteristics, VLSI Cost Function, FPGA.

## I. INTRODUCTION

In many applications of communication and signal processing systems, a narrowband signal of interest is extracted from a wideband signal using filter circuits of receivers. In wireless communication receivers, the multi-rate filter circuits used for this purpose become more complex due to the usage of analog components for its design. Therefore, these multi-rate filter networks are designed and implemented with its equivalent digital counterpart. This eliminates the need for expensive analog components which reduces the overall system cost. Furthermore, the overall system performances of such multi-rate digital filter designs are enhanced by the wide range of recent Digital Signal Processing (DSP) techniques. Recent trends in Very Large Scale Integrated (VLSI) fabrication technology particularly Complementary Metal Oxide Semiconductor (CMOS) techniques merged with DSP filter architectures provides a single chip based digital domain solutions for the implementation of complicated subsystems of digital receivers.

In recent years, design and implementation of low dynamic power and high speed multi-rate filters of digital receivers are becoming more popular. Multi-rate digital filters are widely used in portable equipment's like cellular phones, portable computers etc. These filter networks must be capable of receiving the signals from multiple communication standards like WCDMA, GSM, WiMAX etc. The programmable multi-rate digital filter acts as an important component in the design of digital receivers.

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In order to meet the multi-standard digital receiver requirements of low dynamic power, area and increased speed, it is essential to reduce the area and dynamic power dissipation of digital filters. In the current VLSI technologies, VLSI cost function refers to the optimization effects of area, power and delay of digital circuits.

In multi-standard digital receivers, the received analog signal is converted to an equivalent digital signal by use of oversampled Sigma Delta Analog to Digital Converters ( $\Sigma\Delta$ -ADC). Therefore, the  $\Sigma\Delta$ -ADC's of receiver must be capable of adapting to various sampling rates of the standards that are implemented. In order to extract the original information signal and for further processing in receivers, it is necessary to reduce the sampling rate from oversampled value to nyquist rate. This process of reducing the sampling rate is called as decimation process. The filter network which performs this process is called as Decimation Filter. At the same time, it is required to keep the quantization noise of digitizing process away from the desired frequency band of interest. To achieve the above said twin purpose, the decimation filters are used in digital receivers followed by  $\Sigma\Delta$ -ADC's. The decimation filter is a class of multi-rate low pass Finite Impulse Response (FIR) filter circuit and its main function is to reduce the sampling rate with minimum quantization noise. This work mainly focuses on the design of dual stage multi-rate decimation filter architecture which is suitable for multi standard digital receivers. Section 2 describes the proposed dual stage filter architecture. Section 3 concentrates on design aspects of HDF Filter section in detail. Section 4 deals with the frequency response characteristics of HDF. Section 5 focuses on design parameters of Correction FIR stage. Section 6 covers the simulation results of dual stage filter and Section 7 provides the conclusion.

## II. DUAL STAGE MULTIRATE FILTER ARCHITECTURE

In this dual stage filter architecture, a decimation filter with the decimation factor of 32 is designed using two Finite Impulse Response (FIR) filter stages. This architecture consists of first stage as Higher order Decimation Filter (HDF) and second stage as Compensating Filter (CF). CF is implemented using conventional Multiply and Accumulate (MAC) unit. The first filter stage is designed with high decimation factors and its architecture is implemented with a Cascaded Integrator Comb (CIC) filters [1]. In the digital receivers, the noise spectrum of the sigma-delta conversion can be easily removed by the CIC filters. CIC filters structure is constructed using high sampling rate integrator sections followed by the low sampling rate comb sections.

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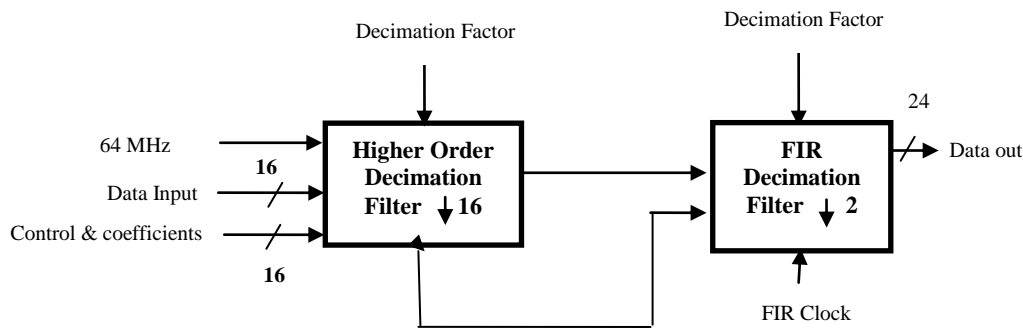


Fig.1. Architecture of Dual Stage Multi-rate Filter

CIC structure is a recursive filter network and it is designed without multipliers and presents low complexity properties. In addition, the CIC filter permits the reconfigurability features to the entire architecture. It implements a low pass filter function using only adders and delay elements instead of a large number of MAC units as that of a standard FIR filters. The fifth order CIC filter structure is considered for the design with the 5 stages of Integrator section followed by 5 stages of differentiators [2]. Thus the CIC filter structure leads to the design of low dynamic power filter circuits of digital receivers. The

integrator and the comb filter operations are performed using registers and adders only. Using CIC filters, the amount of pass-band aliasing or imaging error can be limited. In addition, the passband width and the frequency characteristics outside the passband are severely limited. To overcome these limitations of decimation filter architecture, normally CIC filters are used as a first stage to perform high sampling rate reduction and it will be followed by the corrector FIR filter which operates at lower sampling rates. The corrector FIR provides smoother frequency response of the entire dual stage filter architecture [3].

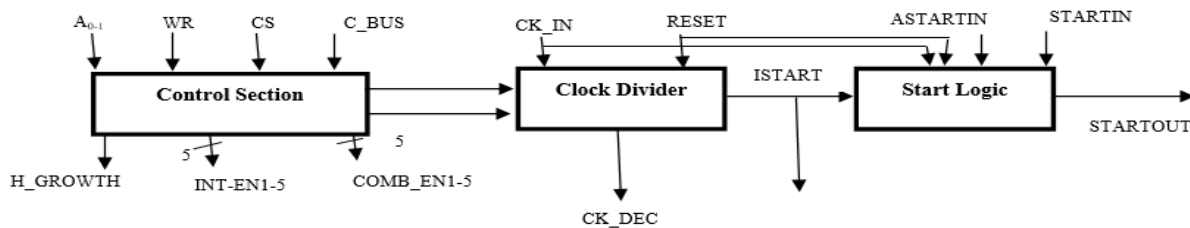


Fig.2. HDF - Control Section

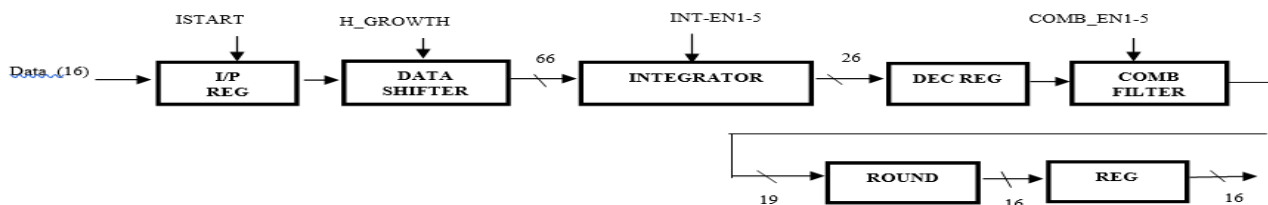


Fig.3. HDF - CIC Filter Section

The block diagram of dual stage multi-rate filter comprising of HDF and CF is shown in “Fig. 1,”. As per the block diagram, the first stage HDF utilizes an efficient sample rate reduction technique to obtain decimation up to 1024 through a course of low pass filtering process. The second stage of dual stage decimation filter, is structured as transversal FIR circuit up to 512 symmetric taps which can implement filters with sharp transition regions [4]. The FIR can perform further decimation up to 16 if required while preserving the 96dB aliasing attenuation obtained by HDF. The combined total decimation factor capability of this architecture comes to 16,384. The decimation filter accepts 16-bit parallel data in 2’s complement format at higher sampling rates [5]. Additionally, to provide configurability, the entire dual stage architecture have an option to bypass either one of the filter stages. To satisfy the need of digital receiver requirements such as minimum power, area and greater performance,

suitable decimation filter architecture is designed and it is implemented.

### III. HDF SECTION

The two sections of the HDF is named as HDF-control section and CIC filter section as shown in “Fig. 2,” and “Fig. 3,”.

#### A. HDF Control Section

HDF control section consists of four control registers. Those registers are called as HDF\_Register 1, HDF\_Register 2, FIR\_Register and FIR Coefficient Register.

The bit positions of HDF\_Registers control the internal operations of HDF stage of the dual stage decimator.

FIR\_Register control bits are used to decide the decimation factor and the order of the CF stage of the dual stage architecture. The filter coefficients of CF stage is stored in FIR Coefficient Register for computations. If Chip Select (CS) and Write (WR) control signals are enabled, the data present in the Control Bus (C\_BUS) will be loaded into the control register addressed by A<sub>0</sub> and A<sub>1</sub> bits.i.e: A<sub>0</sub> and A<sub>1</sub> are the two control signal bits used to select the control registers of HDF stage. Table I describes the selection process of the control registers in detail.

The main purpose of clock divider logic is to generate the appropriate clock signals for the effective operation of the HDF sub sections. The input clock CK\_IN of the HDF stage is divided by its decimation value and produces the output clock signal called as CK\_DEC. The decimation factor of HDF stage is stored in the Hdec bit positions of the HDF\_Register1. CK\_DEC acts as a clocking signal for the decimation register, comb filter and the output register. RESET signal clears the clock generator logic and is not enabled until the HDF is started by an internal start signal.

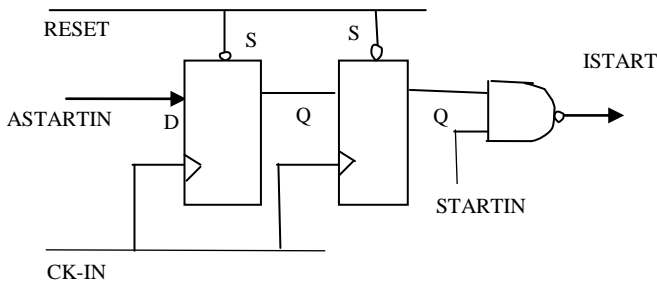
The start signal is generated by Start Logic Unit which is used to synchronize the internal operations of the dual stage decimation filter. When ASTARTIN is activated the Start Logic synchronizes it to CK\_IN by using two D latches as indicated in "Fig. 4,". The NAND gate in "Fig. 4," passes this synchronized signal to be used on chip to provide a synchronous start. When STARTIN is enabled, the NAND gate passes STARTIN which is used to provide the internal start, ISTART for the dual stage decimator.

**B. HDF-CIC Filter Section**

The CIC filter section acts as a second section of HDF stage. Main task of this section is to perform sampling rate reduction by large decimation factors. CIC section provides decimation upto 1024 due to its reconfigurability feature. After being latched into the input register,

**Table I HDF Control Register Logic**

A0	A1	Selection of Control Register
0	0	FIR_Register
0	1	FIR Coefficient Register
1	0	HDF_Register 1
1	1	HDF_Register 2



**Fig. 4. Start Logic Circuit**

the data moves into the data shifter. The data shifter is used to prevent overflow errors due to high sampling rate conversion of the HDF stage. The number of bits to be shifted is controlled by H\_GROWTH control signal of HDF\_Register 2. The transition band and the stop band of the HDF section consists of several side lobes due to its

SINC characteristics, which limits its stand alone operations in mobile networks. The basic structure of the CIC decimation filter is shown in "Fig. 5,". The integrator section of CIC filter consists of N digital integrator stages which operate at the high sampling rate, f<sub>s</sub>. The transfer function for a single integrator stage of CIC is given by "(1),".

$$H_I(z) = 1/(1-z^{-1}) \tag{1}$$

The comb section operates at the low sampling rate f<sub>s</sub>/M, where M represents the decimation factor of HDF stage. This section consists of N comb stages with a differential delay of R samples per stage. The frequency response of the filter is controlled by the differential delay parameter. In normal design, the differential delay will be set to either 1 or 2. The transfer function of a comb stage with low sampling rate is denoted by "(2),".

$$H_C(z) = (1-z^{-RM}) \tag{2}$$

where M- Decimation ratio,  
R- Differential delay  
N - Number of stages

Considering Equation (1) and Equation (2) that the overall transfer function of the CIC filter section with the input sampling rate, f<sub>s</sub> is given by "(3),".

$$H(z) = H_I^N(z) * H_C^N(z) = (1 - z^{-RM})^N / (1-z^{-1})^N = \sum_{k=0}^{R.M-1} [z^{-k}]^N \tag{3}$$

where k ranges from 0 to R.M-1

From Equation (3) it is evident that the transfer function of the CIC-HDF filter section is equivalent to a cascade of N uniform linear phase FIR filter circuits. Thus the CIC filters act as the exact replacement for the high sampling rate FIR filter where the design involves multiplier less solution and with reduced filter coefficient storage. The order N of CIC filter of HDF stage is considered as 5 and it is implemented using only integrators and differentiators (Combs). The equivalent digital circuit of the fifth order CIC filter comprises of 5 stages of accumulator section followed by 5 stages of comb sections for this design. The low power digital FIR circuit can be realized using the cascaded structure of integrators and differentiators.

The advantages of using CIC/ Sinc filters are:

- Multiplier less filter design approach and filter coefficients do not require any storage space.
- The structure is very "regular" consisting of two basic building blocks.
- In CIC structure, the operation of accumulation is done at high sampling rate and low sampling rate is used for comb sections, it leads to reduction in intermediate memory elements when compared to the design and implementation of conventional FIR filter structures.

The shifter output data enters into the integrator network and the low pass filter operation is achieved by five cascaded accumulator stages. The digital equivalent circuit of an integrator stage is implemented as an adder followed by a register in the feed forward path. The integrator sections are driven by the sampling control signal designated as CK\_IN. The output bit width of the first integrator stage is considered as 66 bits and it goes down to 26 bits at the output of the last accumulator stage.

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Bit truncation is performed at each integrator stage because the data in the integrator stages is being accumulated and growing and therefore the lower bits become insignificant and can be truncated without losing significant data. The output of the integrator section is latched onto the decimation register by CK\_DEC. The HDF decimation rate is fixed by H\_DRATE + 1, which is named as Hdec control signal [6]. The decimation register output data is fed into the comb filter section. The comb section consists of five cascaded comb filters. Each Comb filter section calculates the difference between the current and previous integrator output. Individual Comb filter stage is realized using a register unit-controlled by CK\_DEC signal followed by an subtractor where the subtractor calculates the difference between the input and output of the register. The bit width of the first comb stage is taken as 26 bits and the output of the fifth stage falls to 19 bits. In the design of dual stage decimator, the input data of the HDF filter section is limited to 16-bits wide and to provide good accuracy, the output data of the comb section is rounded to 16 bits by the rounder network stage [7].

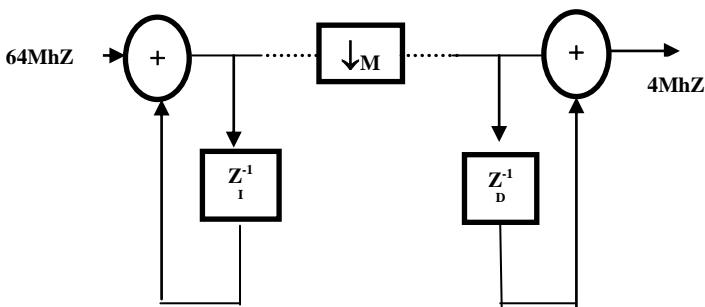
### IV. HDF FREQUENCY CHARACTERISTICS

CIC filters have a low pass frequency characteristic and its frequency response can be evaluated from “(4),”

$$Z=e^{j(2\pi f/R)} \quad (4)$$

where  $f$  is the frequency relative to the low sampling rate  $f_s/M$ . The filter design parameters  $R$ ,  $M$  and  $N$  are chosen to provide acceptable passband characteristics over the frequency range from zero to a predetermined cutoff frequency  $f_c=f_B$ , Equation “(4),” can be expanded as described by Equation “(5),”

$$|H(e^{j\omega})| = [(\sin\omega M/2) / (M \sin \omega/2)]^N \quad (5)$$



<--N Integrator Sections--> <--N Comb Sections-->  
Fig. 5. Structure of CIC Filter

Frequency response of “(5),” clearly describes a linear phase low pass FIR filter with sinc characteristics. Additionally, the sinc filter frequency response produces nulls at integer multiples of  $f_s/M$ , where  $f_s$  is the higher rate input sampling frequency [8]. Thus, the frequency bands that are aliased into the desired baseband signal by the decimation operation are centered around nulls. This provides natural alias-rejection. For CIC decimation filters, the region around every null is folded into the passband causing aliasing errors. “Fig. 6,” shows the frequency response characteristics of CIC filter with a decimation ratio of  $M = 16$ . The CIC filter has a very wide transition band and the

pass band of interest (0 to  $f_c$  in “Fig. 6,”) is typically a small portion of the resulting bandwidth after the decimation. To extract the pass band signal of Interest and to eliminate the aliasing error frequencies (due to decimation process) which lie on the wide transition band of the CIC filter, it is usually followed by a second CF decimator stage. The decimation factor of the CF stage is usually lesser than that of the CIC stage and it is designed as that of conventional FIR filter [9].

### V. COMPENSATING FIR SECTION

As per the block diagram of dual stage decimation filter, the second stage is a compensating /corrector FIR filter. This filter stage performs the final shaping on the desired signal spectrum and removes the aliasing components of the HDF section which leads to a narrow passband and sharp transition band for the dual stage decimator. The CF -FIR is designed using a Multiplier/Accumulator (MAC) unit and Random Access Memory (RAM) units as shown in “Fig. 7,” [10]. The RAM units are used to hold the data and associated filter coefficients of CF stage. The symmetrical FIR filter stage can be designed with reconfigurable implementation up to 512 symmetric taps and with decimation factor up to 16. The coefficient RAM stores the coefficients for the current FIR filter being implemented [11]. The coefficients are loaded sequentially into the coefficient RAM through the control bus and coefficients are stored from starting memory location zero. The rising edge of CK\_DEC control signal latches the 16-bit output data of the HDF output register into the data RAM . RESET signal initiates the write operation process of the data RAM.

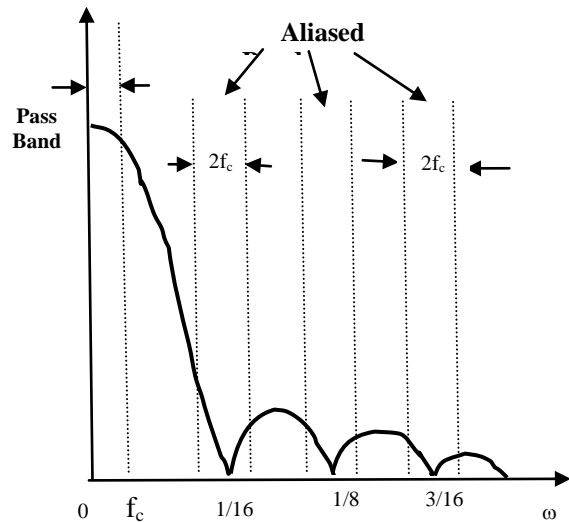


Fig. 6. CIC Frequency Response for  $M=16$

### VI. SIMULATION RESULTS

The dual stage decimation filter network is designed for GSM standard specification with the decimation factor of 32. Using MATLAB filter design toolbox, the frequency spectrum of the dual stage decimator is obtained and its filter coefficients are derived. In order to implement the entire architecture in FPGA using VHDL language, the derived filter coefficients are converted into its digital equivalent.

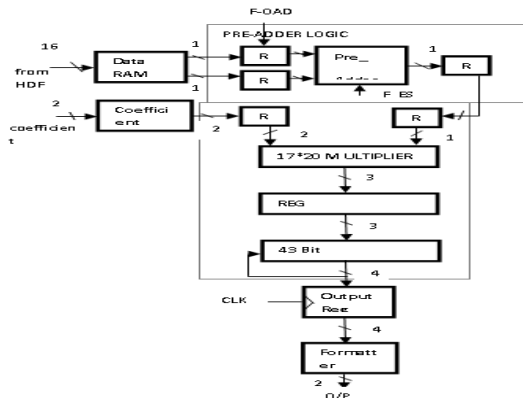


FPGA mapping reports of the dual stage decimator in terms of area, total gate count, dynamic power and its speed are analyzed. Table II describes the FPGA mapping report of dual stage decimation filter. “Fig. 8,” shows the

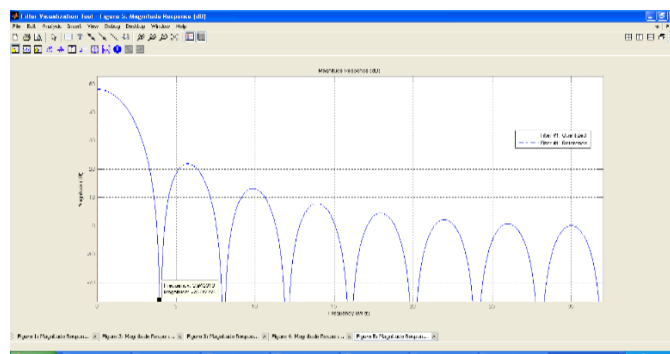
**Table II FPGA Mapping Report**

S.No.	FPGA Parameters	Mahesh et al	Proposed Dual Stage Decimator
1.	Number of Slices	1087	545
2.	Flip-flops used	648	456
3.	LUTs	2016	782
4.	Logic	956	722
5.	IOB's	128	207
6.	Total Gate Count	22581	17624
7.	Dynamic Power (mW)	1274	828
8.	Delay (ns)	33.64	27.801

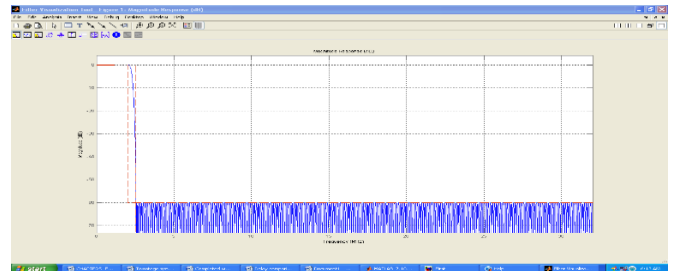
sinc characteristics of HDF section of the decimator. The HDF section of the dual stage decimator operates at 64MHz of input sampling frequency and its decimation factor is set to 16. The output frequency of HDF section is obtained as 4MHz, since its input frequency is divided by its decimation factor. The comb filter stages response of HDF section resembles to CIC (Sinc) characteristics. “Fig. 8,” shows that the aliasing components of CIC filter occurs at  $f_s/16$  and at the integer multiples of  $f_s/16$ . Hence, first null occurs at 4MHz, 8MHz, 12MHz and so on. The corrective FIR filter section response is shown in “Fig. 9,” with the decimation factor of 2 and it specifies the output frequency of the dual stage decimator falls to 2MHz.



**Fig.7. Compensating FIR Section using MAC**

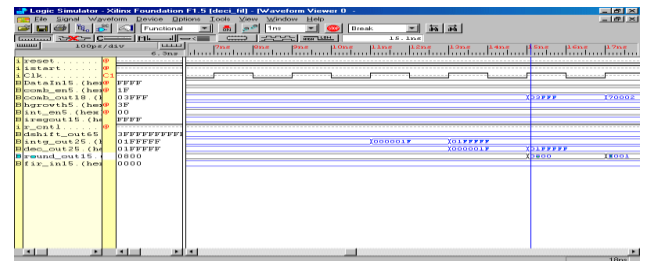


**Fig.8. Frequency Response of HDF Filter with M=16**

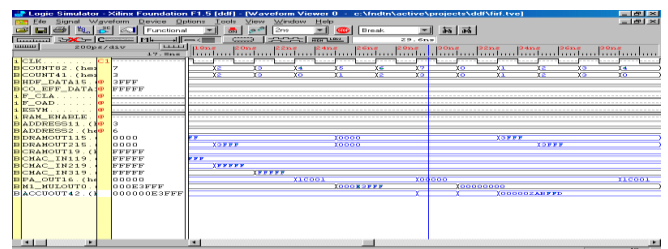


**Fig.9. Dual Stage Decimator Response, M=32**

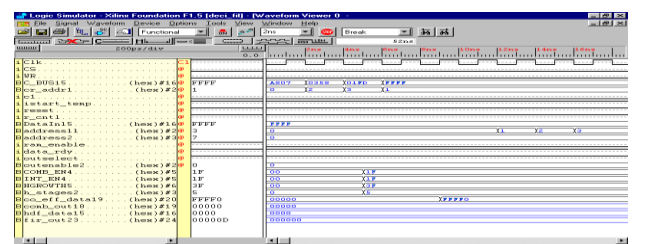
HDF filter section is implemented in VHDL by five stages of CIC structure. The input is represented by its equivalent 2's complement form and by 16-bits value. “Fig. 10,” shows the VHDL simulation result HDF filter section. After rounding process, the comb filter section output comes to 0800H. FIR Filter is implemented as even symmetry filter in and its simulation results is shown in “Fig. 11,”. Entire dual stage filter architecture simulation results are shown in “Fig. 12,”. and “Fig. 13,”. respectively.



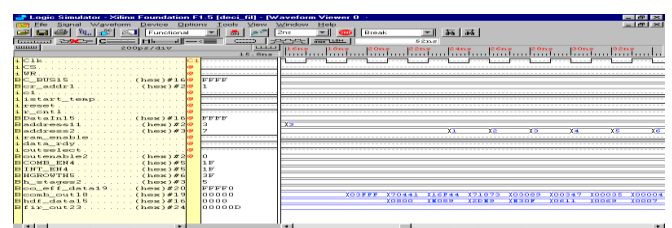
**Fig.10. Simulation Result of HDF Filter**



**Fig.11. Simulation Result of CF Stage**



**Fig.12. Simulation Result of Dual Stage Filter**



**Fig.13. Simulation Result of Dual Stage Filter**

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## VII. CONCLUSION

The dual stage decimator is designed to meet the GSM standard and its performance is tested with a decimation factor of 32. The first HDF stage is implemented in VHDL with a decimation factor of 16 and its performance is tested using Spartan FPGA. The HDL implementation of multiplier-less CIC filter leads to FIR filter realization with more sidebands and with lesser flat response in the pass band of interest. To smoothen the frequency response and to get the desired pass band cutoff, CIC filter is followed by the corrector FIR filter. The total gate count and the power consumption of the proposed dual stage decimator are measured to be 17,624 and 828mW. The time delay of the proposed dual stage filter is observed to be 27.801ns. The implementation results of proposed dual stage decimator provides 22% of area saving and 9.5 % decrease in dynamic power dissipation when compared with the existing literature survey. In addition, the speed of the proposed dual stage architecture is increased by 17.36 % with reference to existing work. Future work focuses on implementation of multi-standard multistage filters using different encoding schemes.

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## AUTHORS PROFILE



**R. Latha (Rajagopalan Latha)**, obtained her Bachelor's degree in Electronics and Communication Engineering and Master's degree in Applied Electronics from Bharathiar University, TamilNadu, India, She pursued her Doctorate in the area of Multi rate DSP and

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