An Energy Efficient Binary Magnitude Comparator for Nanotechnology Applications

Divya Tripathi, Subodh Wairya

Abstract*: Quantum-dot cellular automata (QCA) is inventive nanotechnology that suggest lesser size, lesser power consumption, with more rapid speeds and deliberated as a clarification to the scaling difficulties with CMOS technology. Physical bounds of CMOS for instance the effects of quantum and the limits of technologies like power dissipation obstruct the motion of microelectronics using consistent circuit scaling. In this paper, a 1-bit binary magnitude comparator circuit is proposed that takes down the count of QCA cells related to the previously reported design's cell numbers. The proposed course of study involves just around 29 % of the total area as compared to the preceding design with the lesser speed and clocking cycle performance and energy dissipation also. QCA designerE tool is used for simulation and finding the parameters also. The projected magnitude comparator also compares the metrics result with some of the other preceeding patterns.

Keywords: CMOS, QCA, cell, QCA designerE tool.

I. INTRODUCTION

A binary magnitude comparator is a digital circuitry that have two binary inputs and shows the similarity between them whether one input is greater than, less than or equal to the second input. A precise wide research and growth in the field device technology for the earlier numerous years prepared it probable for originators quickly and constantly decrease semiconductor device size and controlling current. QCA is a leading technology that works a nano-metric scale level to perform logic computation [1]. QCA technology, is committed on a perception that the placement of an electron promising by Coulomb repulsion, although in CMOS device, is a essential voltage for computation [2].

In MOS devices the gate tunneling current upturns with the forthcoming size going despondent to bottomless submicron device geometrical procedure. In several open fields, it is anticipated that these device technologies are coming near to its physical boundaries. Several physical phenomena that contain two discrete states used to define a logic variable in two effective logic states, for example, electron spin, etc. The contemporary effort displayed that QCA can attain high density, fast switching speediness and room temperature performances [1-3].

Magnitude Comparators are broadly applied in CPU and microcontrollers. Since a basketful studies has been designed for comparator design [1] in QCA, the proposed design takes, the more depressed field area and high calculation speed as compared to reported designs. QCA designer tool was adapted to simulation and verification of outcome in the physical forefront [6]. QCA based designs are better in parameters of velocity (high), integrity (higher) and power consumption (low) and the power of highly parallel processing. In summation, few enhancement is realized in the primitives results based on QCA design -

• We put in a compact magnitude comparator circuit which is adapted lower area. The invention has been achieved by utilizing existing comparator design.

• We synthesize the blocks in QCA designer which work along the principle of Columbia interaction.

The accomplishment of this employment such as complexity, area, latency is fairly secure and suitable for nano-electronics application [7]. This work is systematized in the following sections: Section 2 deals the necessary background related to QCA technology to read. Part 3 provides existing work related to the comparator circuit and also dispenses with an prceeding work with its professionals and cons. Part 4 details the architecture, including the QCA design and the revelation of the consequences. Part 5 provides the comparative energy dissipation results based on preceeding work and section 6 their conclusion.

II. QCA CONCEPT

QCA is well-known on the four quantum dot in which full distance settles the two electrons [12]. A polarization framework in the cell is offered in Fig.1.a. The two polarizations are revealed as P=-1, i.e., binary '0' and P=+1, i.e., binary '1'. The activity of a cell is improved due to the columbic interface between cells. The two popular architecture in QCA is known as majority gate and inverter as shown in Fig.1b, 1c.The two identical logic information is transferred to two output node is shown in Fig.1.d. Generally QCA cells are collaborated by four phase clock. The four phase clock is unknown as a switch, hold, release and relaxes as offered in Fig. 1.f [8].The simple QCA cell structural design is shown in Fig.1.g.

Revised Manuscript Received on February 10, 2020.
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At QCA, the elementary logic blocks are the not gate and the majority gate, where

$$Maj(A,B,C) = AB + BC + CA \qquad (1)$$

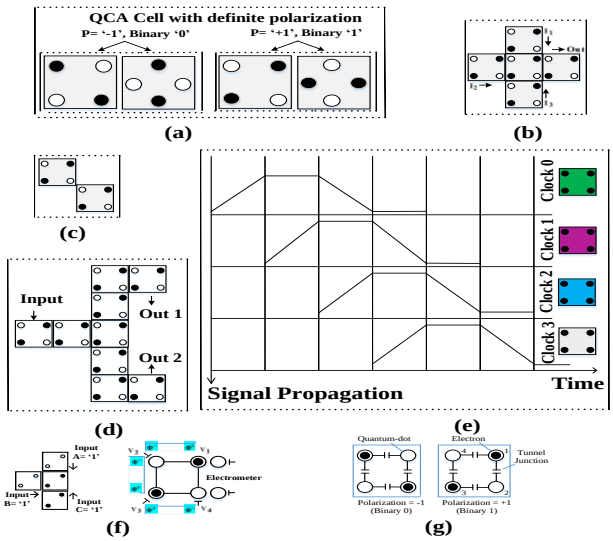

Fig.1. QCA Conception (a) Polarization (b) Majority Gate Cicuit (c) Inverter QCA Cell (d) Fan-Out (e) Clocking (f) Research of cell (g) Cell design[9]

III. EXISTING WORK

A Existing QCA Comparator

Al-Shafil et al. [11] have established a QCA magnitude comparator design without wire-crossing, which is shown in Fig. 2. In this QCA comparator design 0.182 μm^2 area and 117 QCA cells used

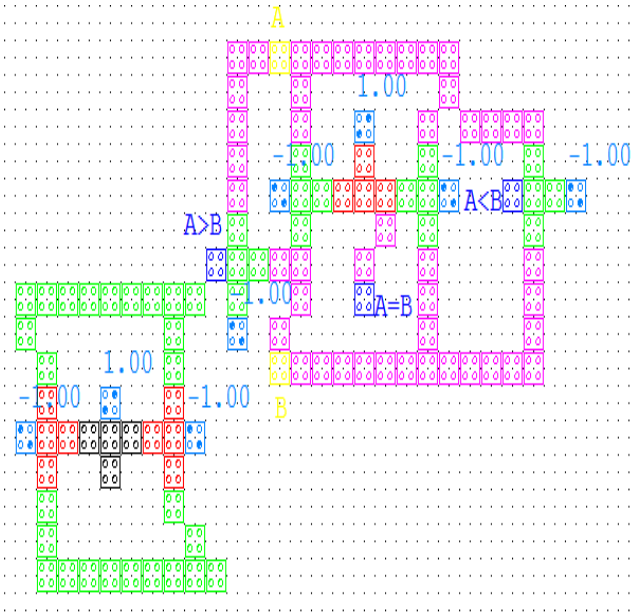

Fig. 2 QCA layout of magnitude comparator design -1

Shinha Roy et al. [12] have planned a QCA magnitude comparator circuit based on layered-T OR and AND gates, which is shown in Fig.3 (a) and (b)

This QCA multilayer comparator circuit utilized 0.039 μm^2 & 0.028 μm^2 area and 37 and 40 QCA cells respectively.

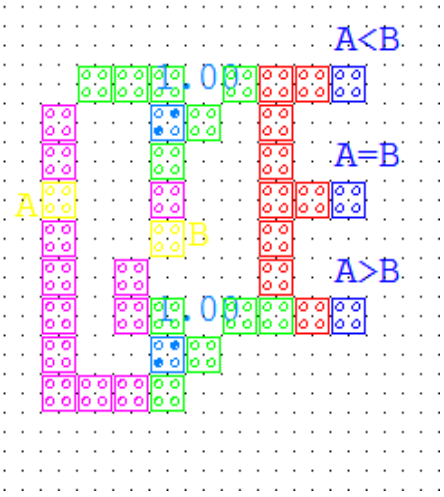

Fig. 3. QCA layout of magnitude comparator design-2

Ghosh et al.[16] have designed a QCA comparator circuit, which is publicized in Fig. 4. This QCA comparator design required 0.06 μm^2 area and 73 QCA cells.

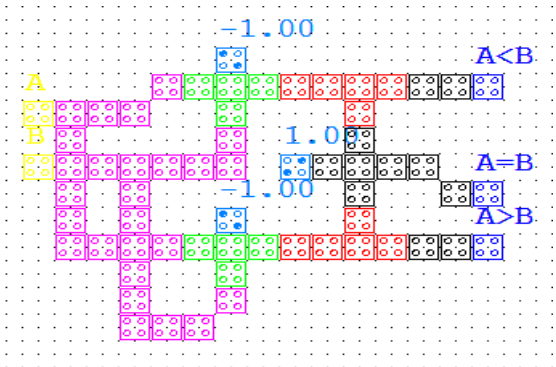

Fig. 4. QCA layout of magnitude comparator design-3

Bhoi et al.[17] have planned a QCA 1 bit magnitude comparator circuit, which is presented in Fig.5. This design utilized 220 QCA cells and 0.23 μm^2 area

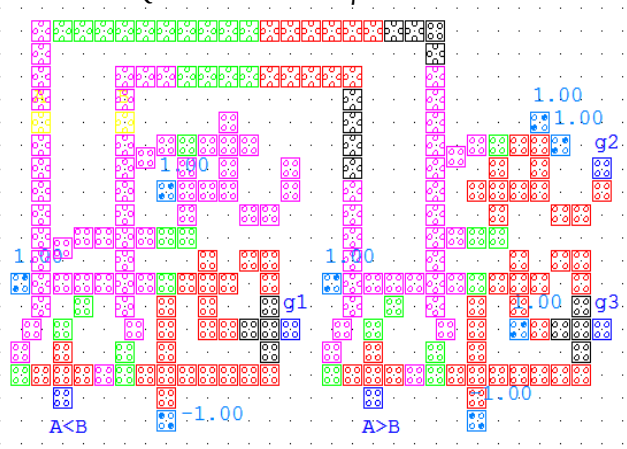

Fig. 5. QCA layout of magnitude comparator design-4

Akter et al.[18] projected a QCA comparator design by using TR and Feynman gates, which is shown in Fig. 6. This QCA comparator reuired 87 qca cells and 0.12 μm^2 area

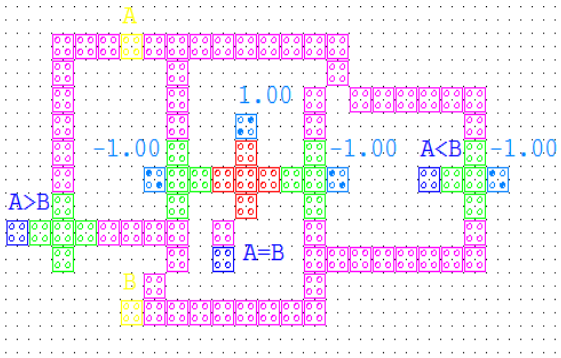

Fig. 6. QCA layout of magnitude comparator design- 5

Ahmadreza Shiri [20] suggested QCA magnitude comparator circuit based on XNOR gate having 38 cells and 0.30μm^2 shown in fig. 7.

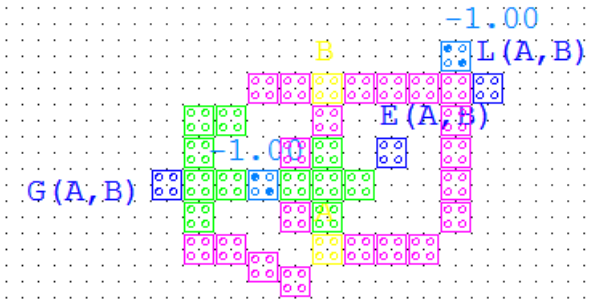

Fig. 7. QCA layout of magnitude comparator design -6

IV. PROPOSED WORK

Comparator can be designated as a combinational circuit which compares the assessment of two binary numbers and explains if one of them is identical to, bigger than, or less than another number. If the binary numbers are A and B, then the outcome is detailed by

$$A = B \longrightarrow AB + \overline{A}\,\overline{B}$$

$$A < B \longrightarrow \overline{A}B$$
$$A > B \longrightarrow A\overline{B} \qquad (2)$$

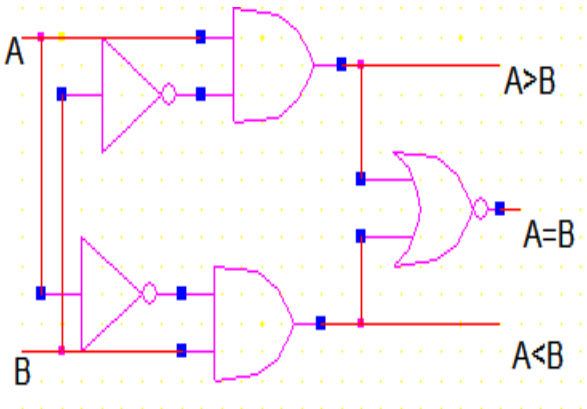

Fig.8. Schematic Of 1-Bit Magnitude Comparator

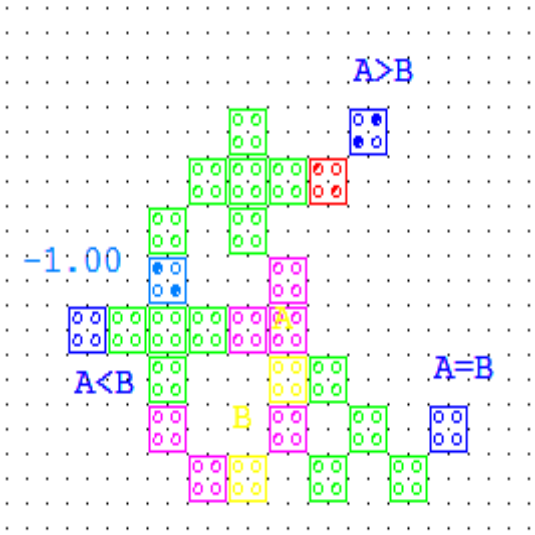

Fig.9. QCA Layout of Proposed 1 Bit Magnitude Comparator

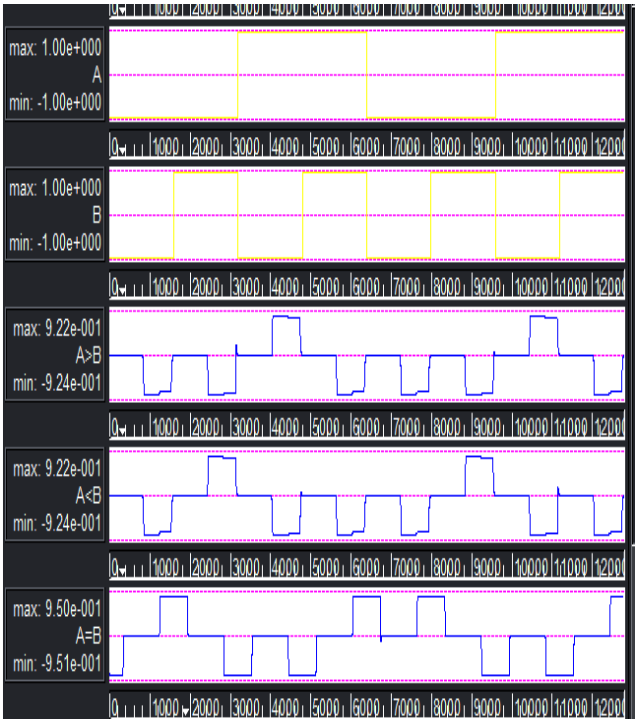

Fig. 10. Simulation Result Of Proposed 1 Bit Comparator

The proposed comparator contains 27 QCA cells and 0.04μm^2 area.

The various designs of magnitude comparator comparison shown in Table-I which indicates that the proposed design in efficient and optimum in terms of number of cells and latency as compare to the preceeding existing design.

Table I - Comparison of various QCA Magnitude Comparator

QCA Comparator	No. Of Cells	Area (in μm^2)	Latency (Clocking Cycles)
Previous 1-bit Comparator design-1 Fig.2	117	0.182	1.00
Previous 1-bit Comparator design-2 Fig.3	40	0.028	1.00
Previous 1-bit Comparator design-3 Fig.4	73	0.06	1.00
Previous 1-bit Comparator design-4 Fig.5	220	0.23	0.75
Previous 1-bit Comparator design-5 Fig.6	87	0.12	0.50
Previous 1-bit Comparator design-6 Fig.7	38	0.30	0.50
Proposed 1-bit Comparator Fig.10	27	0.04	0.25

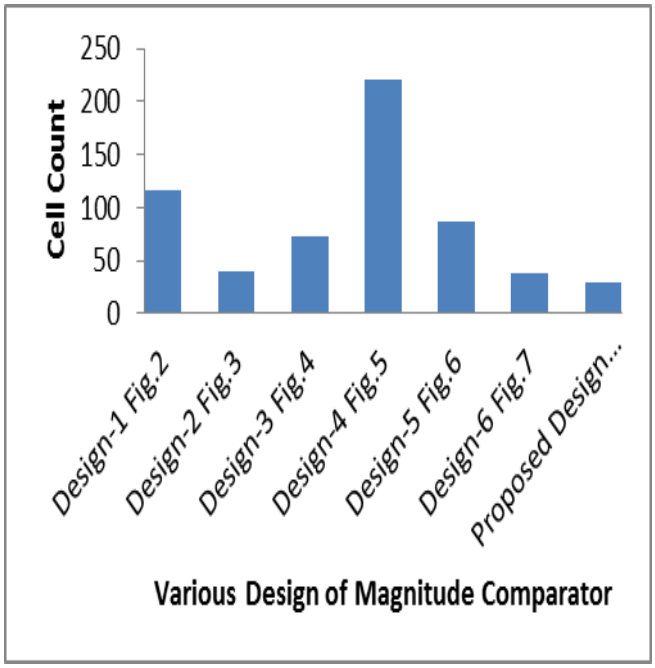

Fig.11. Comparison chart for various designs of Magnitude Comparator

During execution, each QCA cell depletes equal quantity of energy in per clock cycle. The energy dissipation by the full QCA design is estimated by the first certain power dissipation model [19].QCAE Pro is used for prediction of energy dissipation in proposed QCA comaparator design [20-21].

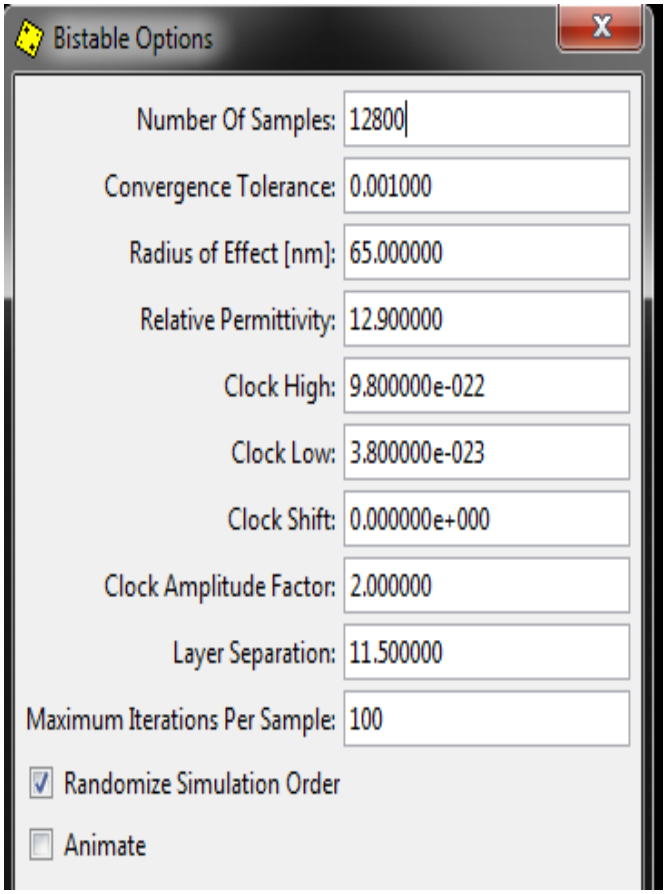

Fig. 12. Default Parameter of Bistable approximation

The QCADesigner has three specific simulation engines which implement an exhaustive verification of the system or a set of user chosen vectors here we are using Bistable simulation engine which exploits an approximation based on the contact between two cells is modeled as a simple two state system. The distance between centers of adjacent cells is of 2nm as there must be to some extent more detachment between electrons of neighboring cells. The defaulting parameters for simulation of proposed magnitude comparator is shown in Fig.-12

In table II a study of energy dissipation of the planned design is shown in the table E_bath_total is energy dissipation in each cycle, Sum_bath total energy dissipation, A_b, A_c is the average bath and average clock energy dissipation during simulation. The value of energy dissipation of each cycle is taken from the QCA Pro tool which is shown in table-II,

V. RESULTS AND COMPARISON

Table-II Energy dissipation in (Ev) by the designed magnitude comparator

E_bath_total (E_{btx})	E_clk_total (E_{ctx})	E_Error_total (E_{Etx})	Sum_bath (S_b)	Avg_bath (A_b)	Sum_clk (S_c)	Avg_clk (A_c)
1.67E-03	8.09E-04	-5.73				
2.13E-03	8.25E-04	-2.22E-04				
1.30E-03	1.58E-03	-1.31E-04				
1.82E-03	7.36E-04	-1.91E-04				
1.67E-03	8.09E-04	-1.73E-04	1.90E-02 (Er:-1.97e-003)	1.73E-04 (Er:-1.79e-004)	1.11E-02	1.01E-03
2.13E-03	8.25E-04	-2.22E-04				
1.30E-03	1.58E-03	-1.31E-04				
1.82E-03	7.36E-03	-1.91E-04				
1.67E-03	8.09E-04	-1.73E-04				
2.13E-03	8.25E-04	-2.22E-04				
1.30E-03	1.58E-03	-1.31E-04				

Table III: Comparison of dissipated energy (eV) by the proposed and existing magnitude comparator designs

Design	Sum_bath	Avg_bath	Sum_clk	Avg_clk
Previous 1-bit Comparator design-1 Fig.2	5.58e-002 (Er:-5.73e-003)	5.07e-003 (Er:--4.49e-004)	-3.02e-002	-2.74e-003
Previous 1-bit Comparator design-2 Fig.3	1.77e-002 (Er:-1.67e-003)	1.61e-003 (Er:-1.52e-004)	8.40e-003	7.64e-004
Previous 1-bit Comparator design-3 Fig.4	1.94e-002 (Er:-1.68e-003)	1.77e-003 (Er:-1.53e-004)	-7.83e-003	-7.11e-004
Previous 1-bit Comparator design-4 Fig.5	6.90e-002 (Er:-5.80e-003)	6.27e-003 (Er:-5.28e-004)	-2.71e-002	-2.47e-003
Previous 1-bit Comparator design-5 Fig.6	3.50e-002 (Er: -3.18e-003)	3.18e-003 (Er:-2.89e-004)	-1.44e-002	-1.31e-003
Previous 1-bit Comparator design-6 Fig.7	2.77e-002 (Er: -2.82-003)	2.52e-003 (Er:-2.57e-004)	-8.34e-004	-7.58e-005
Proposed 1-bit Comparator Fig.10	1.60e-002 (Er: -1.97e-003)	1.53e-003 (Er:1.97e-004)	1.11e-002	1.01e-003

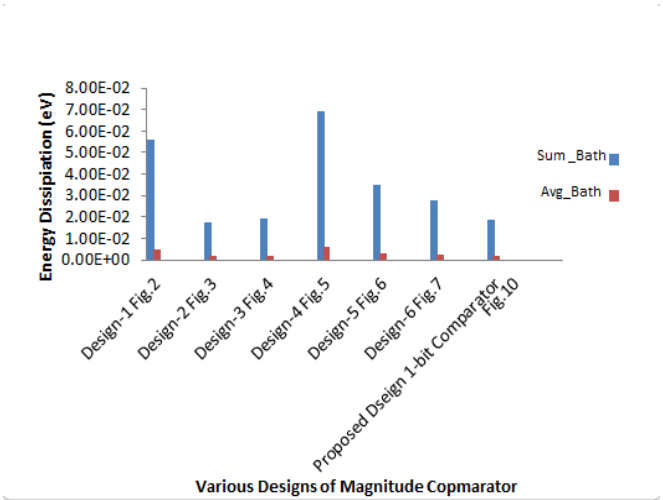

Fig.12-Comparison chart for various designs of Magnitude Comparator in terms of energy dissipation

An extension of QCADesigner 2.0.3 is QCA designer E of Konard Walus [21]. It gives an idea of the energy depletion of QCA logic circuits. It works on after simulation and shown the total and average energy dissipation which is summarized in table -2 and table- 3. In the table E_{btx} is used to complete energy transmissions to the bath of all cells distributed for each clock cycle, E_{ctx} is the total energy transfer between QCA cells and the clock separated for each clock cycle, E_{Etx} is for each clock cycle , S_b is the sum of total energy moves to the bath through the entire simulation and S_{BE} is the related error. A_b is the average standards of the energy moving to the bath and the error for every single clock cycle. S_C is the movement of energy or from the clock during entire simulation, where A_C is the average energy moving through a clocking cycle. To complete the full simulation process, 1- bit magnitude comparator took 9 iterations to converge the initial steady state polarization.

A comparison of energy dissipation between proposed and existing designs in shown in table-3. It concludes that the proposed design of 1 bit magnitude comparator has very less energy dissipation as compared to existing designs.

VI. CONCLUSION

In this work, an efficient design of 1-bit binary magnitude comparator has been planned. The proposed design is more effective as compared to preceeding designs in terms of area and clocking cycle as well as energy dissipation also. The process of the proposed designs has been confirmed using QCA DesignerE tool. The proposed designs are compared with respect of the number of cells, area, latency (clocking cycle) and energy dissipation (eV). A simulation carried out and discloses that the proposed structure of the 1-bit comparator beat the state of the art of preceding designs and demonstrated promising ability against Nano electronics technology. Here in this work both the better primitive's results and proper simulation patterns of individual blocks have been accomplished concurrently. The proposed course of study involves just around 29 % of the area as compared to the preceding figure with the lesser speed and clocking cycle performance and energy dissipation also.

This magnitude comparator design can be applied in many computing applications like ALU, microcontroller and low power devices.

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