Implementation of AMBA Based AHB2APB Bridge

Bhagvati Panchal, Yogesh Parmar, Haresh Suthar

Abstract: ***The Advance Micro controller Bus Architecture bus protocol is used to build high performance SoC designs (system on chip). This achieves communication through the connection of different functional blocks (or IP). By using multiple controllers and peripherals, it makes possible to develop multiprocessor unit. It provides reusability of IP of different buses of AMBA, which can reduce the communication gap between high performance buses and low speed buses. To perform high-speed pipelined data transfers, AMBA based embedded system becomes a demanding hypothesis analytical wise, by using different bus signals supported by AMBA. To synthesize as well as simulate the composite annexation which connects advance high performance bus and advance peripheral bus which known as AHB2APB Bridge in addition to no data loss during transfer is the main target of this work. Implementation of bridge module is designed in Verilog HDL and functional and timing simulation of bridge module are done on a platform of Xilinx.***

Keywords: ***Pipelined Data, SOC, Synthesis, Simulation, Verilog HDL, Handshaking Signal, AMBA.***

I. INTRODUCTION

The AHB bus protocol is implemented with a multiplexer interconnection technique. In this technique the communication of master and arbiter is as follows, The bus masters drives its address and control signal which indicates the transfer type i.e. whether it is a read or write transfer. Address routed to the particular slave when the arbiter selects the master which having its control signal. Main role of the central decoder is to control the data read and signal response multiplexer, which selects the relevant signals from the slaves that is required for the transfer.[8] The APB is connected to any peripherals which are low bandwidth and do not need high performance of a pipelined bus interface.

The advanced high-performance bus (AHB) :

suited for high clock frequency system for providing :

- High performance
- High Bandwidth
- Pipeline data operation
- More than one bus masters
- Burst transfers
- Only one-cycle bus master handover
- Implementation is of Non tri-state type
- (1024bits) data bus configurations.

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The advanced peripheral bus (APB):

Establish connection between peripherals which having small bandwidth.

Low power consumption

Reduce interface complexity

- Pipelined operation is not supported by APB, so it makes communication with ASB or AHB

II. DESIGN OF AMBA BASED AHB2APB BRIDGE

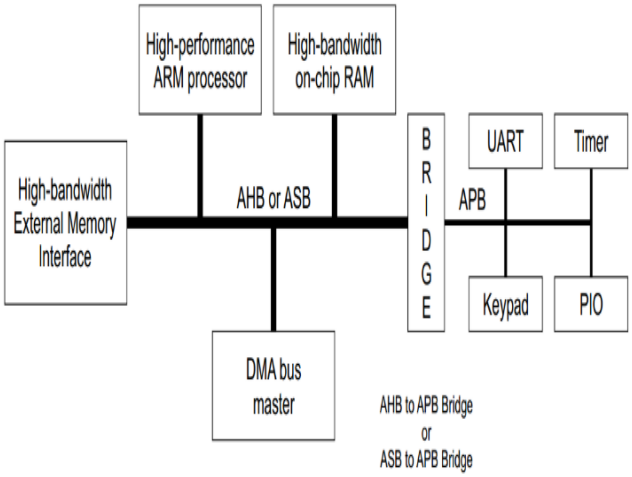

Fig.1. AMBA based AHB2APB Bridge

Here Higher performance Devices like processor, controller, DMA which has high speed and high bandwidth are connected to low speed peripheral devices like UART, Timer, Keypad, and I/O devices through bridge called AHB2APB bridge.

Main units of AHB2APB bridge:

1. AHB Master: AHB master commences write as well as read operations by come up with control and address signals. Only once the bus can be used by a single bus master.

2. AHB Arbiter: It looks for activation of only solo bus master at a time.

3. AHB decoder: It facilitates a select signal for appropriate slave by decrypt address of each transfer.

4. APB Interface: Slave answers to both operations (write, read) in the allotted span of address. Slave signal returns to master which is active and that master is acknowledge by response like success, failure and waiting of the signals(data, address) collected from the bridge.

5. AHB2APB Bridge It is leading chunk which is not a small compared to others.. To connect various elements present in top, all signals behaves as wires and connect all module within chief top chunk. This top factor having AHB slave, AHB2APB bridge element & APB interface.

A. Block Diagram of Bridge Module

AHB2APB works like AHB slave that gives bonding of elevated bandwidth, speedy AHB and small power APB. AHB pass on is converted into analogous pass on to APB. When AHB is waiting for APB transfer , wait states are put on at a moment of pass on to APB or pass on from APB because APB do not contain pipeline operation.

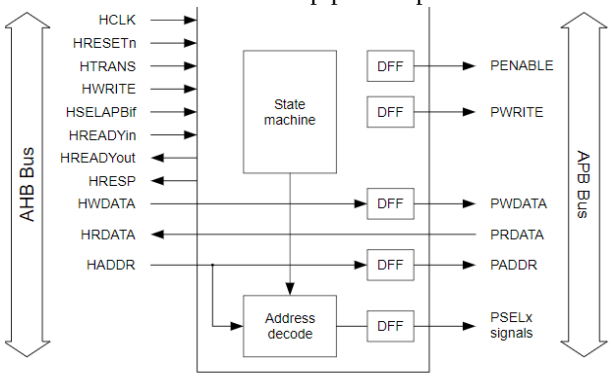

Fig. 2. Block of Bridge Module

III. DATA TRANSFER

Behaviour of the system is asynchronous type. When system going with different frequency or similar frequency and dissimilar phase , system cannot be picked out as asynchronous effortlessly. Given techniques are applied for the transfer of any data from the system or to the system.

1 Handshake signalling method

2 Asynchronous FIFO

In this work handshaking signalling method is used to conduct any data transfer. It makes use of two signals.

1. Hreadyin : It indicates that transfer is switch on .

2. Hreadyout : It indicate that transfer is completed.

IV. STATE MACHINE CAUSE AHB TO APB INTERFACE

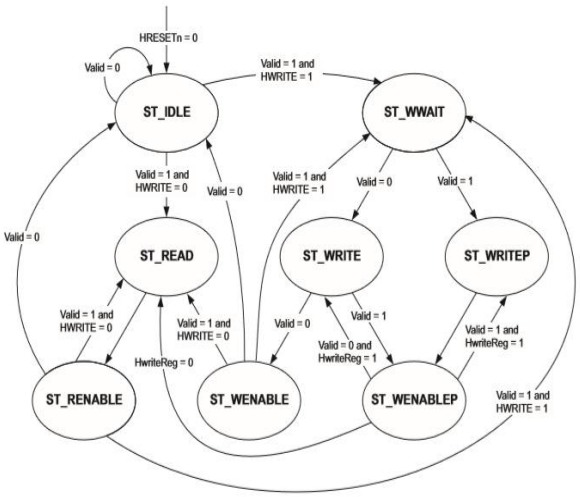

Fig. 3. FSM of AHB2APB

State machine control:

1. AHB transaction with HREADYout signal
2. Generation of each product signals of APB .

State machine is used to track separate Pslex signal according to Haddr. Then APB starts to proceeding further by authorized output.[3] In case of some not determined location there is not a single peripheral get preferred.

A. Execution Steps Of State Machine

Table I : State Transition Table of Bridge FSM

PRESENT STATE	INPUT	NEXT STATE	OUTPUT
ST_IDLE	Valid = 1 Hwrite = 0	ST_READ	AHB have valid APB Read transfer
	Valid = 1 Hwrite = 1	ST_WAIT	AHB have valid APB Write transfer
ST_READ		ST_RENABLE	Enable Current APB transfer
ST_RENABLE	Valid = 1 Hwrite = 1	ST_WAIT	AHB have valid APB write transfer
	Valid = 1 Hwrite = 0	ST_READ	AHB have valid APB Read transfer
ST_WAIT	Valid = 1	ST_WRITEP	Address decoded with presence of wait state to perform pending transfer.
	Valid = 0	ST_WRITE	Address decoded with no wait State
ST_WRITE	Valid = 0	ST_WENABLE	Enable current APB transfer.
	Valid = 1	ST_WENABLEP	Enable wait state for pending transfer.
ST_WENABLE	Valid = 1 Hwrite = 0	ST_READ	AHB have valid APB Read transfer
	Valid = 1 Hwrite = 1	ST_WAIT	AHB have valid APB Write transfer
	Valid = 0	ST_IDLE	No transfer is to perform
ST_WRITEP		ST_WENABLEP	Enable wait state

ST_WENABLEP	Valid = 0 Hwritereg = 1	ST_WRITE	Address decoded with no wait State
	Valid = 1 Hwritereg = 1	ST_WRITEP	Address decoded with presence of wait state to perform pending transfer.
	Hwritereg = 0	ST_READ	AHB have valid APB Read transfer

V. ARCHITECTURE OF AHB2APB BRIDGE

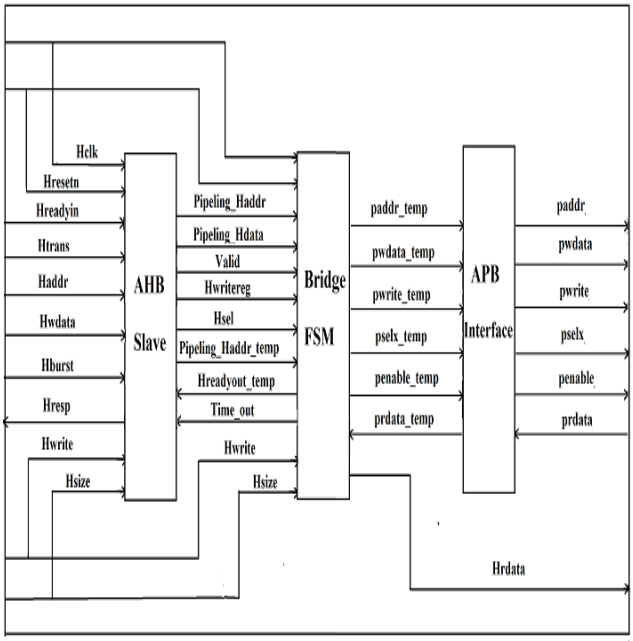

Fig 4. Architecture of AHB2APB Bridge

Architecture of AHB2ABP contains following main blocks:

AHB Slave : AHB master commences write as well as read operations by come up with control and address signals. Only once the bus can be used by a single bus master.

Bridge FSM : It is a sequential type machine that define each steps in sequence.

In this project, State machine control:

1. AHB transaction with HREADYout signal
2. Generation of each product signals of APB .

State machine is used to track separate Pslex signal according to Haddr. Then APB starts to proceeding further by authorized output.[2] In case of some not determined location there is not a single peripheral get preferred

APB Interface: Slave answers to both operations (write, read) in the allotted span of address. Slave signal returns to master which is active and that master is acknowledge by response like success, failure and waiting of the signals(data, address) collected from the bridge.

Top Module:

It is leading chunk which is not a small compared to others.. To connect various elements present in top, all signals behaves as wires and connect all module within chief top chunk.[7] This top factor having AHB slave, AHB2APB bridge element & APB interface.

A. Application of Bridge:

- Used to make affiliate and consistent system on chip associated IP.
- Allow interchangeable Soc unit.
- For rephrasing different IP.
- Permitting SoC design with multiple CPU
- Allow high speed, high performance together with low-power transmission.

B. Qualities covered by AHB2APB Bridge:

- Connection establishment in between Advance high performance bus and Advance peripheral bus hooks information signals (Address, data, Control) for low power peripheral.
- Also synchronization is necessary in between user(client) and attendant (AHB and APB) for optimal performance.

VI. RTL SCHEMATIC OF TOP MODULE

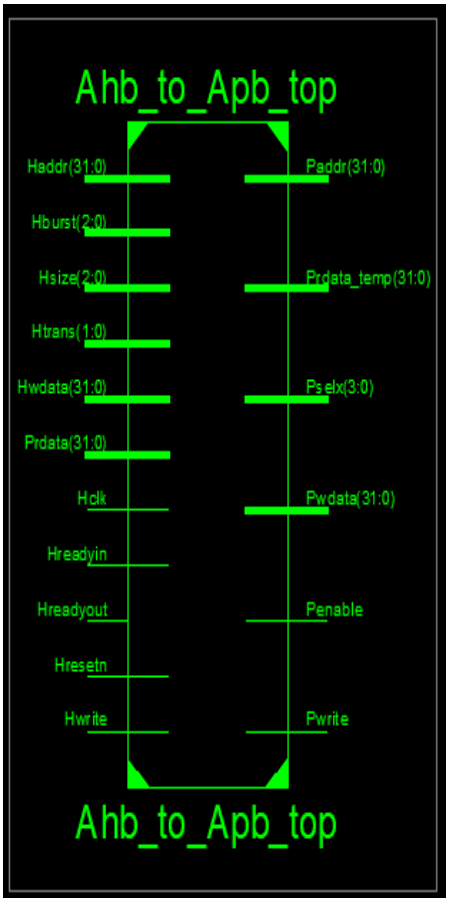

Fig. 5. RTL Schematic of TOP Module

VII. SIMULATION RESULT

A. Read Transfer To AHB

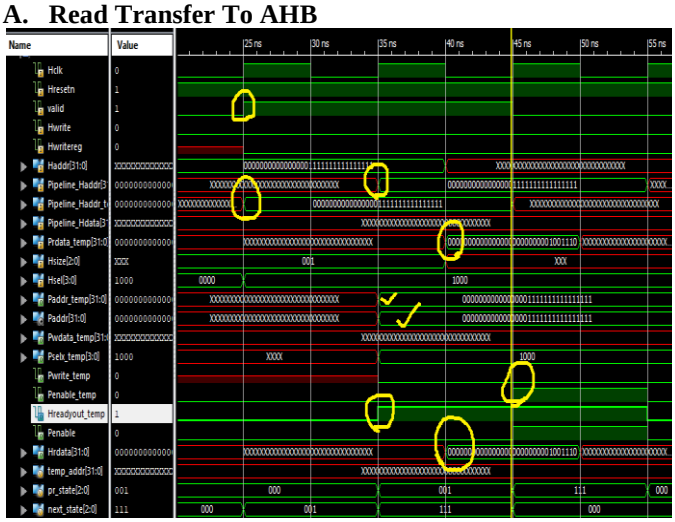

Fig. 6. Read transfer to AHB

B. Write Transfer From AHB

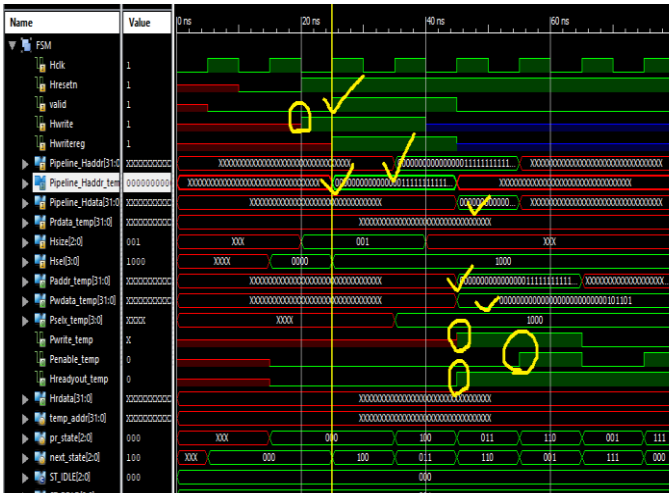

Fig. 7. Write transfer from AHB

C. Burst Read Transfer To AHB

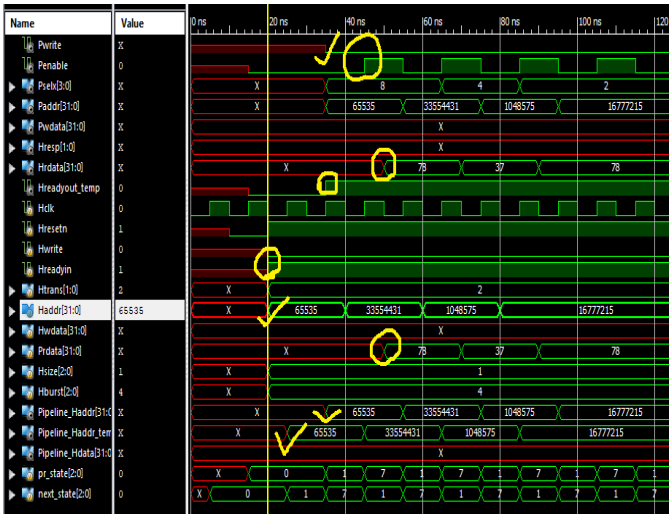

Fig. 8. Burst read transfer to AHB

D. Back To Back Write And Read

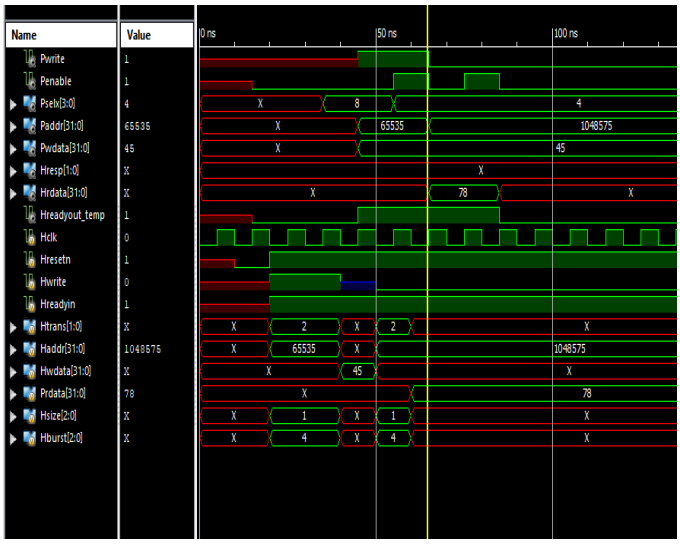

Fig. 9. Back to back write and read transfer

VIII. REVOLUTION

When data transfer is done successfully by bridge, it can be said that bridge is working efficiently. But in case of failure data loss will happen. To overcome this problem of data loss timer concept is added in this work.

When the data transfer is zero or when we not give any data, then timer becomes ON and it remains ON up to 8 Sec. After 8 Sec timeout becomes 1. So, any one can come to know that not a single data is driven by the bridge.

A. Advantage of Revolution

1. Prevent data loss during transfer.
2. Improve reusability.
3. Generic design.

B. Simulation Result of Burst Read Transfer To AHB With Timeout Condition

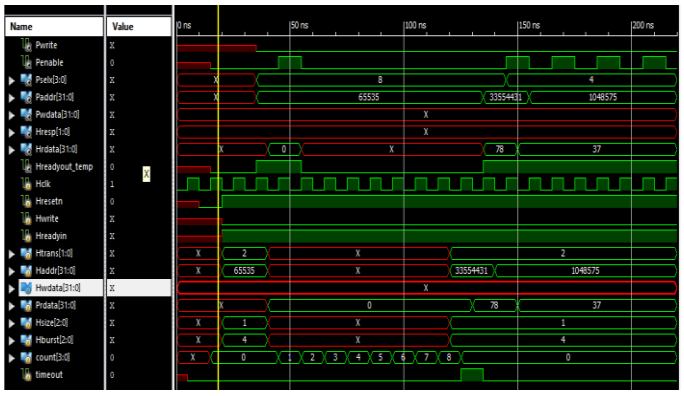

Fig 10. Burst read transfer to AHB with timeout condition

IX. CONCLUSION & FUTURE WORK

AHB2APB bridge design is implemented in Verilog HDL for Read transfer, Write transfer, Read burst transfer, Write burst transfer, back to back read and write transfer and all these design are verified by simulate Xilinx ISE. By adding timeout concept, data loss can be overcome and design will become more generic.

Importance of protocol AHB2APB is to achieve maximum code coverage and functional coverage for making design more efficient. Verification methodologies of system Verilog provides the complete coverages of RTL design. In future, using system verilog or UVM, verification of AHB2APB bridge can be done. AHB2APB bridge can be implemented in real time system for the ASIC implementation and SOC Applications.

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