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Design of Static CMOS 16 Bit High Speeds and Low Power Consumption Hybrid Adder Circuit using Brent Kung Adder

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Abstract: ***This paper presents a static sixteen Bit CMOS Brent kung adder shape was designed, which famous a higher pace and decrease strength intake in comparison with those of the ripple deliver adders. The pace enhancement changed into done through modifying the shape through thru adding a Brent Kung adder, complete adders the usage of (28 transistor, Boolean exact judgment) that is masses speeder whilst in comparison to ripple supply adder and These pace adders will bring about growth in DSP processors. The time delays and power consumptions are lots much less with unique adders with the aid of implementation of 180nm Cadence device.***

Keywords : Brent Kung adder, full adders, CADENCE, Time delay, Power Consumptions

I. INTRODUCTION

The adders are building blocks and also critical path for of microprocessors and digital signal processing chips. Adders are useful not only for addition, but also used for subtraction, multiplication and division in design criteria. In the fundamental arithmetic operations an addition is one of the funadamental. Rapid and correct operation of a digital system is strongly influenced by the performance of resident delay employees. The most important for measuring the standard of summing method in the past were delay and propagation area. There are many model of additives with different delays, energy consumption and uses of the area. Examples include the ripple carry adder (RCA), the carry increment adder (CIA), the carry jump adder (CSKA), the carry selection adder (CSA) and employees of the parallel prefix (PPA). RCA has the best structure with the less space and energy consumption, but with the least life delay. In the CSA, the speed, energy consumption and uses of the space are considerably more important than those of the RCA. The dependence of capacitance and performance on the supply voltage served as a motivation for the style of circuits with the characteristic of dynamic scaling of voltage and frequency. In these circuits, to reduce energy consumption, the system can adjust the voltage and frequency of the circuit based on the required workload. In order to achieving higher speeds with lower supply voltages for computer blocks, with the addition as one of the most important components, can be crucial when designing high-speed processors.

A. Half adder:

The half adder circuit has two inputs one output. The half-adder is added to the one-bit binary numbers (AB). The output is the sum of 2 bits (S) and the carry (C). Note in Fig. 1, but equal square measurement of 2 inputs directed to two different gates. The half-adder input and output is shown in truth table 1.

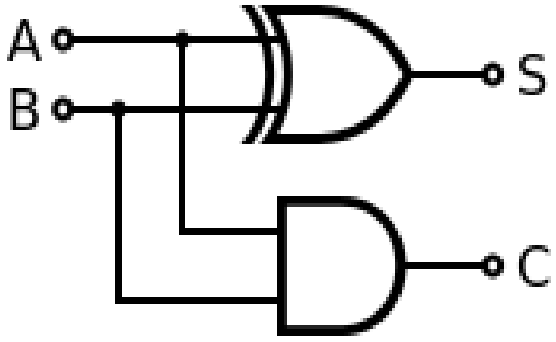

Fig 1: The Half adder Schematic

Table-1: Truth table of half adder (1Bit)

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

B. Full adder:

The full adder adds 3bit binary numbers and takes into account the values that are always output. The single bit full adder adds 3 single bit numbers, usually written as A, B and C_{in} ; The operands A and B, and as indicated in Finn Two, Cin can be slightly transferred to the previous step, more modestly. The entire adder is part of a cascade of adders that sometimes add binary bits of eight, 16.32, etc. The circuit gives a two-bit output, an output hold and a quantity.

The sum and carry equations are

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S = A EXOR B; ---------- (1)

C_{out} = A AND B; ---------- (2)

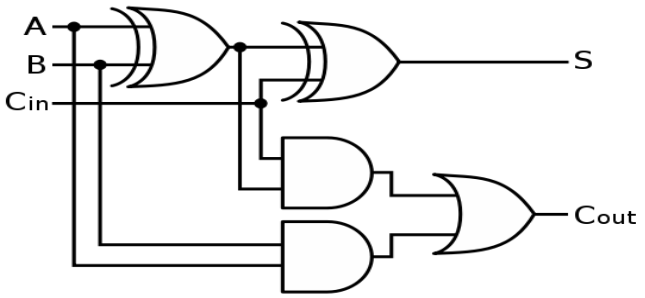

Fig. 2: The Block diagram of a full adder.

Table-2: Truth table of Full adder (1Bit)

X	Y	C_{in}	C_{out}	Sum
0	0	0	low	low
0	0	1	low	high
0	1	0	low	high
0	1	1	high	low
1	0	0	low	high
1	0	1	high	low
1	1	0	high	low
1	1	1	high	high

C. Ripple Carry adder:

Arithmetic operation such as adding, subtraction, multiplication, division, Full adder cannot add two binary digits to one bit. This has the potential to create an adder for logical use of circuits to contain the binary type with N bits. Each full adder takes the inputs, which means the outputs of the previous adder. This type of adder ripple is a carrier adder, reason as each carrier bit "Ripples" after full adder. The primary complete adder can also replaced by the complete adder.

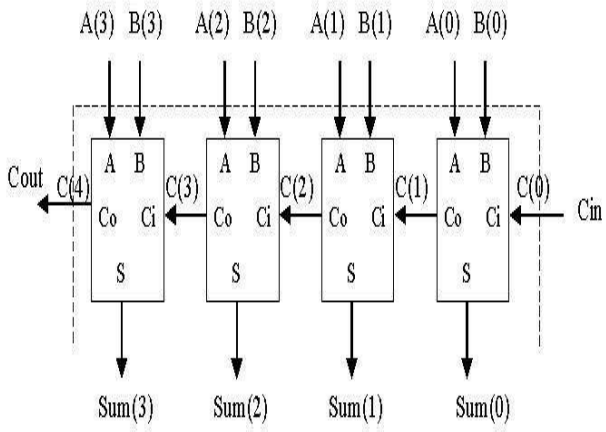

Fig.3: The block diagram of Ripple carry adder (4 bit)

D. Carry Select adder:

A Carry Select Adder is a way to implement an adder, which is a logic element that computes the (n+1) bit sum of two n-bit numbers. The simple, faster carry-select adder has usually having of 2 ripple carry adders and an electronic device. An addition of two n-bit numbers with a carry-select adder is happens with two adders (therefore two ripple carry adders) in order to form the calculation twice, one time with the assumption of the carry being with zero and the other as adding on after the 2 results area unit calculated, the proper total, also because of the correct carry, is then hand-picked with the electronic device once the proper carry is understood.

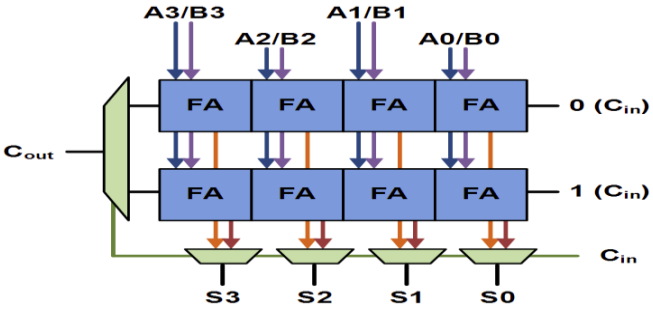

Fig 4: Block diagram of Carry select adder.

E. Carry Look ahead adder:

Carry Look ahead adder (CLA) can be a form of victimization of the adder in digital logic. A carry Look ahead adder increases speed by decreasing the time required to view the carry bits. At this time the simplest but generally lowest add a raid in which the transport bits are counted on the long side of the shipment and each bit must wait for the transport of the safety belt. Bring forward the adder counts one or more gates a little before the total, reducing waiting times and times, for the latest news on all language venues. The Brent-Kung viper stone from Kogge and adder is an example of the type of viper.

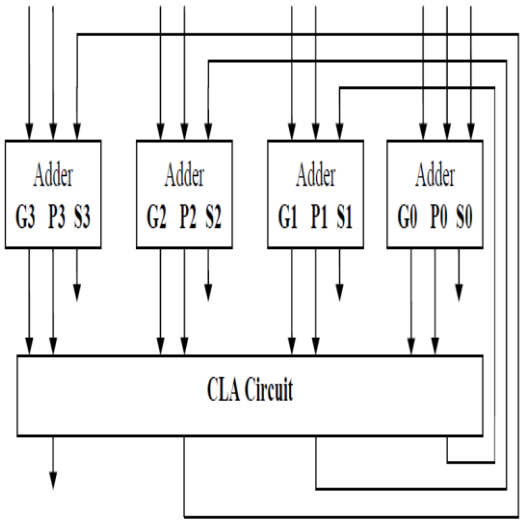

Fig 5: A Carry look ahead adder.

A. Carry Skip adder:

The carry skip adder (also known as transfer pass adder) is an implementation of adder that improves the delay of an adder carry adder with very little effort compared to the different adder Worst case delay improvement is achieved by victimizing many transport skip adders to make a block jump skip, When the propagation condition is true for each pair of digits, a simple wave ripple level. So the slip ripples through the bit adder and appears to be the slip.

For each pair of operand input bits (ai, bi), the propagation conditions pi = ai ⊕bi are determined using an XOR gate. When all of the propagation conditions are met, the slip bit determines the slip bit. This greatly reduces the latency of the adder across its critical path, since the transport bit for each block can now "jump" over the blocks with a group propagation signal defined in logic 1 as a transport chain. Extended ripple, critically, which would require transport to un delete each bit in the adder. The number of inputs of the AND gate is equal to the width of the adder. For large amplitude, this becomes impossible and leads to more delays, after which the logical gate must be designed as a tree. A good width is reached, when the sum logic has the same depth as the input AND the gate n and the multiplexer.

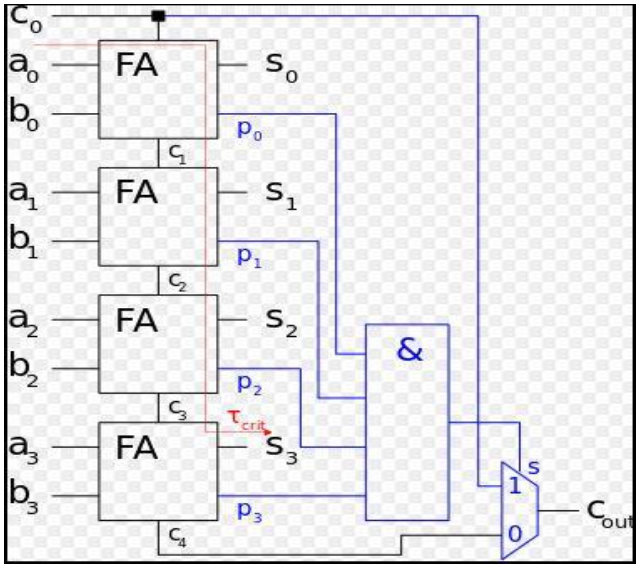

Fig 6: 4 bit carry skip adder block diagram

II. STRUCTURE OF THE MODIFIED HYBRID ADDER

A.. CMOS Technology

Complementary metal oxide semiconductor metal abbreviated as (CMOS) can be a technology to build integrated circuits. This CMOS technology is used in microprocessors, microcontrollers, static RAM and different digital logic circuits. CMOS technology is generally used for many analog circuits like image sensors (CMOS sensor), information converters and extremely integrated transceivers for various types of communication. In 1963, while operating for Fairchild Semiconductor, CMOS patented by Frank Wanlass (US Patent Three, 356,858) CMOS is also generally cited as a semiconductor composed of complementary symmetry metal (or COS-MOS). The words "complementary symmetry" require the real fact that the standard style mode with CMOS uses complementary and symmetric pairs of P-type and N-type metal semiconductor field transistors (MOSFETs) for logical functions. CMOS units have two essential characteristics: high noise immunity and low static energy consumption. Since an electronic test transistor is generally deactivated, the series combination momentarily attracts life energy only when passing from one state to another. As a result, CMOS devices do not produce the maximum amount of residual heat in the form of different types of logic, such as an example of electronic transistor logic (TTL) or NMOS logic, which normally have a constant current even when no state changes. CMOS together allows for a high density of logical functions on a chip. It is mainly for this reason that CMOS has become the most used technology in VLSI chips. The term "metal oxide semiconductor" may be relevant to the organic structure of the connected field effect transistors, which has a metal gate conductor positioned before Associate in a composite material for breastfeeding, which is subsequently su a semiconductor material. Once aluminum was used, but currently the fabric is made of poly silicon. Other metal ports have created a return with the arrival of insulating materials with high k content in the CMOS method, as stated by IBM and Intel for the 45 nanometer node and on the other side.

B. Brent Kung Adder

Parallel prefix additives are used to accelerate binary additions because they are very flexible. The Carry Look Ahead Adder (CLA) structure is used to obtain additives with a parallel prefix. Tree structures are used to increase the speed of arithmetic operation. Square measure of the parallel prefix adder used for high-performance arithmetic circuits in industries when the operating speed increases. The creation of the Adder prefix involves three steps:

1. Pretreatment phase
2. Transport the production network.
3. Post-treatment phase

Pre-possessing stage:

In this *Pre-possessing stage* the generation and propagation of signals to each pair of inputs A and B are calculated. The A and B signals are given by the following equations:

$Pi=A_i$ xor B_i (1)

G_i =Ai and Bi (2)

Carry generation network:

At this network, we calculate a port equivalent to each bit. The implementation and design of these operations is done in parallel. After calculating the parallel transport, they are segmented into smaller pieces. Propagation and carry generation are as intermediate signals which are given aslogic.

Post processing Stage:

This is the last step to calculate the sum of the input bits. It is common to all additives and the sum bits are calculated using logical equations 3 and 4.: Ci-1= (Pi and Cin) or Gi (3)

SI=PI XOR CI-1. (4)

III. METHODOLOGY

Full adder circuit can be realized by using two half adder circuits. Each half adder consists of EXOR and AND logic gates.

1. The ripple carry adder uses blocks of full adder circuits where carry is propagated through all the blocks.
2. For designing the carry select adder, we use four blocks of Brent kung adder and the multiplexer circuits which acts as the unit selection unit.
3. A BEC unit is designed by using EXOR and AND logic gates.
4. The BEC unit is proposed for carry select adder by replacing with one of the RCA present in the conventional CSA.
5. This project is realised in cadence design systems on virtuoso tool.

IV. IMPLEMENTATION OF BRENT KUNG ADDER:

The Brent-Kung adder could be a terribly known indexer design that offers an optimal variety of nursing assistant steps, from entry to exit or all exits, but with an uneven load at all stages intermediate. It is one of the parallel prefix additives. Parallel prefix additives are a unique class of additives based on the use of generation and propagation signals. The cost and quality of the wiring are lower in Kung Goose additives. But the depth of the gate level of the Brent-Kung adders is zero (log 2 (n)), since the speed is lower. The block diagram of the 4-bit Brent-Kung adder is illustrated in Figure 7.

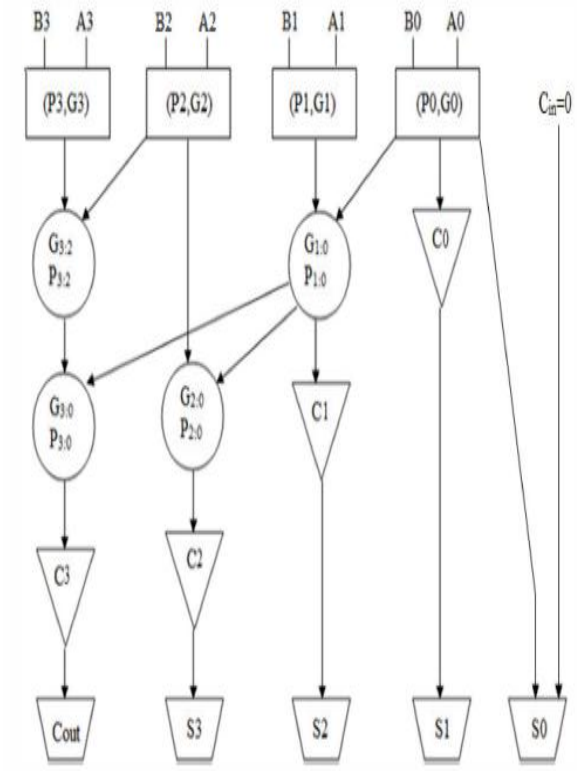

Fig 7: The conventional carry select adder block diagram

A.Full Adder with 28 Transistor:

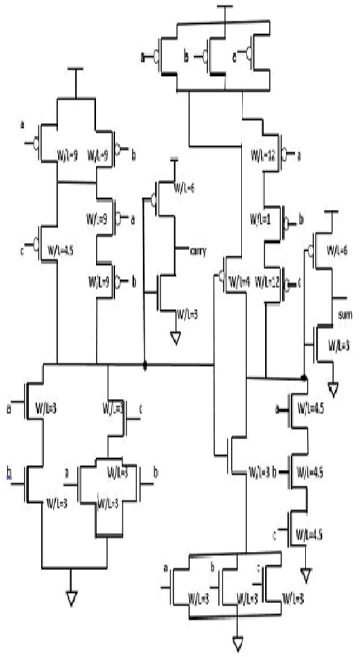

Fig 8 : Block diagram of full adder with 28 transistor

B . Full Adder using Boolean logic:

The common Boolean logical term, we just need to implement an XOR gate and a NOT gate to generate the sum pair. And to generate the load torque, we must implement an OR gate and an AND gate. In this way, the addition and transport circuits can be kept parallel. When analyzing the truth table of the complete single bit adder, the results show that the output of the sum signal as input signal is logic "0" is an inverse signal of itself, because the input signal is logic "1".

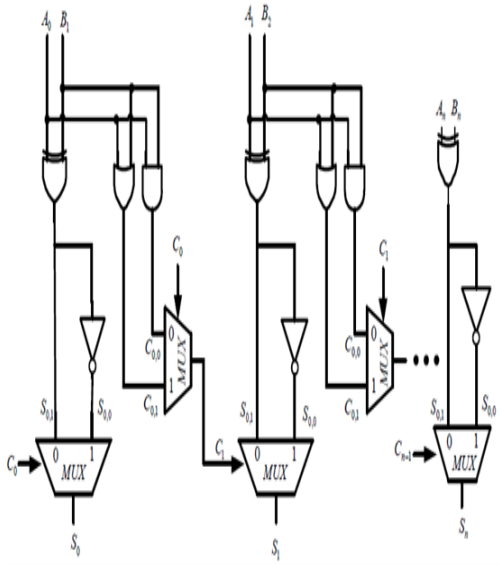

Fig 9 : Block diagram of full adder using Boolean Logic

C. Multiplier

The class-educated method for multiplying decimal numbers is based on the partial merchandise scheme, moving them to the left to add them. The most difficult half is to obtain the partial merchandise, since that implies multiplying an extended range by one digit. A binary laptop wants exactly the same, however, with binary numbers. In binary cryptography, each long range is increased by one digit (either zero or 1), which is much easier than in decimal, because the product at zero or 1 is only 0 or the same number. Therefore, the multiplication of 2 binary numbers is reduced to the partial scheme of the merchandise (which unit of area is zero or the primary number), moving them to the left, so that they add up

The emergence of single-chip multipliers and their integration into microprocessor architectures is the arrival of single-chip multipliers, and their integration into microprocessor architectures is due to the availability of commercial VLSI chips capable of DSP functions called parallel or matrix multipliers. The most important reason is the complementary multiplication of two binary numbers to produce a product in one processor cycle. Multiplication schemes were based on software such as shift and add algorithms or microcoded controllers that implement the same algorithm in hardware. Both options require multiple processor cycles to complete the multiplication. Advances in VLSI technology, both in speed and size, have enabled the implementation of parallel multiplier hardware.

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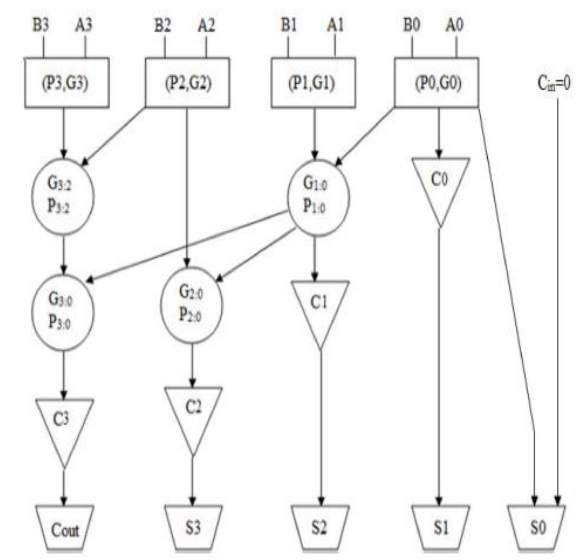
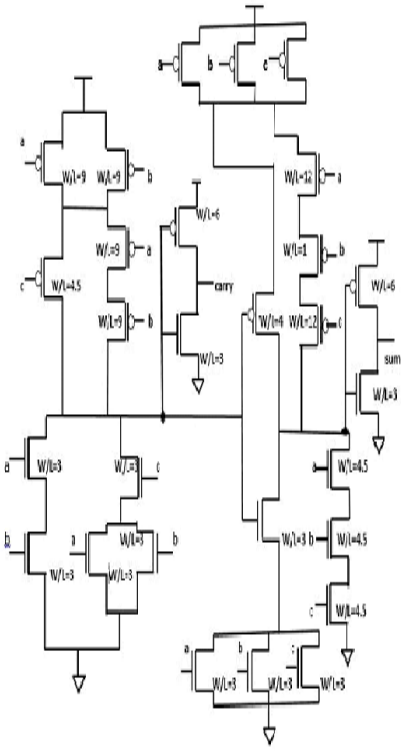


Fig 7: The conventional carry select adder block diagram

A.Full Adder with 28 Transistor:



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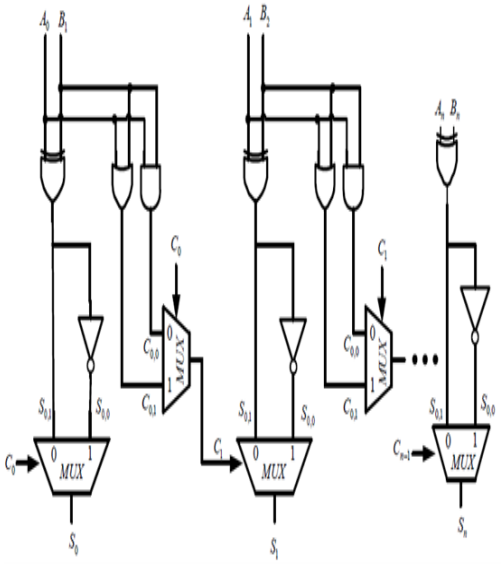

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VI. SIMULATION RESULTS

A.4 Bit Brent Kung Adder

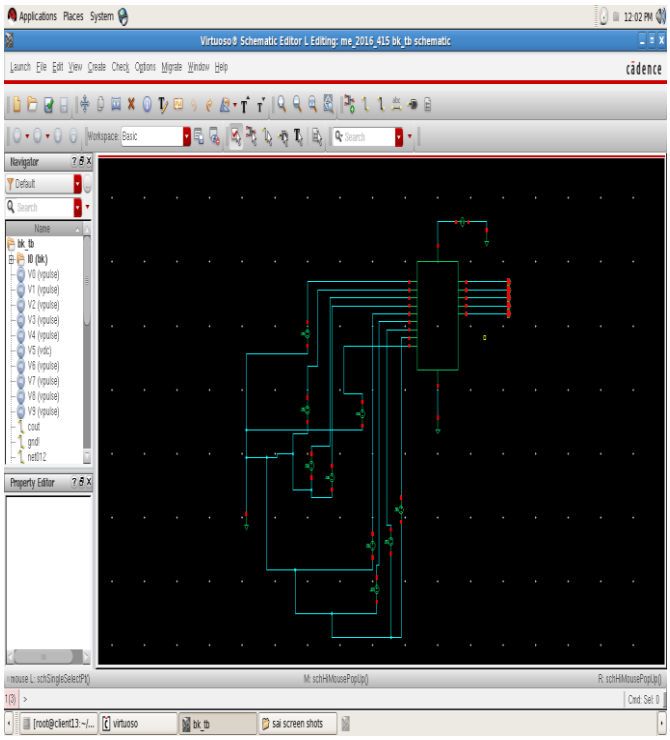


Fig 10: The Schematic of Brent Kung Adder using 4-bit

Outputs of the Brent Kung adder using 4 bit

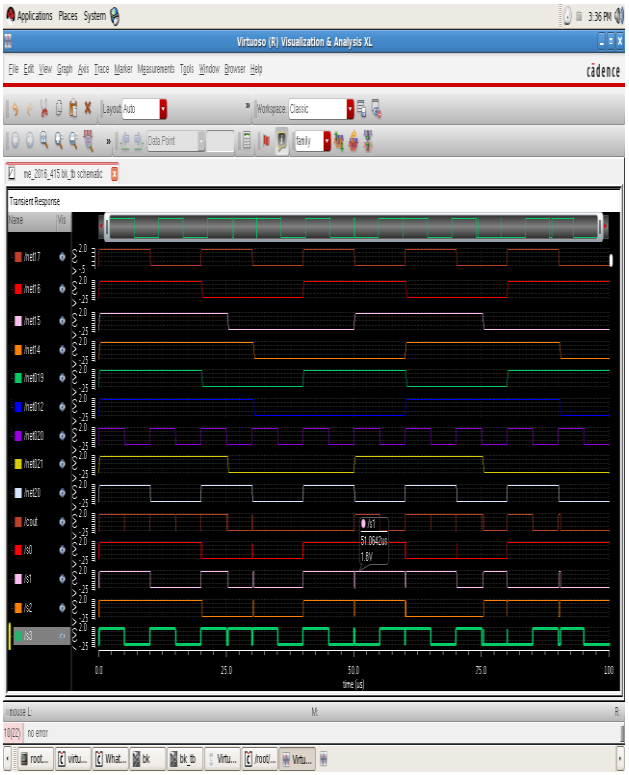


Fig 11 : Outputs of Brent Kung adder.

B. Simulations For Carry Select Adder Using Bk Adder

Carry Select Adder 16 Bit

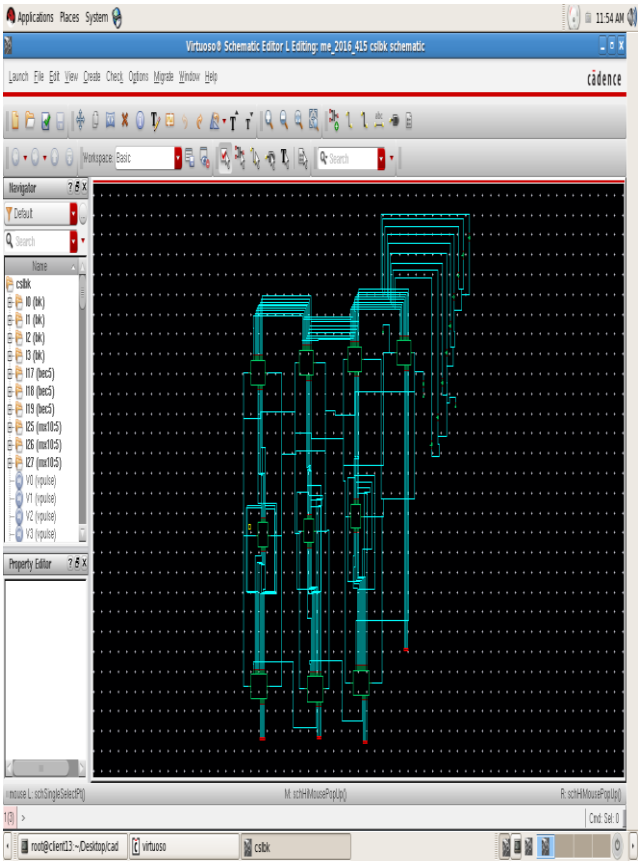


Fig 12: schematic of 16 bit carry select adder

Outputs Of Carry Selec Adder 16 BIT

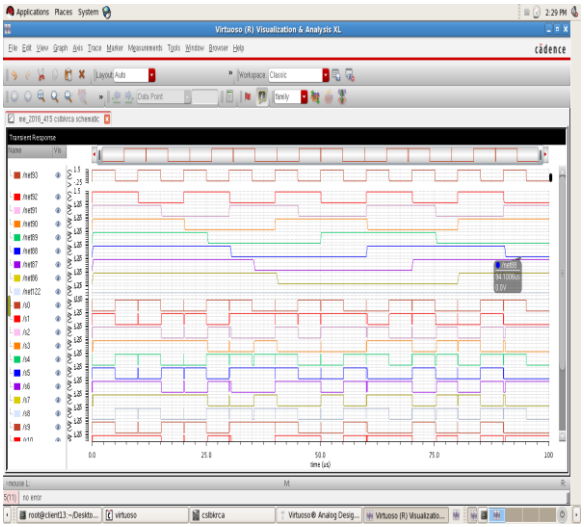


Fig 13: Outputs of carry select adder 16 bit

C. Simulations For Carry Select Adder Using Bec Unit

Outputs Of Bec Unit

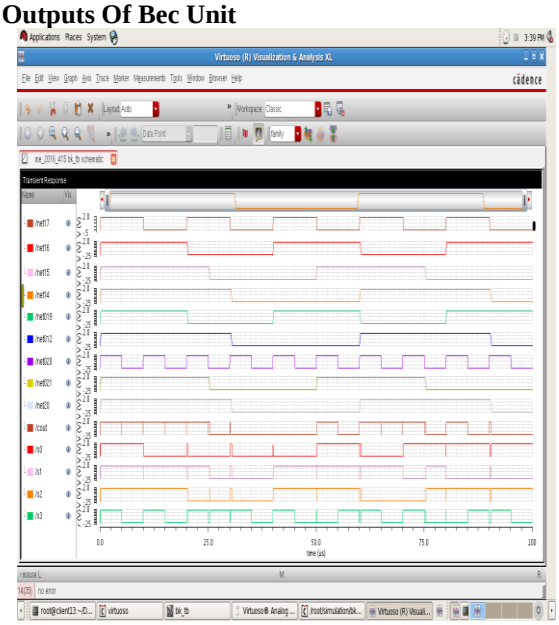


Fig 14: Outputs Of Bec Unit

Carry Select Adder 16 Bit(Using Bec)

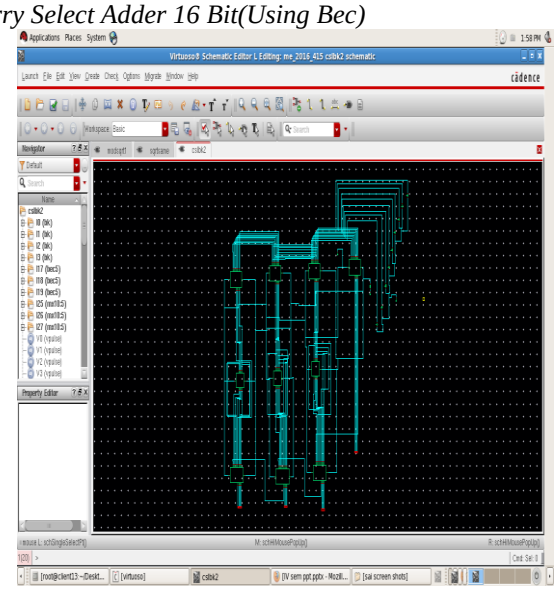


Fig 15: Schematic of Carry Select Adder using BEC

Outputs Of Carry Slect Adder Using Bec Unit

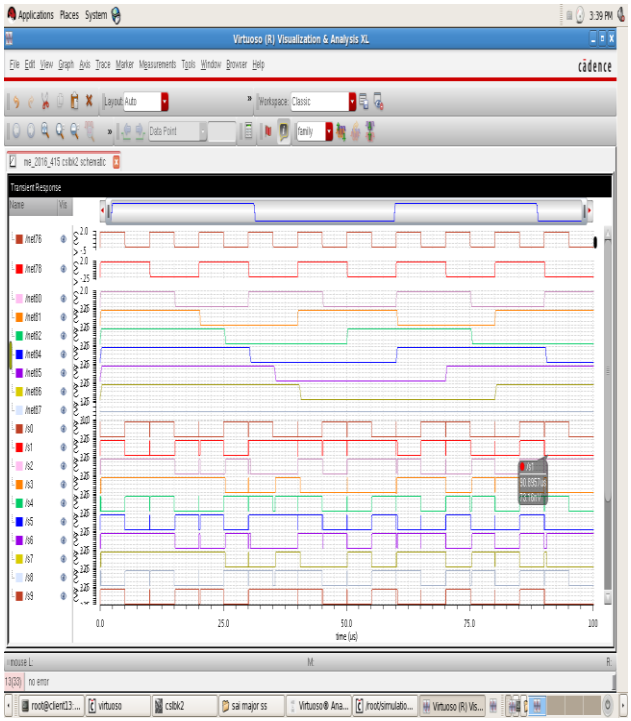


Fig 16: Schematic of Carry Select Adder using BEC

Square Root Carry Select Adder 16 Bit(Using Bec)

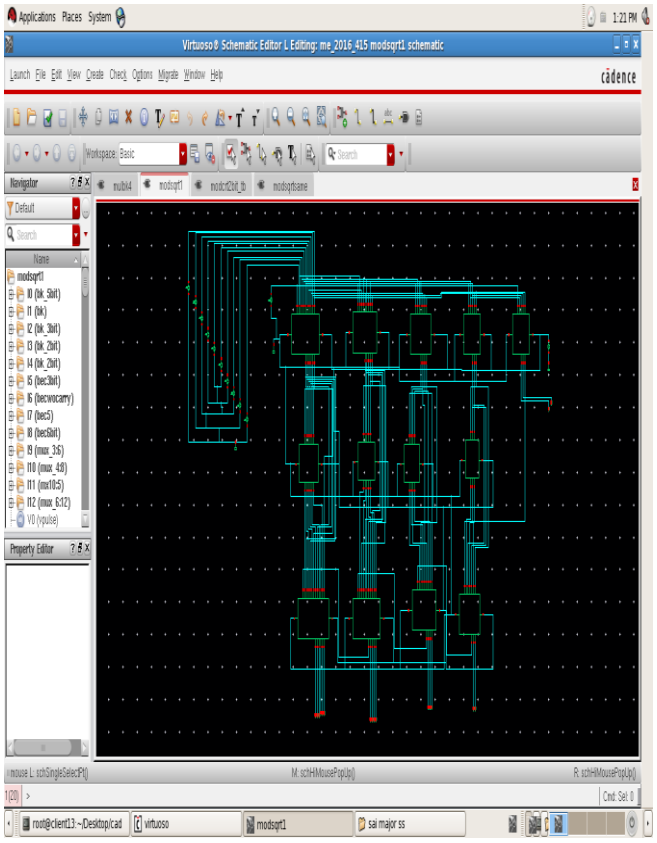


Fig 17 Schematic of Carry Select Adder using BEC

outputs of square root csa 16 bit(using 26 transistorsbec)

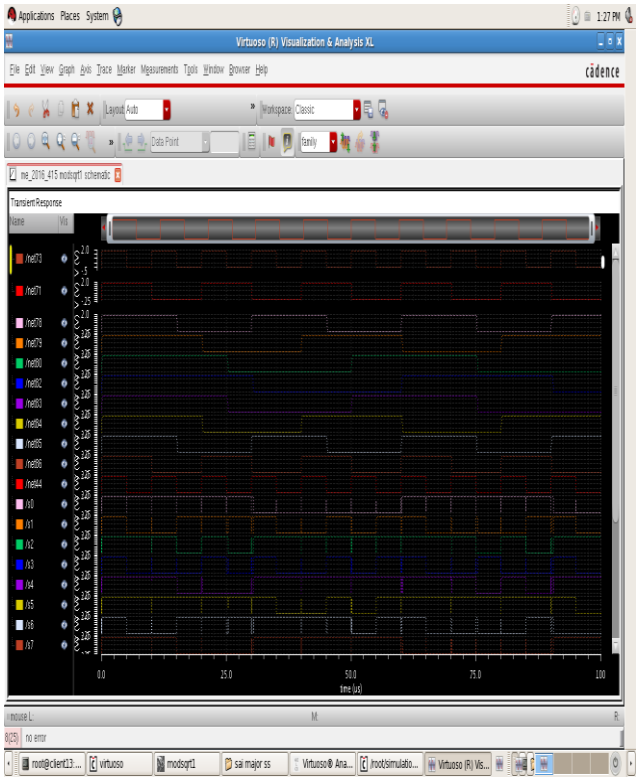


Fig 18: Schematic of Carry Select Adder with BEC

Simulations For Carry Select Adder Using 28 Transistor

Full Adder with 28 Transistors 1 Bit

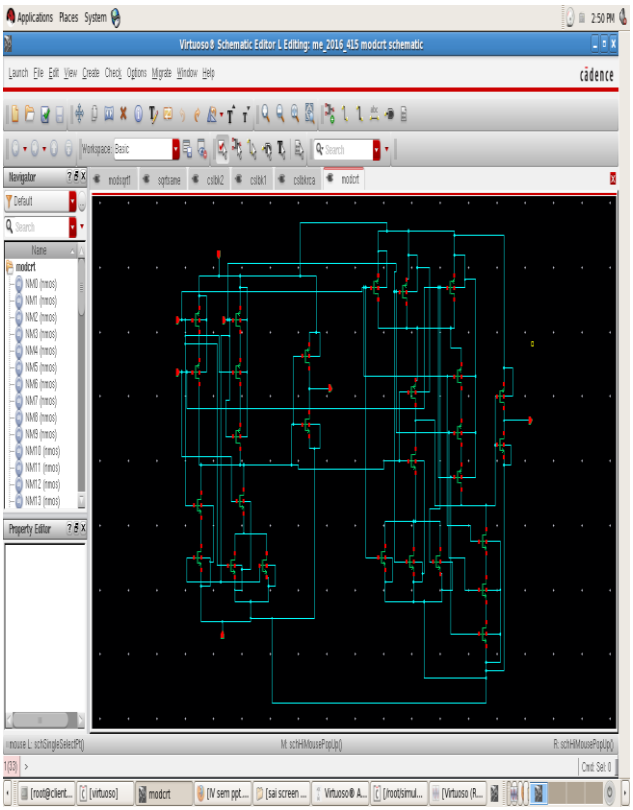


Fig 19: Schematic of Full Adder using 28 Transistors

Outputs Of Full Adder Using 28 Transistors

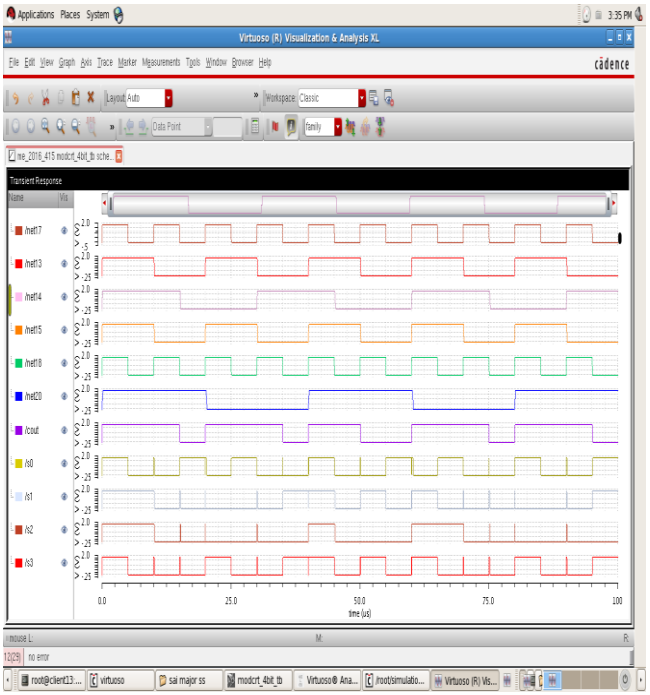


Fig 20: Outputs of Full Adder with 28 Transistors

Carry Select Adder with 28 Transistor

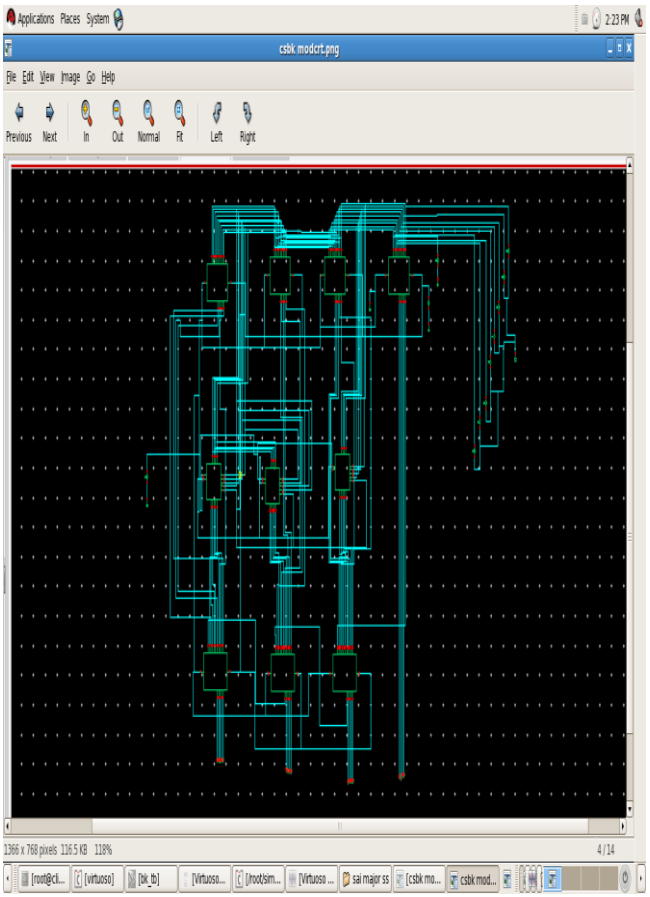


Fig 21 : Schematic of Carry Select Adder using 28 Transistors

Outputs Of Carry Select Adder Using 28 Transistor

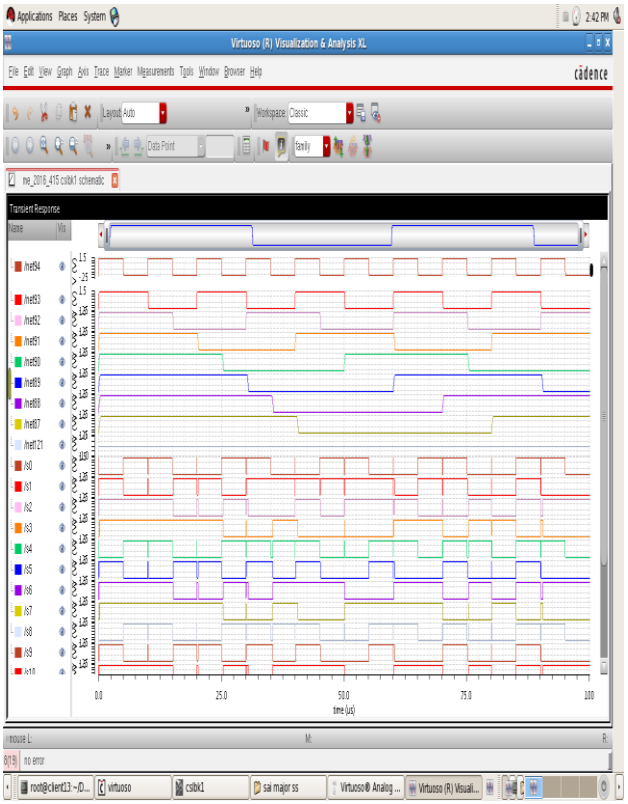


Fig 22: Outputs of Carry Select Adder using 28 Transistors

Square Rooot Carry Select Adder Using 28 Transistor

Fig 22: Schematic of Carry Select Adder using 28 Transistors

Outputs Of Square Root Csa Using 28 Transistor

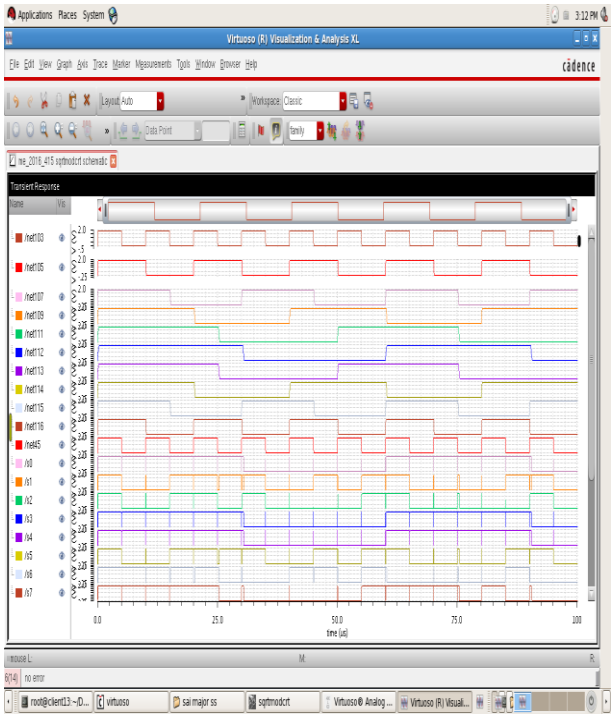
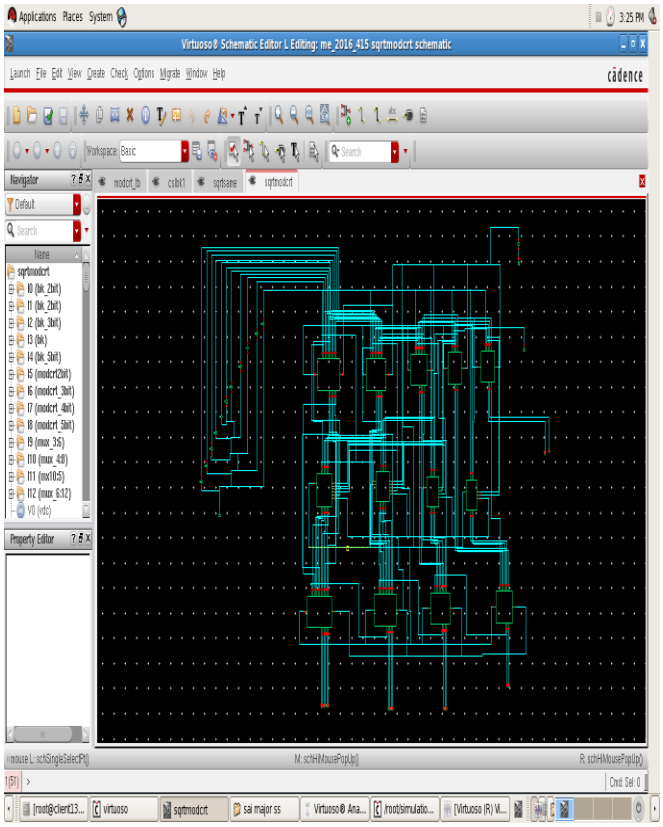


Fig 21: Outputs of Carry Select Adder using 28 Transistors

Simulations Of Carry Select Adder Usingboolean Logic.
Full Adder Using Boolean Logic 1 Bit



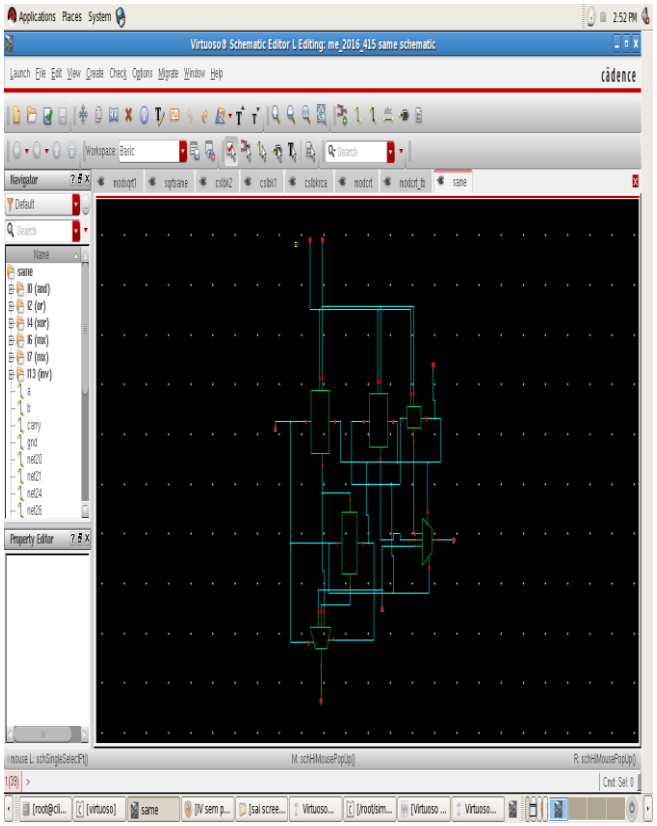


Fig 22 : The Boolean Logic Full Adder Schematic

The Boolean Logic Outputs Of Full Adder

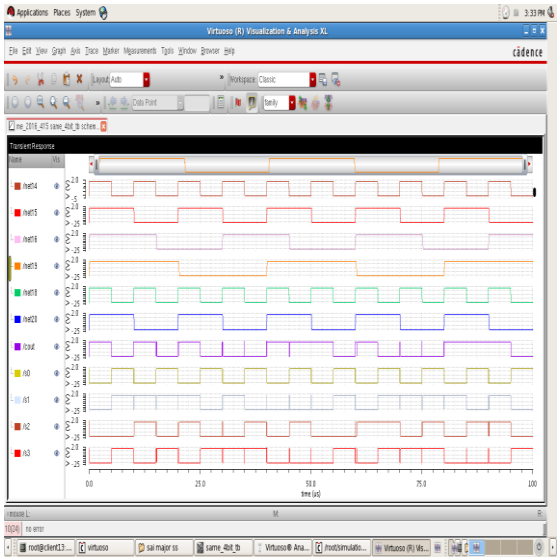


Fig 23: The Outputs of Full Adder with 28 Transistors

Using the Boolean Logic the Carry Select Adder Adder

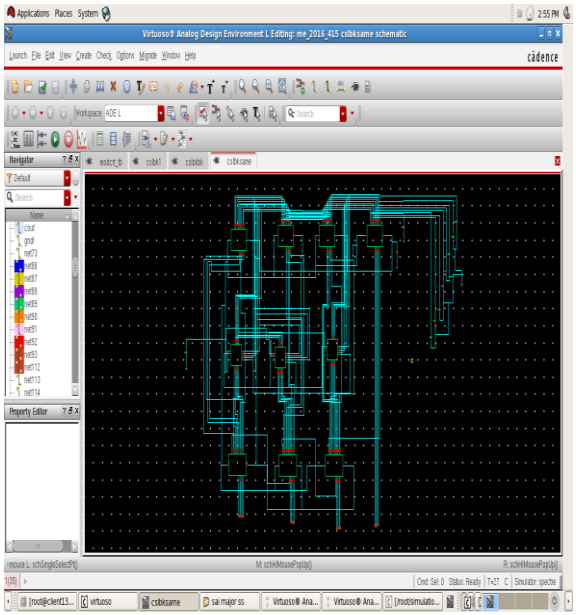


Fig 24: Boolean Logic Carry Select Adder Schematic

The Boolean Logic Outputs Of Carry Select Adder

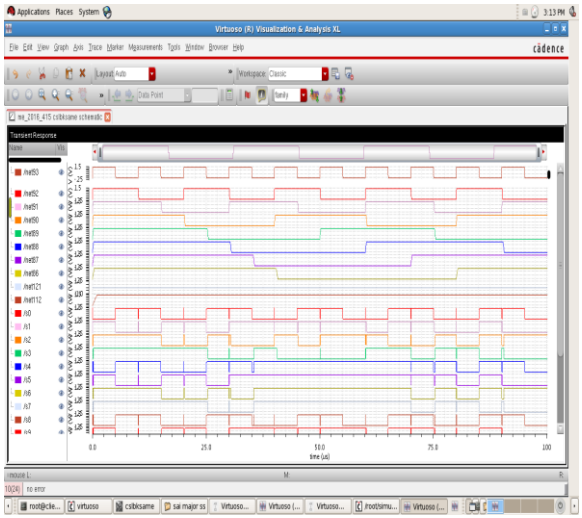


Fig 25: The Boolean Logic Carry Select Adder Outputs

Using Boolean Logic the Square Root Csa Adder

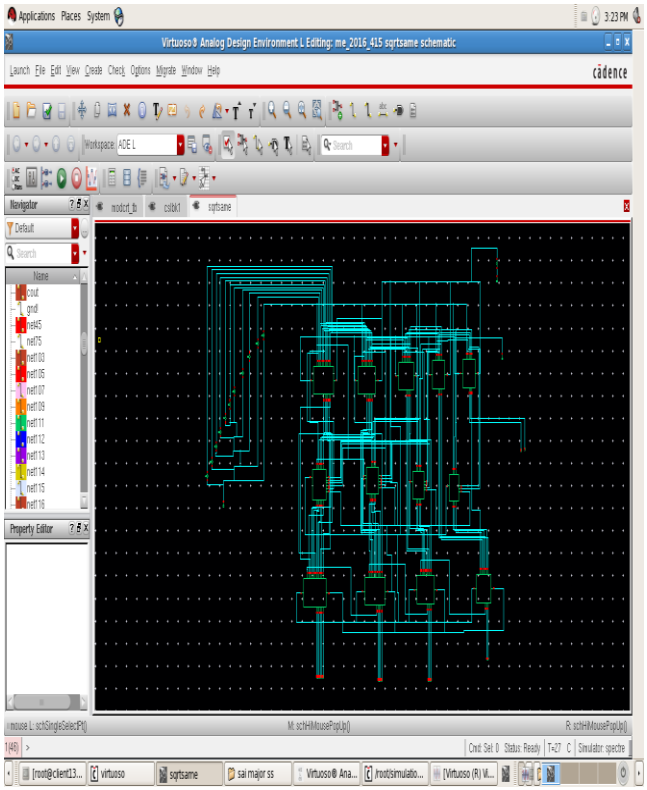


Fig 26: The Boolean Logic Carry Select Adder Schematic

Outputs Of Square Root Csa Adder Using Boolean logic

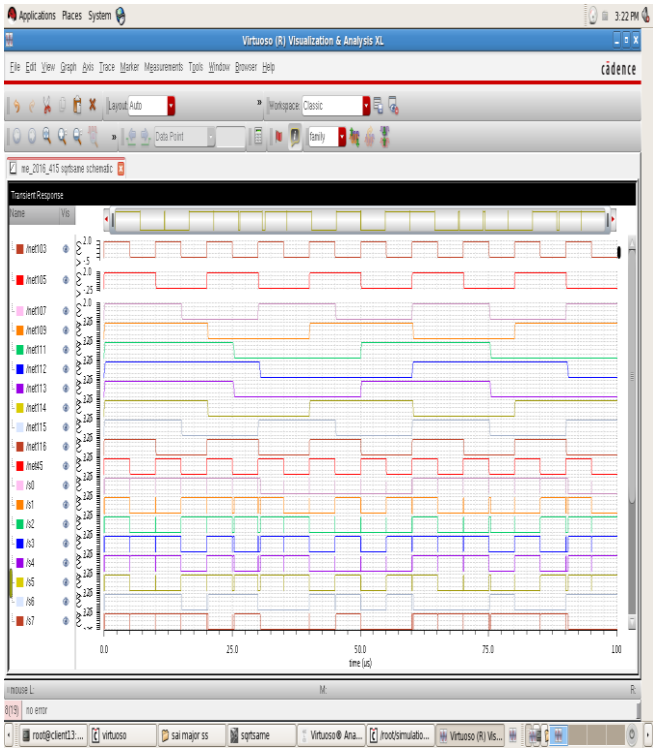


Fig 27: The Boolean Logic Carry Select Adder Outputs

Simulations Of Multiplier
Multiplier(4x4) Using Brent Kung Adder

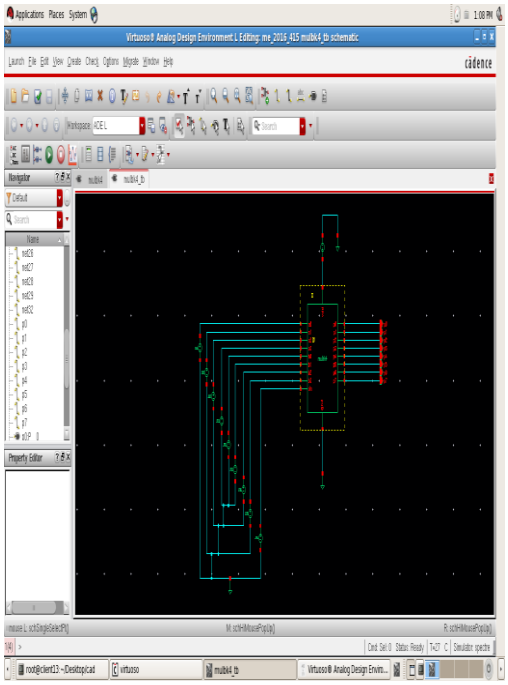


Fig 28: Test Bench of Multiplier using BK Adder

Outputs Of Multiplier(4x4) Using Brent Kung Adder

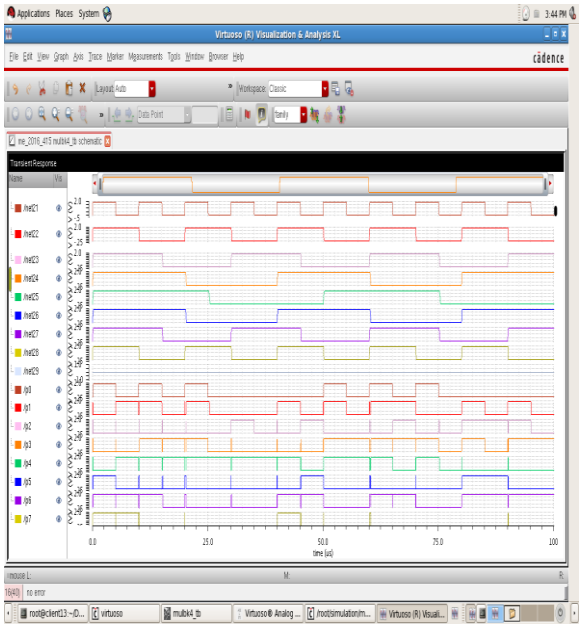


Fig 29: Outputs of Multiplier using BK Adder Naive Bayes

VII. CONCLUSION

In this project, a Brent Kung CMOS static adder structure was designed, which has energy consumption is lower and speed is high than corrugated transport adductors. Due to the modifying structure by adding a Brent kung adder, using complete integrators (28 transistors, Boolean logic) the speed was achieved by which is much faster than the carry operator of rippling and incriminating techniques. These speed adders will result in increase in DSP processors. The work can be further extended by applying the Brent Kung adder in Booth Multiplier and various Multipliers. The use of parallel prefix network helps in increasing the slack time in the structure.

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