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Efficient Design of Control Logic Block in Dual Port Memory

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Abstract: ***A dual port memory in QCA is a study of data in different ports, but the data conflicts are very difficult to identify. Dual port memory is mainly focused on the data priority. It can be generated from the design of the control logic block. Priority bit are used, where both ports access the same memory location. Dual port memory functionality can be identified with a priority bit. When the port having the same memory location, only the port having the high priority is selected and other port are discarded. But when the read operation are requested to both the ports at same locations, having no conflicts and both the ports are requested to perform read operations. Data conflicts on the SRAM cell can be overcome by discarding the lower priority completely. Priorities are defined in terms of the area and delay. The idea behind this work is to minimize the area and delay in the dual port memory and proposed a multilayer Cross-Over design to provide an efficiency to the dual port memory and simulation result of design are shown in QCA Designer Tool-2.0.***

Keywords: QCA, multiple crossovers.

I. INTRODUCTION

QCA could be a feasible alternative that promises operation at high frequency with low power consumption and high device density. QCA is based on the confinement and mutual repulsion of electrons. The fundamental element in QCA is a squared cell with four dots and two excess electrons. Therefore, unlike the conventional CMOS, a change in logic value from 1 to 0 does not yield discharging of the capacitor. It also offers a new horizon in information computation. The information is transferred as a result of the propagation of polarization between two cells, due to the Coulombic interaction of electrons. There is no flow of current as in conventional CMOS. Hence, power dissipation due to change in logic value and propagation does not add up to the total power dissipation. This feature makes QCA useful for computation.

1. Small size
2. Consume less power
3. High speed

The efficient design of dual port memory is based on reducing the area of cells and increase speed of polarization process. The main building block of the proposed dual port memory is macro memory cell, decoder, address checker block, control logic block.single layer QCA cells is almost impossible when compared to the fabrication feasibility of the multilayer design[1-5].

II. RELATED WORKS

The efficient dual port is achieved in a multilayer and it is evaluated in terms of area, latency and logic gates. .The proposed structures performance is low interms of area, latency and power consumption ,a new and efficient architecture for 2x4 decoder , macro memory cell, decoder, address checker block, control logic block are implemented with the crossover .Parameters like density, logic gates and latency are considered in order to confirm faster operating speed and high device density**[6,7].**

III. QCA ARCHITECTURE

A.QCA CELLS

The cells are charged with two electrons which can be allowed to tunnel between the different quantum dots by a clocking mechanism. These electrons are tend to occupy the antipodal sites as a result of their mutual electrostatic repulsion force [8-10].

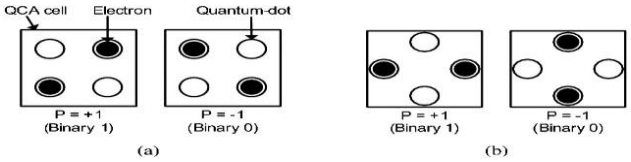

Fig.1 QCA cells

B.QCA WIRES

The wires are a horizontal row of QCA cells and a binary signal propagates from input to output because of their electrostatic interactions between adjacent cells.The electrons will be located diagonally because the cell are charged with two extra electrons. This is because of the columbic repulsion forces which do not allow them to locate in other arrangements[11-15]

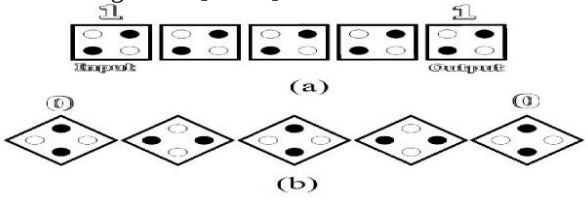

Fig.2 QCA wires

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Fig.2 shows the QCA wires are in which the electron in one cell are located in a special diagonal (logic 1), this polarization induces the electrons in neighbor cells, QCA to be located with the same polarization. In 45˚ wire, propagation of binary signal alternates between the two polarizations.

C.QCA INVERTER

The electrostatic interaction are inverted, because the quantum-dots corresponding to different polarizations are misalinged between the cells. That is, the binary information stored in cell 1 is transferred to cells 2 and then to cell 6. The cell 7 interacts with its neighbouring cells 5 and cells 6 to increase the columbic interaction and switching of the elctron state with opposite polarization [16-18].

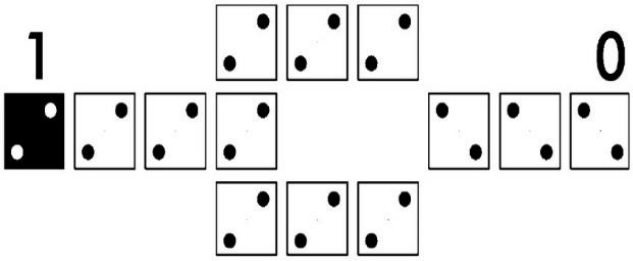

Fig.3 QCA inverter

Fig.3 shows the QCA inverter can be demonstrated in two ways such as positioning and rotation.

D.MULTILAYER CROSSOVER DESIGN

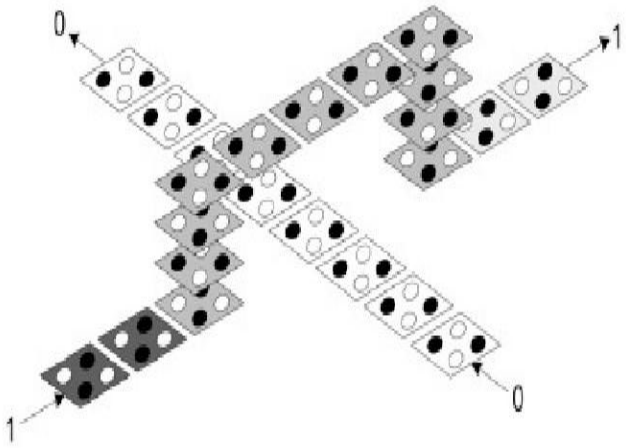

Fig.4 Multilayer crossover

Fig.4 shows the Multilayer cross-over design in which the circuits can be potentially consume much less area.

IV. EXISTING SYSTEM

A.MACRO MEMORY CELLS

Proposed QCA memory cells are made of QCA logic gates, i.e., AND, OR and NOT gates. Both the *write/read* and *row select* wires of the same port are polarized to 1 until the stored data are constantly calculated inside the memory loop. The current memory value inside the loop are fed to the output, if the row select are polarized to 1 and the ***write****/read* are polarized to 0 . Data input of priority port are considered as the input line for the memory cell.

B.DECODER

Since it is a dual port memory, two memory cells are selected at the same time. In QCA block of 2 X 4 decoder in dual port memory, two memory cells are selected at the same time to generate the address for both ports.

C.ADDRESS CHECKER BLOCK(ACB)

Address Checker Block are used to check the inputs of the two ports whether they are equal or not. This can be done by using two decoders, if both the inputs are equal they go to the same AND gate and the output will be one. The output '1' indicates the address of the two ports are equal and output '0' indicates the address of the ports are different.In this block it is used check the inputs of the two ports whether they are equal or not. This can be done by using two decoders.

D.CONTROL LOGIC BLOCK

The control logic block are consisting of *write/read* signals of two ports as well as a control input. CLB produces the priorities for both ports. The address of two decoders are compared to check whether they are same or not in the first step. If the address of the both ports are same no conflicts occurs and if the address of both port are same conflicts.

V.PROPOSED SYSTEM

A.FIVE INPUT MAJORITY GATE

The structure of our proposed majority gate comprises 10 quantum-dot cells, 5 inputs, 1 output, and 4 middle cell. It is easy to access the cells with an additional layers in the design. A five input majority gate, *MAJ5* is a Boolean gate whose output is 1 only if 3 or more of its input is 1.The Boolean expression of *MAJ5* function is given by:

MAJ5(A,B,C,D,E)=ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE

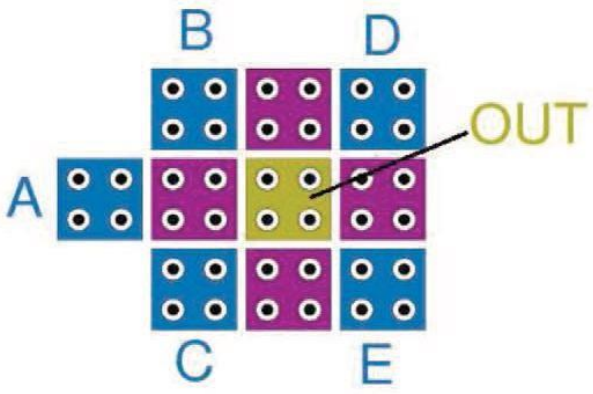

Fig.5 Five Input Majority Gate using 10 cells

Fig.5 shows the five input majority gate and it is extremely versatile and can be readily used to implement a variety of functions by trying some of the inputs to constants and duplicating some inputs. A one bit full adder is designed, . By using this five input majority gate. A full adder is one of the rudimentary components in most digital circuits, having very fast and less complex adders are significantly important.

B.MULTILAYER CROSSOVER

The multilayer crossover are used in order to reduce the area ,time delay and cell count in the dual port memory to make a dual port more efficient.

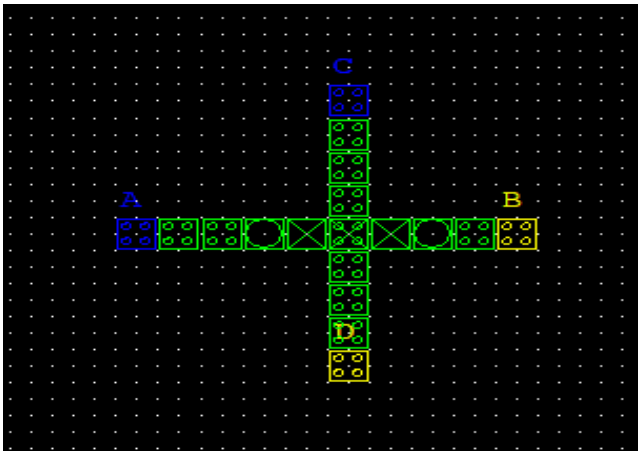

Fig.6 Multilayer Crossover Design

Fig.6 shows the Multilayer Cross Over Design.

Simulation and Result of Multilayer Crossover Design

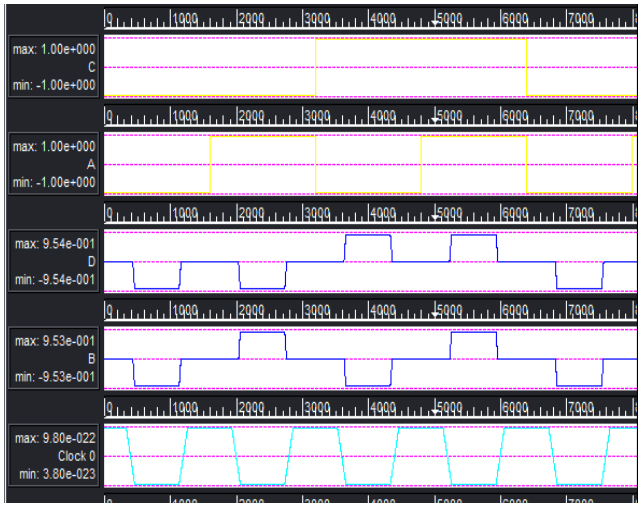

Fig.7 Simulation of Multilayer Crossover Design

Fig.7 shows the simulation of Multilayer Cross-Over Design. In this design the delay has been reduced when compared to the existing method.

C.SCHEMATIC AND SIMULATION OF 2 X 4 DECODER

In it all design are designed by using crossover to reduce the area of the memory cell. The schematic and simulation of 2x4 Decoder circuits are designed

Schematic of 2x4 Decoder

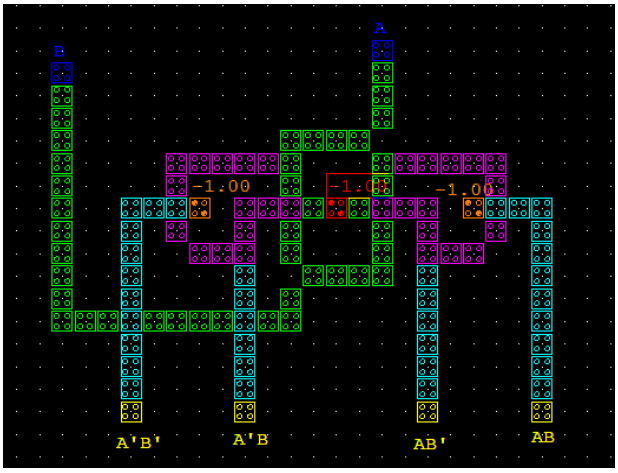

Fig.8 2x4 Decoder

Fig.8 shows the schematic diagram of 2 x 4 Decoder in which two memory cells are selected at the same time. So the decoders are used to generate addresses for both ports. Therefore, we need a decoder to generate a 'row select' signal for addressing an appropriate memory array.

Simulation Results Of 2x4 Decoder

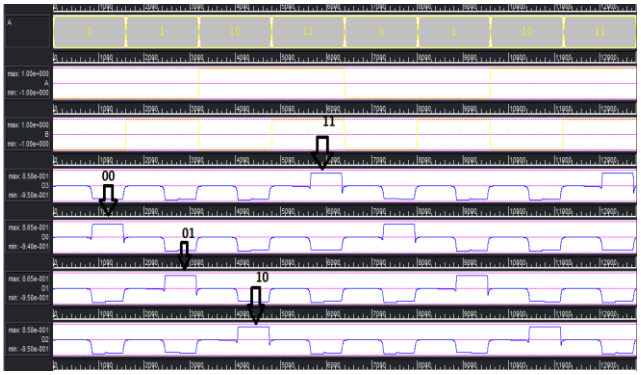

Fig.9 Simulation of 2x4 Decoder

Fig.9 shows the simulation output of the 2x4 Decoder where the D0 will be 1 if both the inputs are 0, D1 will be 1 if A is 0 and B is 1 , D2 will be 1 if A is 1 and B is 0 and D3 will be 1 if both inputs are 1.

Table 1: Comparison of 2x4 Decoder with Existing System

PARAMETERS	EXISTING SYSTEM	PR0POSED SYSTEM
NUMBER OF CELLS	104	63
AREA(µm^2)	0.15	0.07
DELAY	0.75	NO DELAY

Table 1 shows the number of cells, area and delay for Existing Decoder and Proposed decoder.

D.SCHEMATIC AND SIMULATION OF ADDRESS CHECKER BLOCK

In it ,all the design are designed by using crossover to rreduce the area of the memory cell.The schematic and ssimulation of Address Checker Block are designed.

Schematic of Address Checker Block

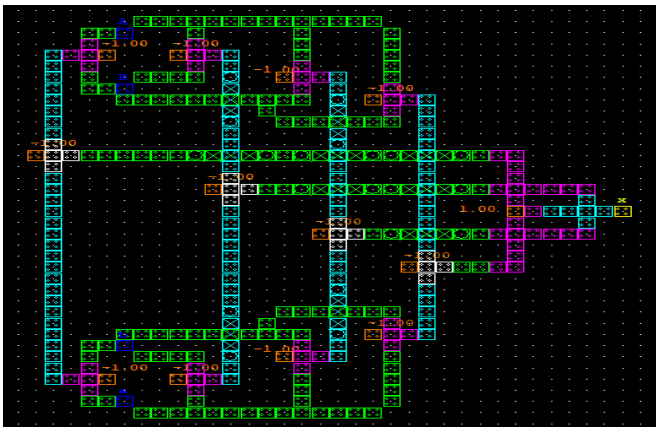

Fig.10 Address Checker Block

Fig.10 shows the Schematic diagram of Address Checker Block and it is used to check the inputs of the two ports whether they are equal or not. This can be done by using two decoders.

Simulation Results Of Address Checker Block(ACB)

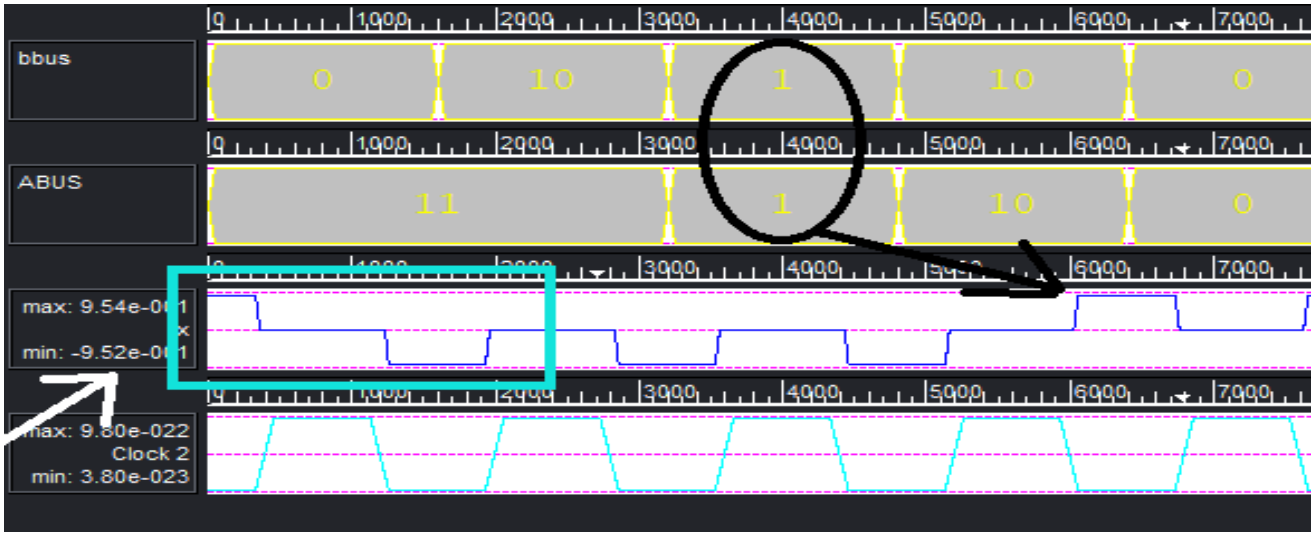

Fig.11 Simulation of Address Checker Block

Fig.11 shows the Simulation result of the Address Checker Block(ACB) where the output will be one if both the address are same or the output will be zero.

Table II: Comparison of Address Checker Block with Existing System

PARAMETERS	EXISTING SYSTEM	PROPSED SYSTEM
NUMBER OF CELLS	427	382
AREA(μm^2)	0.89	0.49
DELAY	1.75	1.25

Table II shows the number of cells, area and delay for Existing ACB block and Proposed ACB block.

E.SCHEMATIC AND SIMULATION OF CONTROL LOGIC BLOCK

In it ,all the design are designed by using crossover to reduce the area of the memory cell.The schematic and simulation of Control logic Block are designed.

Schematic of Control Logic Block

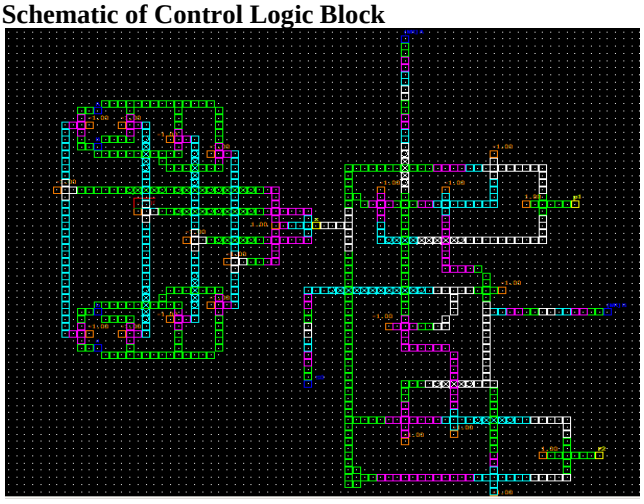

Fig.12 Control Logic Block

Fig.12 shows the schematic diagram of Control Logic Block(CLB) and in this produces the priorities as well as the *write/read* signals for both ports. In this block, the address of two decoders are compared to check whether they are same or not.

F.Simulation Result of Control Logic Block

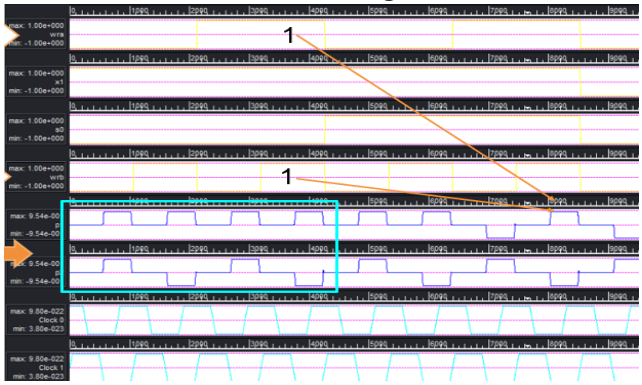

Fig.13 shows the simulation result of the control Logic Block(CLB) of the proposed system.

Table III: Comparison of Control Logic Block with Existing System

PARAMETERS	EXISTING SYSTEM	PROPOSED SYSTEM
NUMBERE OF CELLS	805	713
AREA(μm^2)	2.40	1.14
DELAY	3.25	4

Table III shows the number of cells, area and delay for Existing CLB block and Proposed CLB block

Table IV: Overall comparison between the existing and the proposed System

BLOCKS	PARAMETERS	EXISTING SYSTEM	PRPOSED SYSTEM
DECODER	NUMBER OF CELLS	104	63
	AREA(μm^2)	0.15	0.07
	DELAY	0.75	NO DELAY
ADDRESS CHECKER BLOCK	NUMBER OF CELLS	427	382
	AREA(μm^2)	0.89	0.49
	DELAY	1.75	1.25
CONTROL LOGIC BLOCK	NUMBER OF CELLS	805	713
	AREA(μm^2)	2.4	1.14
	DELAY	3.25	4

Table IV shows the overall comparison between the Existing System and Proposed system

VI. CONCLUSION AND FUTURE SCOPE

The architecture is based on the priority and the circuit is synchronized. Priorities of two ports are generated from control logic block. The proposed architecture resolves the data conflicts problem by discarding, the priority signal of the port having less priority and send a priority bit to the memory cells.In our design , we optimized the area of the decoder by 53%, the area of the address
checker block by 45% and the area of the control logic block by 52.5%.
In future the results confirmed that the presented structures have outperformed all prior designs in term of new cost function and showed significant improvements in terms of complexity, area occupation and input to output clock delay as compared to most of the designs. Further, in future, a simple clock-based approach will be incorporated to enable.

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