

Design of Low Power 6T Sram with and without ROFs



C. Gangaiah Yadav, K. S. Vijula Grace

Abstract: An aggressive scaling in size and the increasing number of the transistor count are the important challenge of the design of Integrated Circuit (IC). In the same manner interconnection lines and resistive opens also became a major problem in present nanometer technology. The resistive open faults [ROFs] represent degradation [1] in connectivity's within a circuit's interconnections because of unavoidable manufacturing failures present in both current and future developing technologies. The resistive open fault [ROF] is an imperfect circuit connection that can be modelled as a defect resistors between two nodes of the circuit. The Resistive open faults [2] not causes the functionality of the circuit instantly. But, it causes the delay faults. In this research proposal, the impact of resistive open faults measured in 6-Transistors (6T) Static RAM memory cell design. The proposed 6T Static RAM memory cell implemented in 45nm technology by using Cadence Virtuoso library. The main goal of this proposed research work is to analyse the effect of resistive open faults and how it reduce delay and power of 6T Static RAM cell. The resultant outputs of proposed 6T SRAM cell operation with and without ROFs will be compared.

Keywords: Resistive Open Faults [ROFs], Delay Faults, Conductivity, 6T SRAM, Area, Current, Power dissipation, Delay.

I. INTRODUCTION

Advanced technologies are unfortunately affected by a number of unwanted side effects. Increased the level of the leakage current is one of the major reason of undesired side effect. Hence, higher power dissipation and leakage currents represent a significant challenge for the employ of current based parametric test quiescent test and all current based test methods. A more serious effect causes by high leakage current [3] is the functionality failing of Static RAM cell, which can be modelled with data retention faults where the memory cell lost stored value due to the leakage current. In fig.1 shown circuit diagram of 6T-Static RAM cell design. The 6T-SRAM memory cell is designed by considering of two different operations are Read and Write operations. In SRAM cell, reading operation during data is requeansted and writing operation during updating the contents.

The SRAM cell design to operate in the read and write mode operation should have reliability and write stability, respectively.

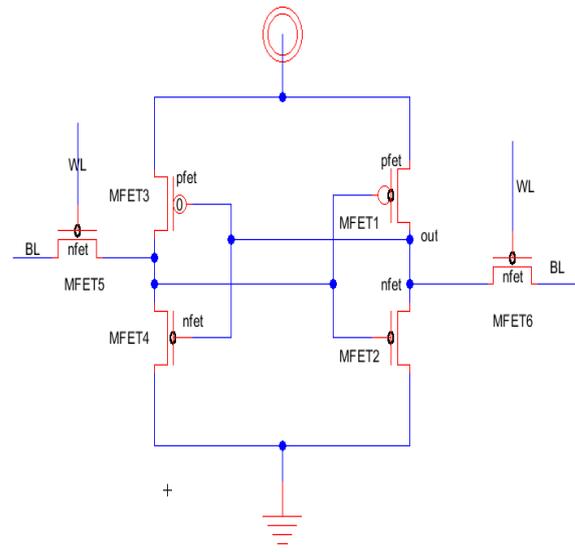


Fig.1. 6T SRAM cell design

The brief organisation of this work as follows: The 6T Static RAM read and write operations described in below Section II & Section III. The existing design of 6T Static RAM described in below Section IV. The circuit designing process in cadence virtuoso tool described in below Section V. The impact of ROFs on 6T Static RAM circuit explained and discussed in below Section VI. Concluding remarks are presented in section VII.

II. 6T SRAM WITHOUT RESISTOR

For read operation, both are Base Lines (BLs) like BL and BL_b precharged to VDD. When the Write Lines (WLs) goes to high (logic 1) enables the access transistors. The read pulse will store in memory after that value is read. If internal node Q value is logic 1 bit stored in memory when the internal node Q_bar is a logic 0 bit. At the time BL_bar is a logic 1 bit and internal node Q_bar is a logic 0 bit, here having voltage difference between BL_bar & Q_bar so that decrease the BL_bar voltage. And then BL and BL_bar value given to the sense amplifier, which is act as comparator circuit. Finally, the BL_bar output is logic 1 bit. Modifying the constant in the storage memory, if assume internal node Q value is logic 0 bit at the time the internal node (Q_bar) value is 1 bit. The WL= 1 value is required to write operation in the 6T-Static RAM. When WL=0, it is not possible for write operation.

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Here, input operations perform through the BL and BL_bar pins. After that, the BL_bar should be connected to ground because of the internal node Q value is 0 bit at the time Vdd value is 1 bit, here voltage is different so that entire system voltage is discharged.

And then, the BL_bar bit value is less compared to the threshold voltage MFET2 at the time MFET is turn on, which is based on BL_bar should be output is 1 bit. In this research proposal, we have added an extra resistor in the 6T SRAM for analyzing resistive open fault compared to the without resistor 6T-SRAM cell and 7T SRAM cell, Inverter Chain. Finally, the proposed method of the area, power, and delay are computed in the 45nm technology with Cadence SRAM library. The 6T SRAM without resistor is given in below figure.2.

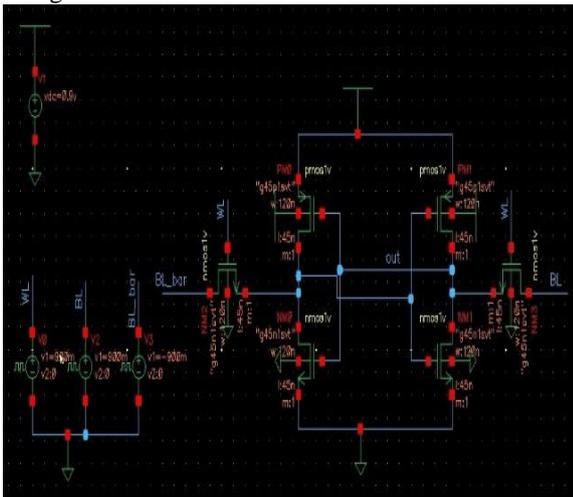


Fig.2. 6T SRAM without Resistor

III. 6T SRAM-WITH RESISTOR

The 6T SRAM with Resistive Open Faults [ROFs] is shown in below figure 3. Due to these resistive open faults [ROFs] degrades the conductivity [4] causes delay fault. This delay fault effect the circuit operation. That means it effect the read and write operation of the 6T SRAM. For read operation bit lines BL and BL_bar act as output lines. If WL=1 and inputs of inverters Q=1, Q_bar=0 at NM3 there is no voltage difference and BL is charged. Then read data 1 from memory at BL node. Here if ROF induced at NM3 location BL charged to Vdd slowly. So, Causes delay fault. Due to this delay the power consumption also increases and it is shown in table1 & 3. Similarly for read 0, BL will discharge due to voltage difference at NM3. The ROF also causes on this discharging operation. Similarly in Write operation the BL and BL_bar act as an input lines. If writing 1 into memory and ROF induced at bit line BL node, due to this ROF write bit 1 into memory slowly and causes delay fault. The library of 6T Static RAM with ROFs designed in cadence virtuoso tool. By using 6 Transistors each transistor L: W taken as a 45: 120 nm designed 6T Static RAM. In this design connected different resistors in between two nodes in the circuit, assumed it as a Resistive Open Faults [ROFs]. The area, power and delay of this 6T SRAM circuit derived by using cadence tool.

IV. EXISTING METHOD

In this section described about only current existing design method of 6T Static RAM. The 6T Static RAM memory cell consist of combination of weakly cross coupled inverters [5] hold the state, this circuit also consist of two access transistors for performing of read and write operations. The write operation is performed by driving the desired value and its compliment value into BL-Bit Line named as bit and bit_b, then raising the WL-word line named as word. The Over powering of the data is measured using the cross coupled inverters.

The pre-charging of two bit lines are set as high firstly and then set to float. When word is raised then bit_b is pulled down, and indicating the value of the data. The main challenge of the Static RAM is to ensure that the circuit holding the state is weakly enough to ensure the write operation by over powering the previous stored value and strong enough. So, that it can be retained during the read operation. Both of them should be ensured to perform proper READ and WRITE operations [6] respectively. Static RAM operations are divided into two phases.

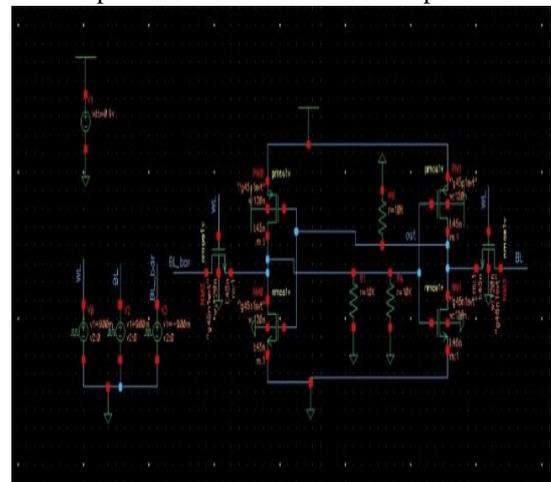


Fig.3. 6T SRAM with Resistor

Let the two phases be called as $\phi 1$ and $\phi 2$. These are generated generally from clk (clock) and its complimentary clk_b . In Phase 1, the read and write operations are performed. Here our main concern is phase 1 of Static RAM cell. The complete architecture of 6T Static RAM is given in below figure.4.

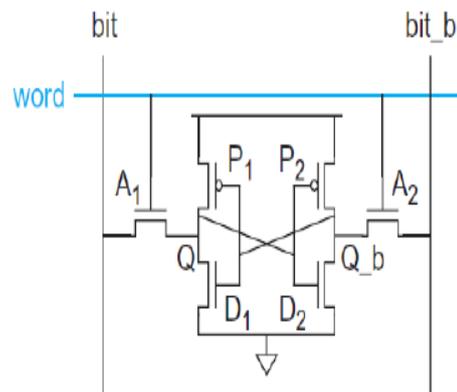


Fig.4 Detailed structure of 6T SRAM cell

V. DESIGN A TRANSISTOR IN CADENCE TOOL

CMOS Inverter design and simulation in Cadence tool must have account in UNIX/LINUX. The following steps describes the design and simulation of CMOS inverter.

First access UNIX/LINUX account by using login credentials. Then one terminal window will open.

Now run the Cadence tools into that system.

```
>> mkdir cadence
>> cd cadence
Now start Cadence by typing
>> csh
>> source cshrc
>> cd cadence_ms_labs_613
>> virtuoso
```

For above commands see the following figure. 5.

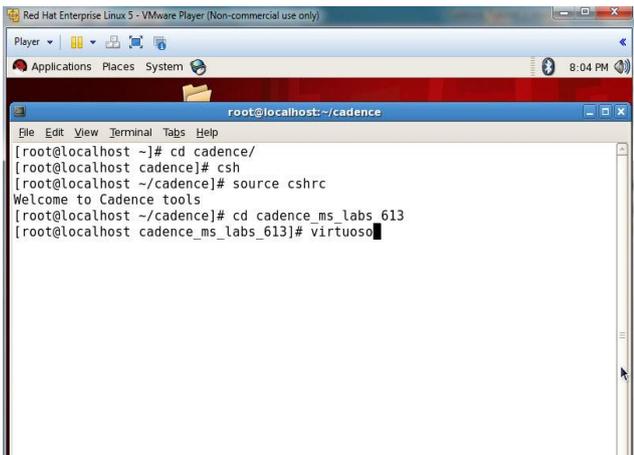


Fig. 5 Terminal window

Then first Cadence will start with a command and within few seconds should get a window like “Virtuoso@ 6.1.5”, also called Command Interpreter Window (CIW) as below: Figure 6.

Now create a new library from the **Virtuoso (Figure 6) CIW**

Then Go to the **File ---> New ---> Library** from the File menu. Will see a “New Library” window (Figure 7). In dialog window create new library name as (e.g. CMOSInverter) .Then select “**Attach to existing tech library**” and double click on OK.

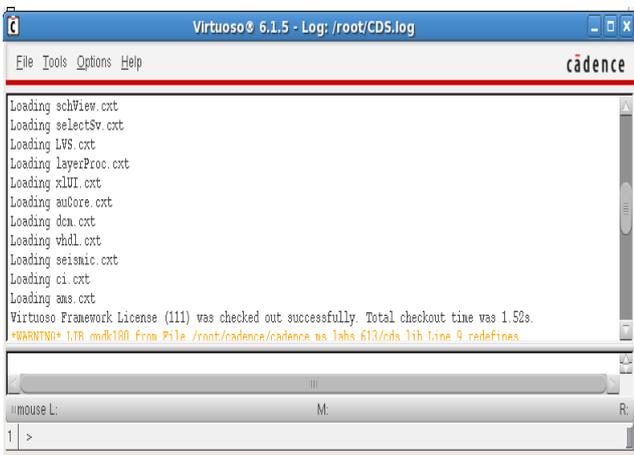


Fig. 6 Cadence virtuoso (CIW) window

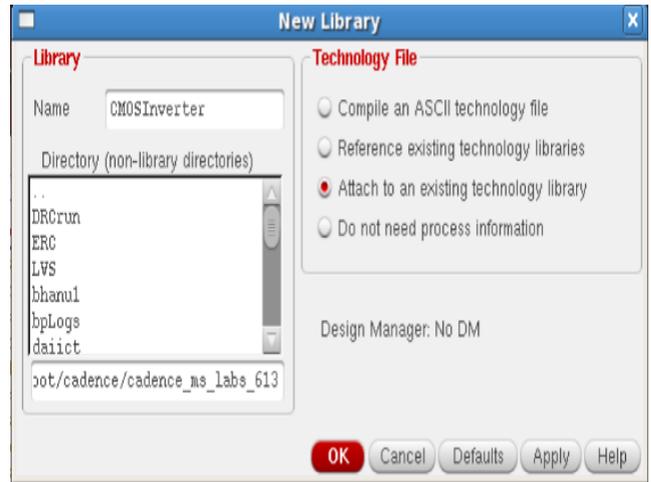


Fig. 7 New Library Window

By using Library Manager performs the above steps. Then after start the Cadence and will get one window like “Virtuoso CIW”, then go to **Tools--->Library Manager** or press **F6 button** on keyboard.

First open the Library Manager window (Figure 8). Then create one new library (CMOSInverter) from the Library Manager. Then “CMOSInverter” library will appear in the Library Manager window.

A. SCHEMATIC CAPTURE

From the **Virtuoso CIW** window first go to the **File ---> New ---> Cell View**. Then get one window like “Create New file” (Figure 7). In the dialogue window fill the information as below and press OK button.

Library Name: CMOSInvcircuit
Cell Name: myinvcircuit View Name: Schematic
Tool: Composer-schematic

“Then one window of schematic will appear. Then will get one “Virtuoso Schematic Editing” window.

Start the first schematic to create the CMOS Inverter circuit. If it is necessary then elaborate the editor window of Virtuoso Schematic. Next place the NMOS and PMOS transistors on the schematic editor window. Then the schematic design process over.



Fig 8 Create New File window

B. Placing Instances:

First click on “Instance” button on the left this will pop-up window an “Add Instance” window. Next browse for the window called “Library Browser – Add Instance” will pop up. Next select and place one PMOS transistor on the Virtuoso Schematic window.

The following steps will represents creation in Library Browser window.

Library =>gangayadav
 Cell => pmos
 View => symbol

Next modify the following properties of *pmos* in “Add instance” as given here.

Names => M1
 Width =>800 nm
 Length => 180 nm

Similarly, for placing of nmos transistor follow same steps above mentioned.

Library =>gangayadav
 Cell => nmos
 View => symbol

C. Connecting Wires:

For connecting of wires, first click on the button “Wire (narrow)” on the left side of the screen. Then appears an “add Wire” window. Select the colour whatever want to do. Next go to the title bar then activate Virtuoso Schematic Editor Window. Rotate the mouse over then it snaps the wires for connecting in between little diamond-shapes displaying by the nodes. Next represent the all wires in the same manner. After completion of connecting wires press the ESC button. For deleting unwanted wires if connected accidentally, choose the wire with left mouse click then press delete button of keyboard.

D. Adding Pins:

Next for adding *input* and *output* pins, press on “Pin” icon at lower left corner. Then “Add Pin” will appears. Next under Pin type name as *Vin*. And it is shown below (Figure 9).

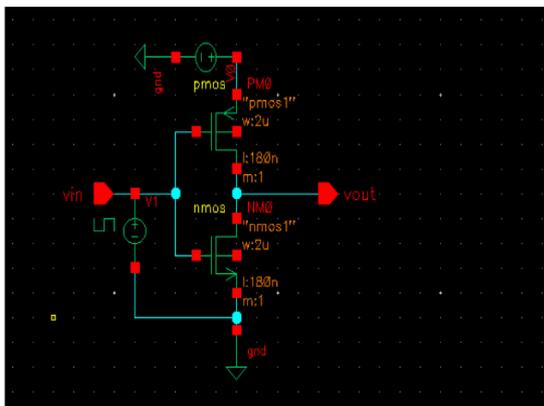


Fig 9 CMOS with pin, gnd and supply (Vdd)

E. Check and Save your design:

For saving of design follow the following steps. First press on the top left button or go to Design -> Check and save. First check the “Virtuoso” CIW window whether it having any errors or warnings, if it have any errors or warnings next to go back and first rectify them.

F. Simulation of the CMOS Inverter:

In the Virtuoso Schematic window go to launch _ ADE L Then will get the simulation window or ADE pop-up window

Next have to select the type of simulation. From “Virtuoso Analog Artist”. Then first go to Analyses ---> Choose. If selected a transient analysis. Then type the 200ps as stop time for transient analysis. Then select OK.

VI. RESULTS

The simulation results of 6T Static RAM without and with ROFs shown in below. The comparison analysis of area, power, current, delay of 6T Static RAM with and without ROFs circuit given in below tables 1,2&3. The results of 6T Static RAM described that ROFs changes the circuit operation and changes these all below mentioned parameters.

A. Power Analysis:

The calculated power given in table.1. Table 1 shows the power values of 6T SRAM with and without ROFs. If performing either read or write operation in 6T SRAM circuit represented in manner of charging and discharging to Vdd at bit lines BL and BL_bar nodes. If ROFs induced somewhere in this circuit that degrades the charging and discharging operations. So, delay fault induces. Due to this delay fault the required power also increases and it is given in below table.

Table.1. Power

Circuits	Power (uW)
6T-SRAM-ROF - Read	43.805
6T-SRAM - Read	10.508
6T-SRAM-ROF - write	68.022
6T-SRAM - write	75.588

B. Current Analysis:

The calculated current given in table.2. The ROFs degrades the conductivity and drives the low current at output node. In this below table gives the comparison of current value of the 6T SRAM with and without ROFs.

Table.2. Current

Circuits	Current (uA)
6T-SRAM-ROF - Read	48.672
6T-SRAM - Read	11.676
6T-SRAM-ROF - write	27.957
6T-SRAM - write	31.0636

C. Delay Analysis:

The Resistive Open Faults degrades the conductivity. Due to this causes delay fault. The delay [8] of the inverter chain, 7T SRAM with and without resistor given in below table.3.

Table.3. Delay

Circuits	Delay (nS)
6T-SRAM-ROF - Read	0.4
6T-SRAM - Read	0.1
6T-SRAM-ROF - write	0.1
6T-SRAM - write	0.06

M.Tulio Martins [12] developed 65nm 6T SRAM. Described NBTI impact on 6T SRAM with ROFs. Explained about only weak ROFs in aging of SRAM. Luigi Dilillo [13] designed embedded SRAM explained about address decoder ROFs in SRAM. Mentioned placing resistor in circuit and analysed the operation. But circuit less sensitive to resistive defects placed on the gate node. Subhashree Rath [14] also given delay of 45nm 6T SRAM and value is 0.6 ns. Jennifer Eunice.R [15] designed 6T SRAM & 7T SRAM using DSCH and layouts drawn using MICROWIND. In this paper given only power dissipation analysis.

The 6T Static RAM circuit diagrams with and without ROFs are given in below figure 10, figure 11. Designed by Cadence tool. The output waveforms of 6T Static RAM read operation with and without ROFs are given in below figure 12, figure 13. The waveforms of 6T Static RAM write operation with and without ROFs given in below figure 14, figure 15.

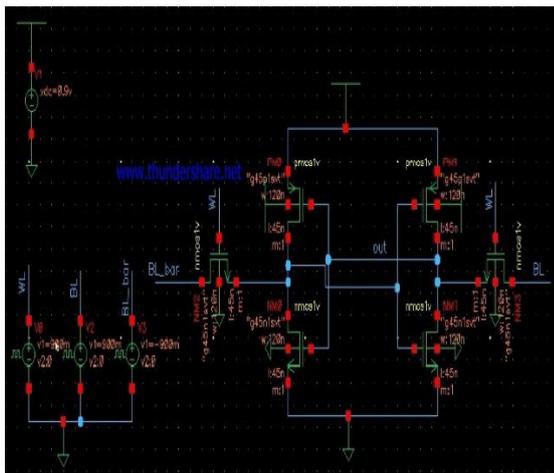


Fig.10. 6T SRAM

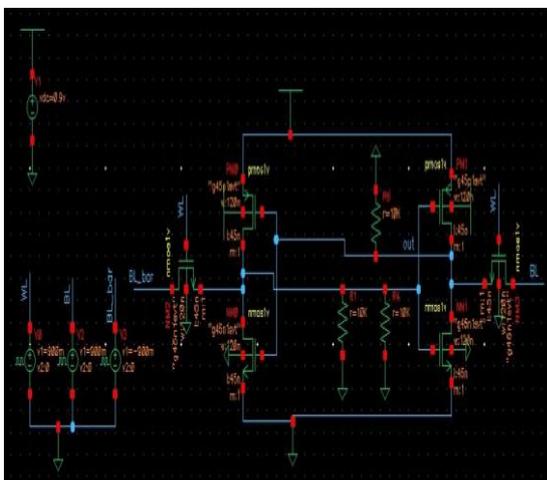


Fig.11. 6T SRAM with ROFs

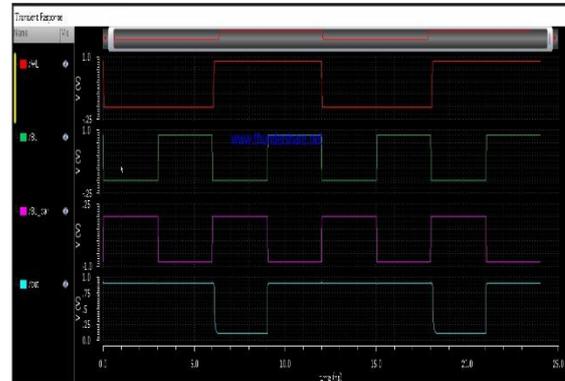


Fig.12. Waveform of 6T Static RAM Read Operation

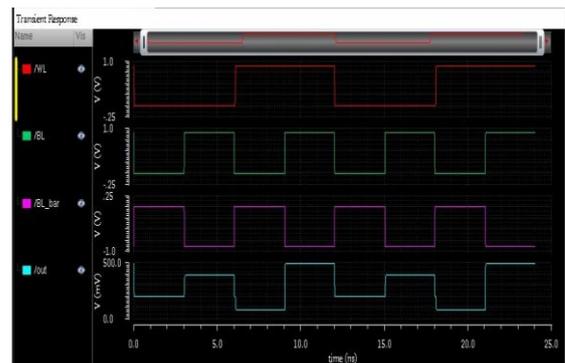


Fig.13. Waveform of 6T Static RAM Read Operation with ROFs

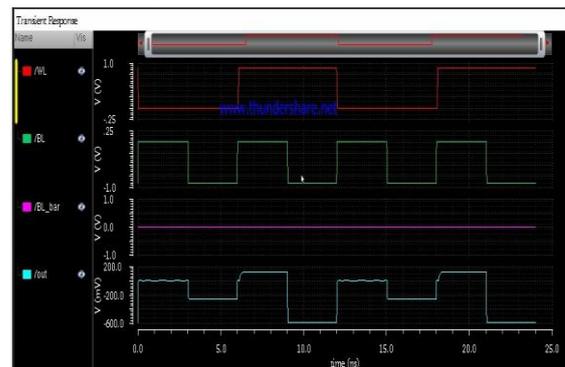


Fig.14. Write Operation waveform of 6T Static RAM

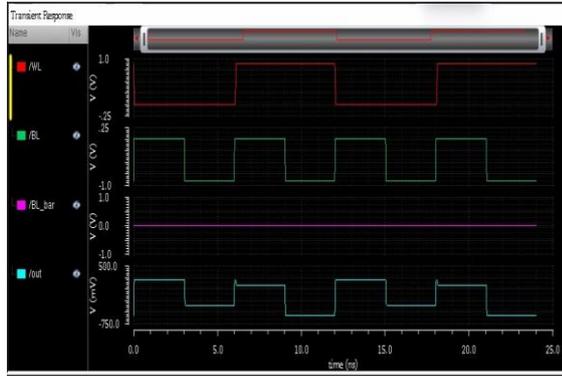


Fig.15. Write Operation Waveform of 6T Static RAM with ROFs

VII. CONCLUSION

During the fabrication of Integrated Circuits majorly induce ROFs, Due to this degradation present in the conduction and cause delay faults. This work describes the effects of ROFs on the 6T SRAM circuit operation. This proposed work given the analysis of 45nm 6T SRAM operation without ROFs and with ROFs. The ROFs reduce the conductivity in the circuit. So, drive low currents and increase the delay in 6T SRAM if performing either read or write operations.

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