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Reduction of Current Harmonics by Cascaded Multilevel Inverter based Shunt Active Power Filters

R. Sheba Rani, C. Srinivasa Rao, M. Vijaya Kumar

***Abstract*: Majority of loads in use today are power electronics based non-linear devices. Despite being compact and providing low energy consumption these loads generate inherent harmonics. Harmonics have several adverse effects such as interference with the communication lines, incorrect meter readings, increased losses, increased heating of electrical and sensitive electronic equipment. Sophisticated power electronic converter based filters named as Shunt Active Power Filters (SAPF) are widely being employed that provide superior harmonic filtering capabilities. Basic objective of SAPF is to generate or absorb currents that compensate harmonic currents produced by non- linear loads. These currents should be opposite in phase but have equivalent magnitude as that of harmonic currents. As compared to Diode-Clamped and Flying capacitor multilevel inverters, Cascaded multilevel configuration is employed for many applications due to ease of control and simple structure.**

In this research paper, power quality in a three-phase three-wire system is improved by reducing source side current harmonics produced by a non-linear load. Initially a three-level Cascaded multilevel inverter based SAPF is developed and its performance is analyzed by using advanced Adaptive Neuro Fuzzy Inference System (ANFIS) controller. DC link capacitor voltage and percentage Total Harmonic Distortion (%THD) in source currents is measured at PCC for balanced loading conditions and results are compared. In this paper, it is also proposed to incorporate multilevel inverter topology concepts by employing Five-Level and Seven-Level Cascaded Multilevel Inverters as VSI circuit for SAPF. Performance of these multilevel Shunt Active power filters is analyzed by ANFIS controller. Instantaneous Active-Reactive power theory is implemented to compute reference compensating currents for all Shunt Active power filter models. Phase Disposition type Pulse Width modulation is chosen for generating gate pulses for VSI circuits of all Cascaded multilevel inverter configurations. Three-level, Five-level and Seven-level Shunt active power filter models are developed and simulated using MATLAB/ Simulink and results are presented.

Keywords* : *Adaptive Neuro Fuzzy Inference System (ANFIS), Cascaded Multilevel Inverter (CMLI), Fuzzy inference system (FIS), Level Shifted Pulse Width Modulation (LSPWM), Percentage Total Harmonic Distortion (%THD), Phase Disposition PWM (PDPWM), Point of Common Coupling (PCC), Shunt Active Power Filter (SAPF).

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I. INTRODUCTION

Harmonics are referred to as voltages or currents that have frequencies (usually integer multiples) higher than the standard 50 Hertz design frequency of an electrical system. Harmonics when left unidentified may cause severe consequences such as total damage to consumer equipment.

Passive filters are a traditional approach to eliminate harmonics. Shunt passive filter also referred to as notch filter is the most economical type of all passive filters [1]. Usage of series passive filters is limited as they are tuned to eliminate harmonics of only one particular frequency. Hence separate series filters need to be designed for each harmonic to be filtered out. Other configurations such as First-order, second-order and third-order high pass filters were also developed. These filters are not widely used due to high cost and low reliability. Application of passive filters is restricted in varying load conditions due to their incapability to provide necessary compensation. In spite of extensive research, usage of passive filters has become obsolete due to their shortcomings. Passive filers cause resonance with the line impedance in the system where they are placed. Thus stability of the system is reduced. Computation of tuning frequency is difficult and any small discrepancy may result in inaccurate tuning frequency value [2]. Owing to limitations of passive filters, active filtering technique was introduced and widely implemented.

The concept of active filtering has been subjected to extensive research for past three decades. The idea of active power filtering for mitigating current harmonics was proposed by Sasaki and Machida in 1971 [3]. For effective harmonic filtering by an active power filter, choice of a suitable control technique, inverter configuration and relevant pulse width modulation technique plays a significant role. Harmonic extraction methods are broadly classified into Frequency domain and Time domain methods. Several time domain methods were proposed for estimating reference currents such that instantaneous compensation may be provided for current or voltage harmonics present in a system. Time domain methods are advantageous for online applications where compensation should be provided very quickly. PQ theory was first proposed by Akagi, Nabae and Kanazawa. This method is also named as Instantaneous Reactive Power theory (IRP).

This technique was employed for control of APFs and power line conditioners for the purpose of instantaneous harmonic mitigation. This method is quite simple as it involves simple calculations and hence is easy to implement [4].

Synchronous detection theorem was then introduced that allowed estimation of reference currents and voltages under non-sinusoidal and unbalanced conditions. This method was similar to PQ theory and is based on the assumption that after harmonic compensation three-phase source voltages remain balanced which is not true practically. Then this theory was modified and employed for an APF for varying load conditions [5]. Suitability of this method for three-phase systems alone and impact of voltage harmonics on compensation capability of APF has limited its applications.

Synchronous reference frame method was introduced that involves load current transformation into AC and DC quantities [6]. Filtering of DC quantities may result in a delay. Though this method may give good results, it cannot be used for systems with unbalanced supply voltages. Among all the control techniques discussed, PQ theory is simple to implement and exhibits good steady state behavior. In this research PQ theory is implemented for a three-phase three-wire system.

Power circuit of APF requires an AC-DC inverter and a coupling inductor or a balancing capacitor for connecting APF to the power system. Depending on the type of application for which APF is employed, power converters used in power circuits may be either a Voltage Source inverter (VSI) or a Current Source inverter (CSI). For many industrial and commercial facilities these VSIs are widely employed. Initially two-level VSIs were used for active filtering applications. In medium and high voltage systems, applications of these two- level APFs are limited due to power losses, switching noise, interference with communication systems etc. For high voltage systems, mostly 6-pulse or 12-pulse inverter circuits were in use for harmonic filtering and reactive power compensation [7]. These inverters required zigzag transformers additionally by means of which they are connected to the power system which increased total cost of the system. Transformers occupied larger space, produced losses and over voltages due to saturation.

Multilevel inverters seemed to be a possible solution for active filtering in high voltage systems [8]. Main objective of these devices is to synthesize the desired output voltage from several levels of DC input voltage. These inverters do not require a coupling transformer and the presence of high switching devices makes the circuit compact. Hence these inverters are of low cost and occupy less space. As compared to conventional two-level Voltage Source inverters, multilevel inverters are known for many advantages some of which include low harmonic distortion, less switching and conduction losses.

A Neutral Point clamped inverter also named as Diode Clamped inverter was introduced by Akira Nabae, Isao Takahashi and Hirofumi Akagi in 1981 for variable speed drive system. Later this configuration was modified and extended for higher number of levels such that it is compatible for high-power medium-voltage applications [9]. It has been observed that application of Diode Clamped inverter is restricted to fewer output voltage levels. Switching device should be able to block a voltage of $V_{dc}/(m-1)$, where m is number of levels and reverse blocking capability of clamping diodes should be equal to the level in which clamping is performed. This procedure additionally requires series connected diodes that increase the number of components, price and control complications.

Clamping diodes were replaced with capacitors thus resulting in a different topology named as Flying Capacitor multilevel inverter. This topology was presented by Meynard and Foch [10]. Redundant states were considered for balancing flying capacitor voltages to the required output voltage level by using two or more suitable switching combinations. Flying capacitors required additional capacitors for equal sharing of voltages due to which control of this inverter has become difficult.

Next multilevel inverter topology introduced was Cascaded H-Bridge Inverter which comprised of single phase H-Bridge units each supplied by a separate DC voltage source. A comparison of all three topologies i.e. Diode Clamped, Flying Capacitor and Cascaded H-bridge inverters were compared with respect to the number of components required is discussed. Number of components required for any level is comparatively less in CMLI as compared to DCMLI and FCMLI [11].

Main factors that define a modulation technique are its ability to reduce harmonics, achieving proper balance of DC voltage and reduction of common-mode voltage. Multilevel PWM techniques are widely used for the control of Cascaded multilevel inverters. Multilevel PWM techniques employ several triangular carrier waves that are modulated either with respect to the angle or shifted to different levels with respect to the zero reference. Based on these factors, multilevel PWM techniques are classified as Phase Shifted PWM and Level Shifted PWM. Level Shifted PWM was initially employed for the control of Neutral Point Clamped inverters and later used for control of Cascaded multilevel inverters. Phase Shifted PWM techniques are widely used for control of Flying Capacitor and Cascaded H-Bridge inverters.

In Level-shifted PWM (LSPWM) method, m-1 carrier waves are required that are shifted with respect to a reference. In LSPWM, each carrier wave is associated with two voltage levels. Different types of LSPWM methods such as PDPWM, PODPWM and APODPWM were introduced based on phase displacement with level shifted carrier waves. PDPWM involves all carrier waves to be level shifted with respect to each other with no phase displacement. PODPWM involves all positive carriers to be in opposite phase with negative carriers with respect to the reference. APODPWM involves alternate carriers to be in opposite phase with respect to each other. Different types of carrier based PWM techniques and phase shifted PWM techniques were compared and presented by Agelidis.V. et.al [12].

It has been observed that when LSPWM techniques were applied for the control of three phase inverter, PDPWM is more reliable and harmonics have been reduced to a very low value as compared to other methods [13]. For multilevel inverter control, as number of output voltage levels increase, increase in harmonic reduction may be observed when PDPWM method is implemented.

For SAPF to operate efficiently, it is necessary to maintain a constant DC link capacitor voltage. Conventional method of controlling DC link voltage includes using a PI controller that is used to process the steady state error.

A PI controller was employed for mitigation of harmonics and reactive power compensation such that improvement in transient behavior of a SAPF may be observed. PI control has been in use widely due to its simple and effective control.

But PI controller will be subjected to dynamic interaction between active and reactive power flows and it is sensitive to parameter variations and other unbalances occurring in a system and needs a linear mathematical model [14].

Intelligent controllers were designed for control of DC voltage in a SAPF. Fuzzy Logic Controller is a significant choice for the control of non-linear systems due to its ability to handle inaccurate information in an efficient way [15]. Further it was proved analytically that when a non-linear Defuzzification method is adopted for a Fuzzy logic control, it is equivalent to a non-linear controller. This provided a way for the usage of Fuzzy logic control in applications such as motor drive controls and active power filters.

Mamdani and Takagi Sugeno types of FLC controllers were employed for control of SAPF and its performance was observed and compared to that of a conventional PI controller. As compared to Mamdani type FLC, Takagi Sugeno FLC required fewer fuzzy sets and rules and took less computational time. Due to these advantages it exhibited good response when compared to conventional PI controller and Mamdani type FLC [16]. An APF was designed for a three-phase four wire system based on i_d-i_q approach by Suresh Mikkili and Anup Kumar Panda. Effectiveness of SAPF for harmonic current filtering was investigated using PI and Fuzzy Logic controllers. Fuzzy Logic controller based SAPF exhibited better performance than PI based SAPF [17].

Formation of rule base for a Fuzzy Logic controller was complicated which led to development of a simple intelligent controller known as ANFIS controller. ANFIS structure is a combination of Fuzzy and Neural Networks. Thus this controller includes advantages of both FLC and NN controllers and provides better performance with no time delay. ANFIS structure has been widely employed for modelling non-linear systems and for identification of non-linear components in a control system [18].

This paper initially presents implementation of a three-level CMLI based SAPF for harmonic mitigation. Control of this SAPF is based on PQ theory and LSPWM method is implemented for generation of switching pulses for CMLI. ANFIS controller is developed for processing the error of DC link voltage. Learning method implemented in this system is a fusion of Back Propagation Algorithm (BPA) and Least Square Estimation (LSE) method which is used to train a 5-layer ANFIS controller. Performance of three- level CMLI based SAPF is observed for balanced non- linear load and simulation results are presented. Also five- level and seven-level CMLI based SAPFs are also developed and their effectiveness in reducing current harmonics at PCC is observed and simulation results are presented. Simulation work is carried on MATLAB/ Simulink platform.

a) Introduction to SAPF

A SAPF continuously tracks harmonic currents and generates compensating currents by means of a control algorithm. These filters have wide real time applications as these devices respond very quickly to the load changes and produce suitable compensating currents. Thus a SAPF exhibits high adaptability in compensating harmonic currents of a chosen non-linear load. A simplified block diagram of a three-phase CMLI based SAPF and controlled by PQ theory based control algorithm is shown in Fig 1.

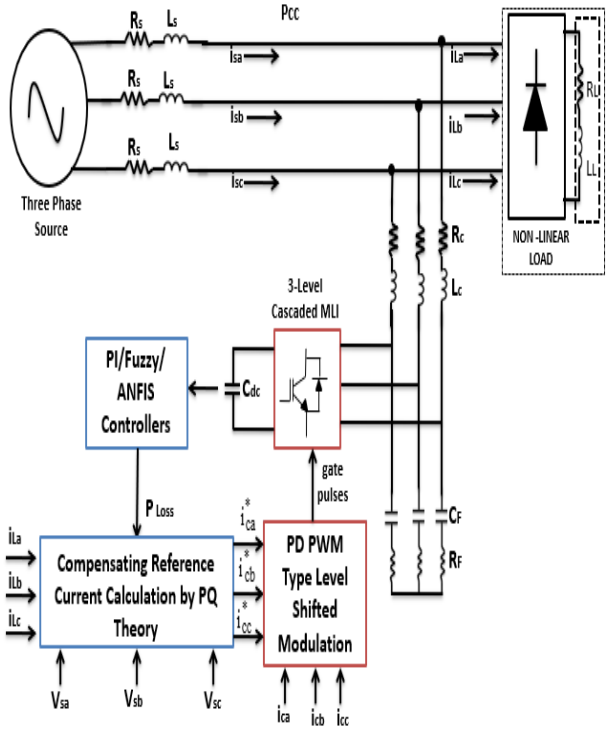

Fig. 1 Control circuit of Three-Level CMLI based SAPF

Performance of SAPF is mainly dependent on its control circuit. SAPF performs following operations.

1. Generation of switching pulses for Cascaded Multilevel Inverter by using PWM methods.
2. Extraction of compensation reference currents by PQ method.
3. DC voltage control by means of suitable current controller.

II. CMLI FOR SAPF

Cascaded Multilevel Inverters are found to be more beneficial than their counterparts in terms of device count, price and ease of control. This paper presents implementation of a CMLI for filtering harmonic currents at the source side in a three-phase three-wire system.

b) Three- Level CMLI Structure

SAPF offers a closed loop operation by detecting the changes in load currents (i_L) continuously and generating corresponding reference compensating current signals (i_c^*) required for harmonic current compensation at source side. Thus compensating currents (i_c) continuously track the calculated reference compensating currents (i_c^*) required for compensation. Block diagram of three-level CMLI employed for SAPF is shown in Fig. 2.

Three- Level Cascaded Inverter structure comprises of one H-bridge unit for each phase as shown in Fig. 2. Each H-bridge structure has 4 IGBT switches, 4 freewheeling diodes and a DC source.

This inverter structure generates 3 levels of output voltages ($-V_{dc}$, 0 , $+V_{dc}$) for different switch combinations. In general, for CMLI topology, if 'n' is number of DC voltage sources, then number of output voltage levels 'm' is given by m= 2n+1.

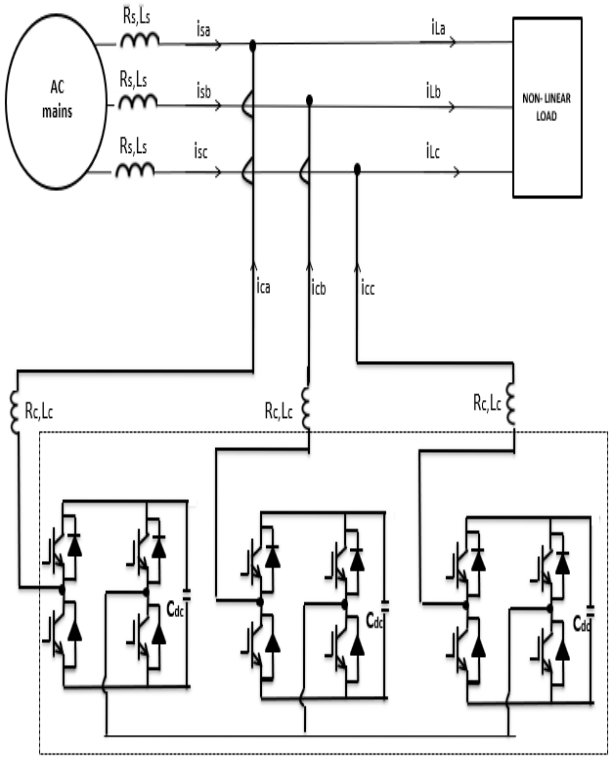

Fig. 2 Block diagram of Three-Level Cascaded MLI employed for Active Filtering Application in a Three-phase Three- wire System

a) Five-Level CMLI Structure

A single-phase Five-Level CMLI cell is realized by cascading 2 three -level full- bridge units. If 'm' is number of levels of output voltage, number of DC sources (or number of H-Bridges) required, 's' is given by

$$S = \frac{m-1}{2} \quad (1)$$

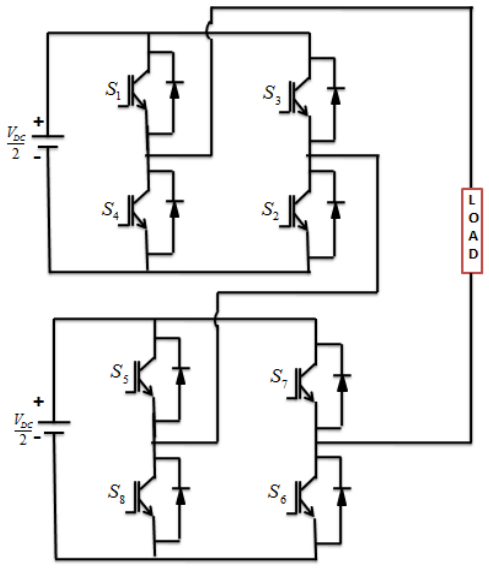

Fig. 3 Single-Phase Five-Level CMLI Structure

Thus for a Five-level CMLI, 2 DC sources are required for each phase as shown in Fig.3 Five levels of output voltages obtained at the output of this inverter are $V_{dc}, \frac{V_{dc}}{2}, 0, -\frac{V_{dc}}{2}, -V_{dc}$.

b) Seven-Level CMLI Structure

Structure of Seven-Level CMLI for single-phase system is shown in Fig. 4. Each phase comprises of three H-bridge units cascaded as shown in Fig. 4.

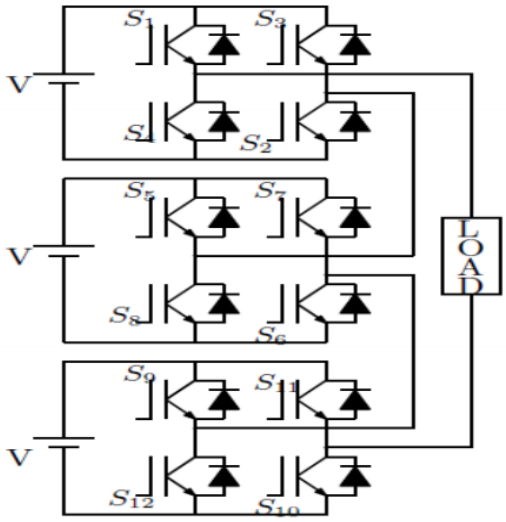

Fig. 4 Structure of a Single- phase Seven-Level CMLI

Each H-bridge unit made up of 4 IGBT switches requires an independent DC source. Thus for obtaining a seven- level voltage, three H-bridges are required for each phase. A total of 12 IGBT switches and 3 DC sources are needed per phase as shown in Fig. 4.

c) Generation of Switching Pulses for CMLI in a SAPF

LSPWM technique is commonly employed in Cascaded H- Bridge inverter as it is simple and can be effectively implemented to obtain higher levels of output voltage. This technique is also known for even distribution of power among individual H-bridge cells in an inverter.

In LSPWM, number of carrier signals needed for N-level inverter is N-1. So in order to employ LSPWM for a three-level CMLI, number of carrier waves required is '2'. These signals should have equal frequency and equal amplitude. A comparator compares carrier signals with modulating signal and a pulse is generated at the instant where magnitude of modulating signal is higher than carrier signal. LSPWM technique is sub-classified into three types- Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD).

PD type LSPWM modulation is more reliable and reduces harmonics to a much lesser extent as compared to other modulation techniques. Hence PDPWM is implemented for three- level, Five- level and Seven- level CMLIs which are used as VSIs in a SAPF. After reference compensating currents have been computed, these signals are compared with their corresponding actual currents. Errors thus obtained are compared with triangular carriers as a result of which gate signals required for CMLI are obtained.

d) Extraction of Compensation Reference Currents by Employing PQ Theory

Many methods were developed for computing reference currents needed for compensation, but PQ method is often used. Procedural steps followed in PQ theory for deriving reference currents are depicted in Fig 5. Voltages at source side and load currents are sensed and converted into α-β-0 reference frame by Clarke's transformation.

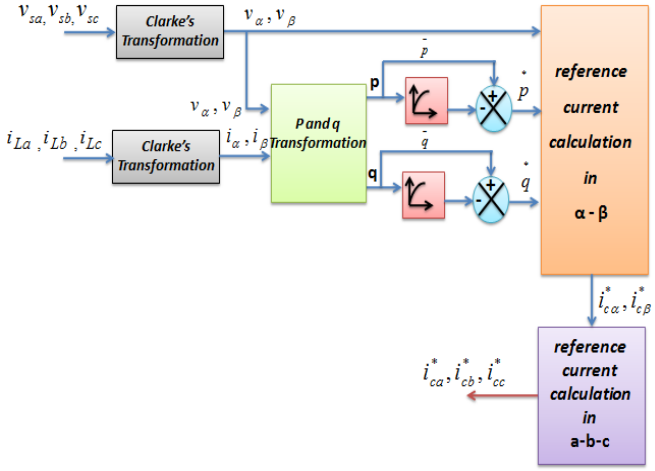

Fig. 5 Derivation of Reference Currents using PQ Theory

Instantaneous active power is comprised of fundamental current and voltage and termed as direct component. Similarly, instantaneous reactive power comprises of current and voltage harmonic components and is termed as alternating component. By means of simple algebraic computations reference currents are obtained in α-β frame which are transformed into a-b-c coordinates by inverse Clarke's transformation [19].

e) DC Link Voltage Control by ANFIS Controller

ANFIS is similar to Fuzzy inference systems (FIS). For active filtering application, ANFIS controller is used to reduce error between actual voltage and reference voltage of DC capacitor [20]. Capacitor voltage must remain constant which helps in generating accurate reference compensating current signals by SAPF.

➢ **Structure of ANFIS**

General architecture of two inputs – One output ANFIS structure is depicted in Fig.6. It comprises of five layers. Data processing steps involved in ANFIS are as follows:

Step 1: Inputs X_1, X_2 expressed as triangular membership functions are chosen in first layer. Node function with respect to each node 'i' is given by

$$O_i^1 = \mu_{Ai}(x) \quad (2)$$

where input to the node is given as 'x',
linguistic variable related to node function is Ai and Membership function of A_i is given by μ_{Ai}.

Step 2: In layer 2, the nodes are fixed. The computation of firing strength w_i for each rule is carried out by the nodes. Output of each node is as expressed below.

$$O_i^2 = \omega_i = \mu_{Ai}(x) x\, \mu_{Bi}(y) \quad i = 1, 2 \quad (3)$$

As per equation (3), output is obtained by multiplying every signal entering at that node.

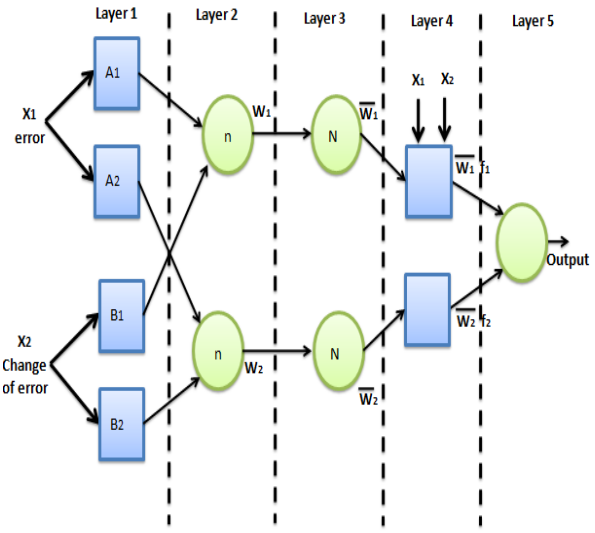

Fig. 6 Structure of Artificial Neuro Fuzzy Inference System

Step 3: In this layer also, nodes are fixed. Considering the assumption that number of layers is equal to fuzzy rules, normalized weights are computed in layer 3. Process includes computation of ratio of i^{th} rule's firing strength with respect to sum of firing strengths of all the rules. Output from i^{th} node is the normalized firing strength given by,

$$O_i^3 = \overline{\omega_i} = \frac{\omega_i}{\omega_1 + \omega_2} \quad i = 1, 2 \quad (4)$$

Step 4: Node function is expressed as

$$O_i^4 = \overline{\omega_i} f_i = \overline{\omega_i}(p_i x + q_i y + r_i \quad i = 1, 2 \quad (5)$$

where w_i is output of Layer 3 and $\{p_i, q_i, r_i\}$ is the consequent parameter set. Defuzzification is carried out in layer 4. A set of Neuro- Fuzzy parameters are obtained by Fuzzy Singletons that are indicated by weighted connections between Rule Layer and Defuzzification Layer.

Step 5: This layer has only one fixed node. Outputs obtained from layer 4 are accepted and are summed up and finally transformed into crisp sets. Output thus obtained is expressed as

$$O_i^5 = \sum \overline{\omega_i} f_i = \frac{\sum_i \omega_i f_i}{\sum_i \omega_i} \quad (6)$$

➢ **DC Voltage Regulation in SAPF by ANFIS Controller**

Inputs to ANFIS controller are actual DC capacitor voltage and its reference value. Output obtained is peak value of current (I_{max}). Among different membership functions that are available, triangular membership functions are chosen. By choosing appropriate tolerance value and number of epochs, FIS is trained by clicking 'Train Now' button in the ANFIS editor tool. Tolerance of error is assumed to be 0.01. Total epochs chosen are 200. Output I_{max} thus obtained is multiplied with corresponding sine vectors. Thus the errors obtained by comparing compensating current and actual current are then sent for implementation of PDPWM such that gate pulses for VSI are generated.

III.RESULTS AND DISCUSSIONS

a) Simulation Results of Three-Phase CMLI based SAPF with ANFIS Controller

This section discusses implementation of ANFIS controller in MATLAB and also presents the corresponding simulink block diagrams, control circuits, relevant waveforms and Harmonic Spectra of source currents to observe the performance of SAPF for balanced load conditions.

Table 1 System Parameters Chosen for Simulation

AC supply voltage	110V (peak to peak)
Components of VSI	DC link Capacitor C_{dc} = 1650µF AC inductor = 2.5 mH, Switching frequency of the inverter = 12.5KHz Ripple filter components: C= 10 µF, R= 25Ω
PI controller parameters	K_p= 0.3 K_i= 1
Balanced Non-linear load	Diode Bridge rectifier with a resistor on DC side R_{dc}=20Ω

Control circuit for a three-level Cascaded SAPF model with ANFIS controller is represented in Fig. 7. Extraction of reference compensating currents, production of gating pulses for inverter circuit and DC link voltage regulation is depicted. Transformation of three phase source voltage and load current is carried out and instantaneous active, reactive and zero sequence powers are computed. All the powers obtained are segregated into DC and AC components. AC components are separated by a Butterworth low-pass filter. Reference compensating currents are computed and transformed into a-b-c components.

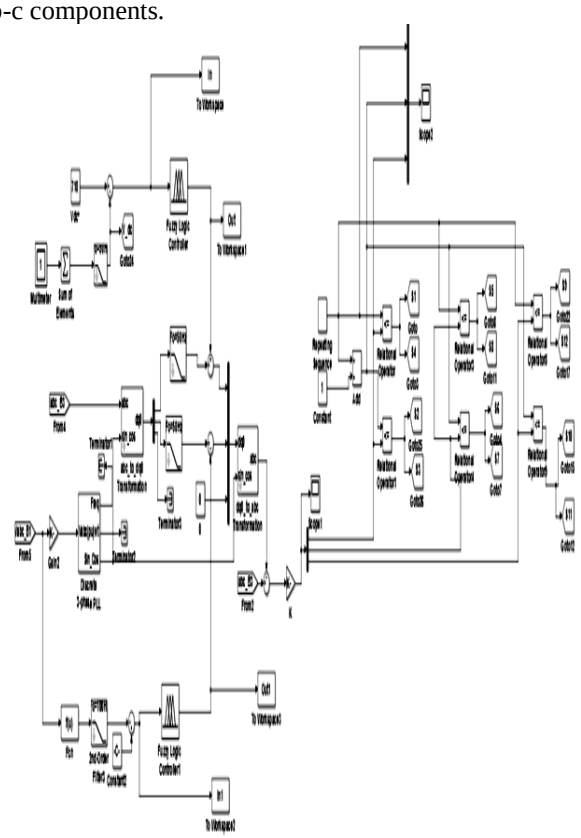

Fig. 7 ANFIS Control Circuit Employed for Three- Level CMLI based SAPF

Comparison of actual voltage (V_{dc}) with reference voltage (V_{dc}^*) is carried out by comparing and error obtained is fed to ANFIS controller. Control circuit also depicts generation of gating pulses using PDPWM method as shown in Fig.8.

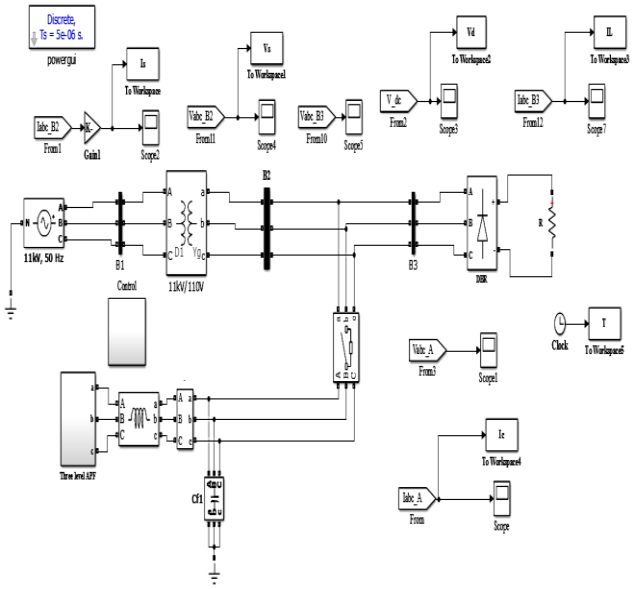

Fig. 8 Simulink Model of Three- Level CMLI based SAPF

In this section, simulation results are presented to that pertain to conventional Three-Level SAPF employing a CMLI in a three-wire system feeding a balanced non-linear load. Implementation of this conventional SAPF is investigated by employing PDPWM modulation for CMLI for generating gate pulses. DC voltage control is accomplished by employing ANFIS controller in the control circuit of SAPF. SAPF is connected to the system at t=0.1 seconds.

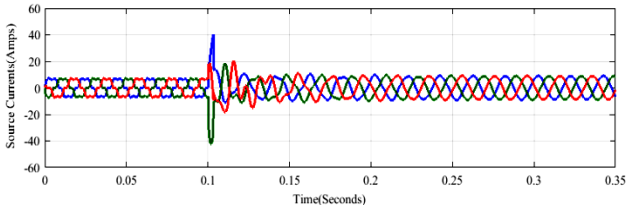

Fig.9 Waveform of Source Current

Currents at source side obtained are shown in Fig.9. Due to the presence of balanced non-linear load, source currents are distorted due to harmonics at source side. At t= 0.1 seconds, SAPF is connected to the system which performs harmonic filtering at source side. It can be observed that after t=0.15 sec source currents become sinusoidal.

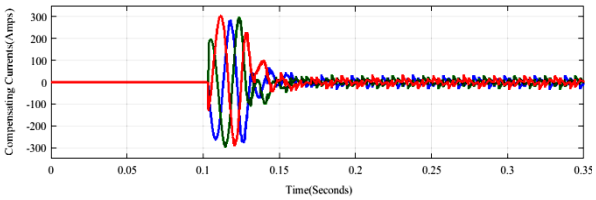

Fig.10 Waveform of Three- Phase Compensating Currents Generated by Conventional SAPF

Fig.10 shows three-phase compensating currents generated by conventional SAPF injected at PCC.

At t= 0.1 seconds as SAPF is connected, system is subjected to sudden changes and after a small delay required compensating currents are generated.

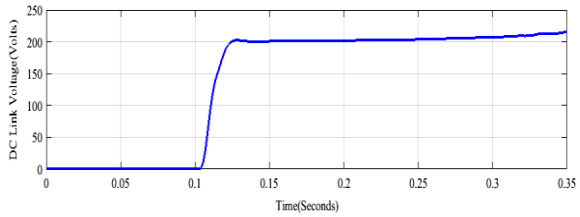

Fig.11 DC Link Voltage

A constant voltage of 200V is maintained across DC link as shown in Fig.11.

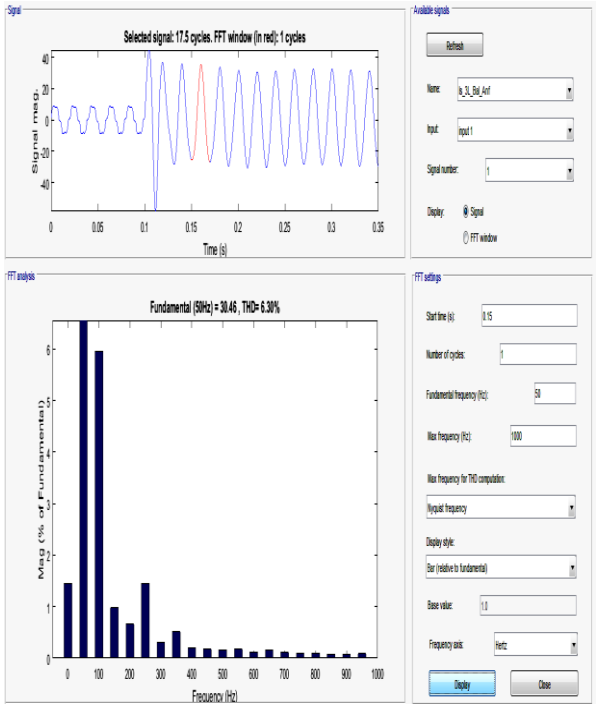

Fig. 12 %THD in current at source side of PCC after connecting SAPF

Fig.12 indicates that after compensation of harmonics at source side, %THD in source currents has been reduced to 6.30 % when load is balanced non-linear load.

b) Simulation Results of Five - Level CMLI based SAPF using ANFIS Controller for Balanced Non- Linear Load conditions.

Control circuit of Five-Level Cascaded SAPF model with ANFIS controller is represented in Fig. 13. Extraction of reference compensating currents, generation of gate pulses for the inverter circuit and regulation of DC link voltage is depicted. Control circuit depicts the generation of gating pulses using PD modulation. Control of SAPF by PQ theory is also depicted.

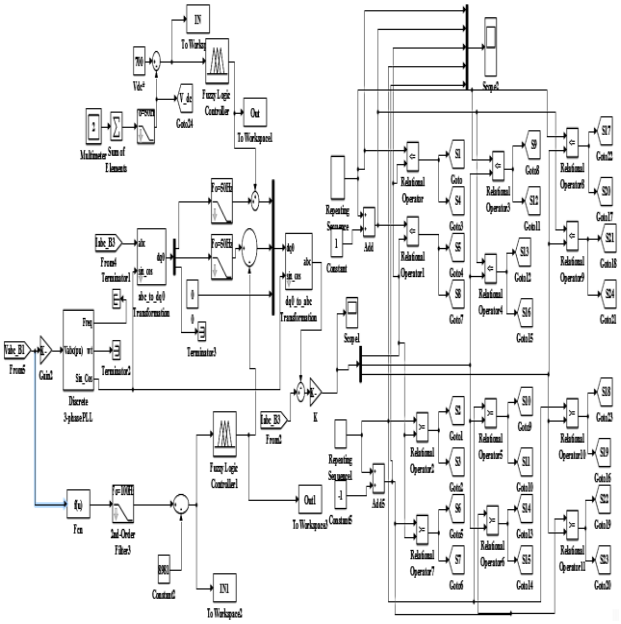

Fig. 13 Control Circuit of Five-Level Cascaded SAPF with ANFIS Controller

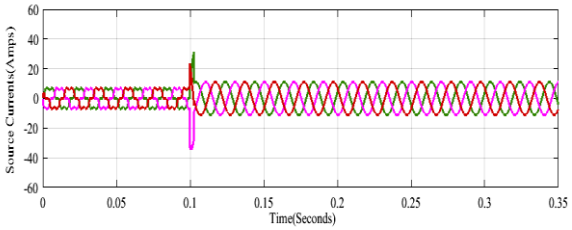

Fig. 14 Waveform of Three-Phase Source Currents

Currents at the source side of PCC are shown in Fig. 14. Due to the presence of balanced non-linear load, source currents are distorted due to harmonics at the source side. At t= 0.1 seconds, SAPF is connected to the system which performs harmonic filtering at source side. It can be observed that after t=0.15seconds, source currents become sinusoidal.

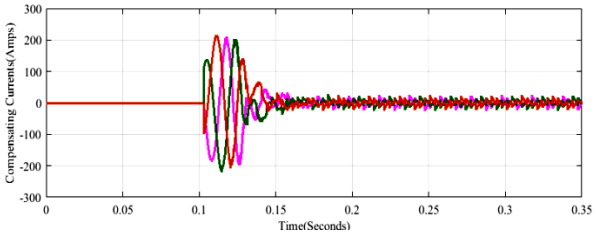

Fig. 15 Waveform of Three-Phase Compensating Currents Generated by

Five-Level CMLI based SAPF

Three-phase compensating currents generated by Five-Level CMLI based SAPF injected at PCC are as shown in Fig. 15. It is observed that for t= 0 to 0.1 seconds no compensating currents are generated since SAPF is not connected to the system. At t=0.1 seconds as SAPF is connected, the system is subjected to sudden changes and after a small delay required compensating currents are generated. After SAPF is connected to PCC of the system at t= 0.1 seconds, it is observed that DC link voltage is retained at exact steady state value of 200V as shown in Fig. 16.

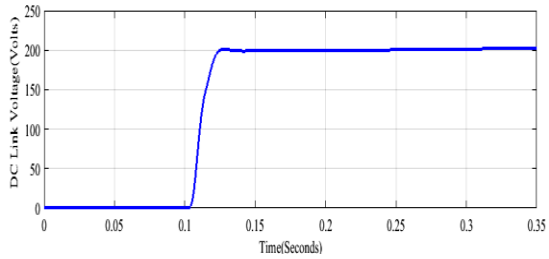

Fig. 16 DC Link Voltage

Triangular carrier waves being in phase and are level shifted at different voltage levels are as shown in Fig. 16. Four triangular carrier waves are required for Five-Level CMLI and these are compared with a sinusoidal wave as shown in Fig. 17. As a result gate pulses required to drive Five-Level CMLI are generated.

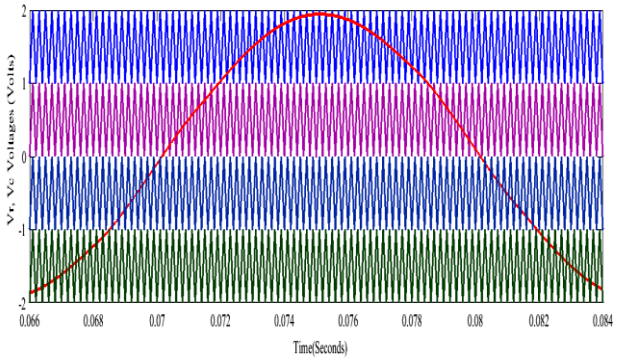

Fig. 17 PDPWM Method for Five-Level CMLI

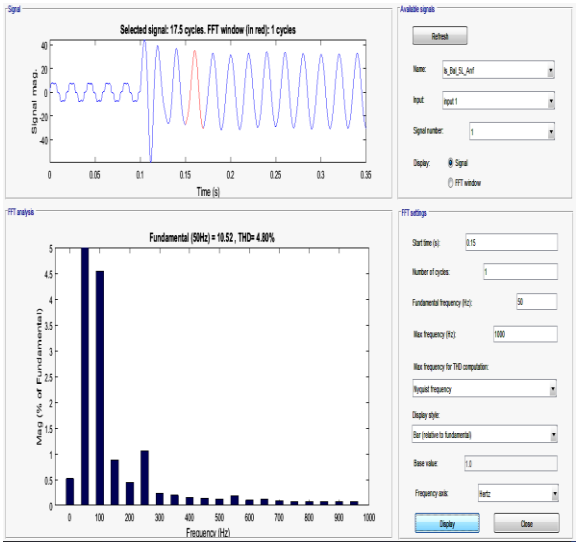

Fig. 18 %THD in current at source side of PCC after connecting SAPF

Percentage of harmonic content present in the source current is depicted in Fig. 18 which indicates that after compensation %THD in source currents has been reduced to 4.80% when load is a balanced non-linear load.

c) Simulation Results of Seven- Level CMLI based SAPF using ANFIS Controller for Balanced Non- Linear Load conditions.

Control circuit of Seven-Level Cascaded SAPF model with ANFIS controller is represented in Fig 19.

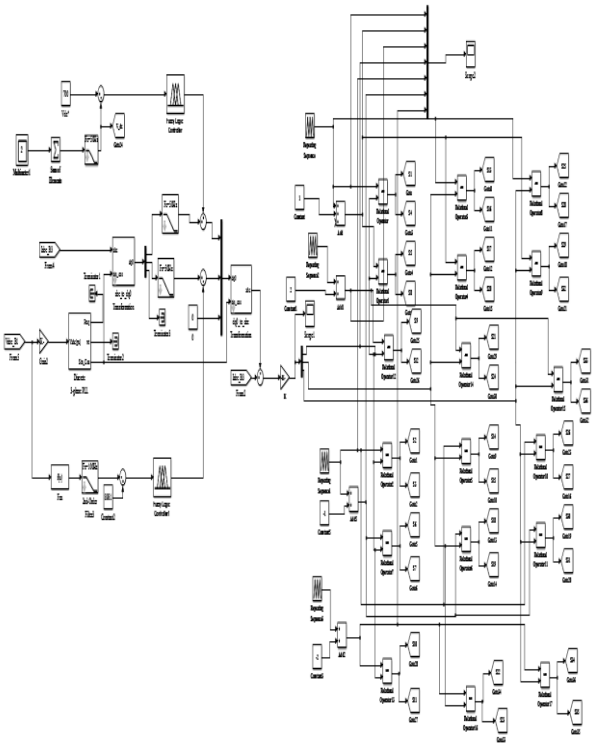

Fig. 19 Control circuit of Seven-Level Cascaded SAPF with ANFIS controller

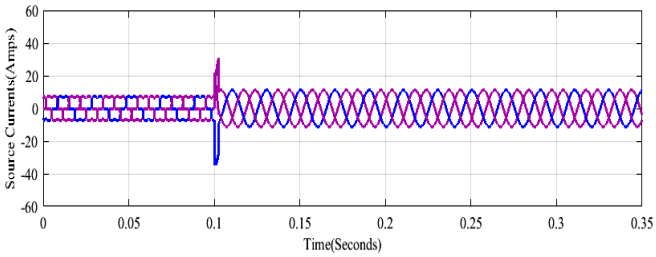

Fig. 20 Waveform of Source Currents

Currents obtained source side of PCC is shown in Fig.20. Due to the presence of balanced non-linear load, source currents are distorted due to harmonics at source side. At t= 0.1 seconds, SAPF is connected to the system which performs harmonic filtering at source side. It can be observed that after t=0.12 seconds, source currents become sinusoidal.

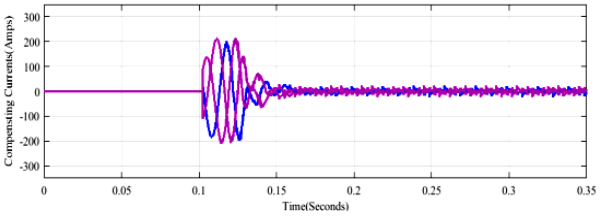

Fig. 21 Waveform of Three-Phase Compensating Currents Generated by Seven-Level CMLI based SAPF

Compensating currents generated by Seven- level CMLI based SAPF and injected at PCC are shown in Fig 21. At t=0.1 seconds as SAPF is connected, the system is subjected to sudden changes and after a small delay required compensating currents are generated.

Table 2 Comparison of %THD in Source Current at PCC in a Three-Phase Three- Wire System by Employing CMLI Based SAPF for Balanced Loading Conditions

Type of SAPF employing ANFIS Controller	% THD in source current after connecting multilevel CMLI based SAPF
Three-level SAPF	6.30 %
Five-level SAPF	4.80%
Seven-level SAPF	1.30%

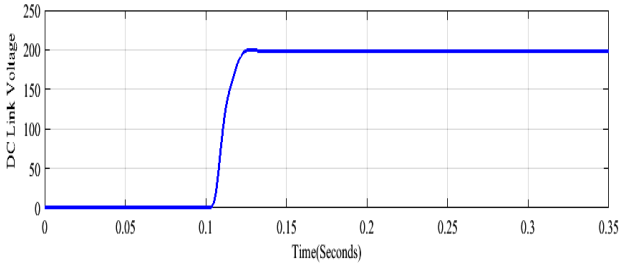

Fig. 22 DC link voltage waveform

After SAPF is connected to PCC of the system at t=0.1 seconds, it is observed that voltage of DC link is retained at exact steady state value of 200V as shown in Fig. 22.

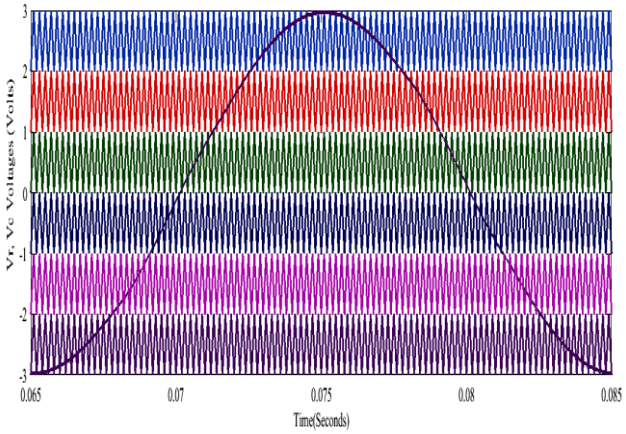

Fig. 23 Triangular Carrier Waves for PDPWM Modulation of Seven-Level CMLI

A total of six carrier waves required for seven- level CMLI are represented in Fig 23. All the carrier waves have equal amplitude and are in phase as shown in Fig 22. Comparison of carrier and reference waves will result in suitable gating pulses as required By Seven-Level CMLI.

Percentage of harmonics present in currents at source side of PCC is shown in Fig. 24 which indicates that after compensation of harmonics at the source side, %THD in source currents has been reduced to 1.30% when the load is balanced non-linear load.

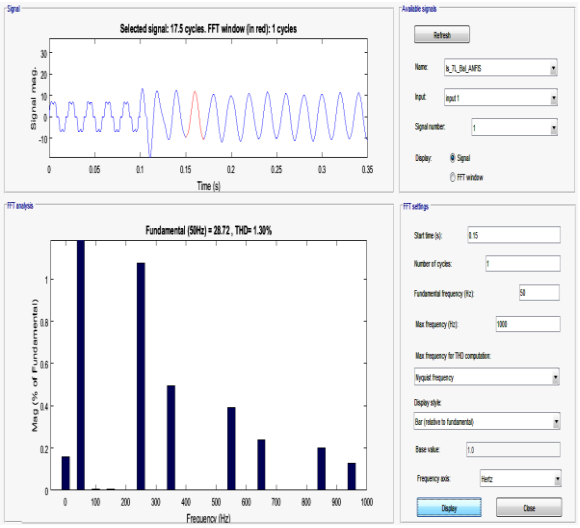

Fig. 24 THD in current at source side of PCC after connecting SAPF

IV. CONCLUSION

This paper discussed the performance of three- level, five-level and seven- level CMLI based SAPFs for harmonic mitigation in a three- phase system with balanced load. PQ theory was implemented for estimating reference compensating currents of SAPF. LSPWM method was implemented for generating gating pulses for three- level, five- level and seven- level CMLIs. ANFIS controller was employed for processing the error between reference and actual DC link voltages such that DC link voltage is maintained constant. The performance of these SAPFs was observed and corresponding waveforms were presented. %THD in source currents was measured and compared. It was observed that when three- level CMLI based SAPF was connected to the system, %THD is source current at PCC is about 6.30% which exceeds IEEE standards. %THD in source currents is reduced to 4.80% when five- level CMLI based SAPF is connected. It was observed that when seven-level SAPF was employed harmonic content in the source current at PCC is reduced to an acceptable level of 1.30%. Thus ANFIS controller based seven- level SAPF resulted in satisfactory current harmonic mitigation as compared to three- level and five- level SAPFs.

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