International Journal of Recent Technology and Engineering (IJRTE)
ISSN: 2277-3878, Volume-8 Issue-5, January 2020

Bidirectional Resonant DC-DC Converter for Microgrid applications

Amritha. G, Kanimozhi. G, Umayal. C, Ravi. S

Abstract: ***This paper presents a non-isolated bidirectional soft-switching dc-dc converter for DC microgrid energy storage synchronization. To assist the soft switching of switches and diodes, the LCL resonant circuit is applied and an input end half-bridge boost converter is enforced. Using the voltage doubler circuit introduced on the output side, a voltage gain of 2X is achieved. Through the non-isolated circuit, the total voltage gain is obtained. The capacitive divider halves the voltage on the greater hand. The circuit performs a high frequency ripple of low output voltage. Diodes guarantee zero voltage Turn ON for switches and zero current turn ON and turn OFF during buck / boost operation Although no internal snubber circuits are available, the circuit ensures low voltage stress across semiconductor systems.***

Keywords: bidirectional converter; DC Microgrid; zero current switching; buck-boost operation; zero voltage switching

I. INTRODUCTION

Electricity generation from non-renewable energy sources contributes to pollution of the environment and risks to human lives. Generation plants are generally situated away from urban and residential regions to prevent pollution negative impacts. But this leads to a significant quantity of energy being wasted through transmission losses. In such situations, microgrids play a crucial role. The transmission losses are negligible when the energy generation meets the load demands, thus improving effectiveness.

Micro grids achieve this by using photovoltaic panels to generate variable DC, controlled by means of a regulator or regulatory circuit, and supplied to load.Fig.1 shows the DC microgrid architecture. A 380V DC bus is used for the transmission of power from multiple sources of renewable electricity. Generally speaking, the energy storage devices implemented in the generation schemes have a 48V rating, while the DC bus has a 380V rating. For step-up and step-down activities, this requires a buck-boost bidirectional converter as the voltage ratio is nearly 8 times.

Manuscript published on January 30, 2020.
* Correspondence Author
Kanimozhi G*, School of Electrical and Electronics Engineering, VIT Chennai, Tamilnadu, India.
Amritha G School of Electrical and Electronics Engineering, VIT Chennai, Tamilnadu, India.
Umayal.C, School of Electrical and Electronics Engineering, VIT Chennai, Tamilnadu, India.
Ravi.S, Department of Electrical, Computer and Telecommunication Engineering, Botswana International University of Science and Technology, Botswana

Therefore the bidirectional buck / boost converter must be designed to operate in high duty ratio. This situation leads to stress throughout the diodes and increased losses of inverse regeneration resulting in low effectiveness of the converter [3-6].

There are and are presently in use several topologies of isolated and non-isolated DC-DC converters. Due to low magnetic bulk, high effectiveness, non-isolated converters generally have an edge over others and are very compact to use[7-9]. To achieve high-frequency switching, high power density of the DC-DC converter is crucial. Reported previously, the bidirectional converter topologies have a high operating frequency along with high switching capacity and high effectiveness but have constraints in either step-up or step-down ratios[10-14].

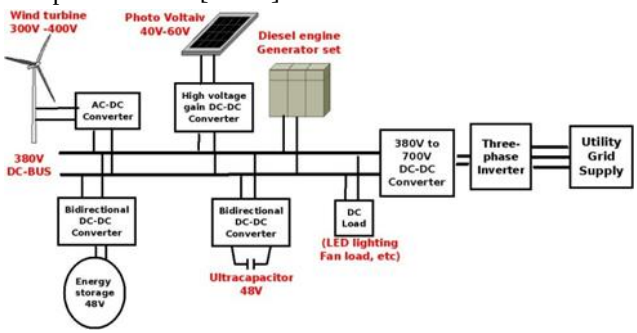


Fig. 1 Typical DC microgrid

The converter [10] mentioned has a high-frequency operation, but the use of coupled inductors leads to complications in design. For a broad range of load demands, the suggested topology is used in [11].

A high performance and step-up / step-down ratio converter is suggested in [15], but limitations include the use of coupling inductor and restricted frequency difficult switching. The converter in [16] is not intended for reasons of smooth switching. Fig.2. shows the converter you are proposing. The benefits of the design proposed are as follows. 1) ZVS of all buck-boost switches during turn ON and OFF time. 2) Low tension through the switches. 3) A snubber circuit can be used to clamp the voltage across the switches. 4) Operation at high frequency. 5) The magnetic quantity decreased.

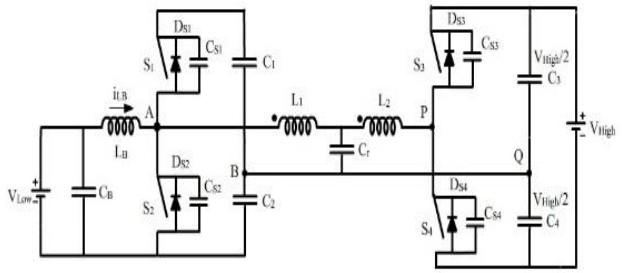


Fig. 2 The proposed converter

II. OPERATION OF CIRCUIT AND THE CONVERTER ANALYSIS

The suggested converter is a half-bridge boost converter operated through an LCL resonant circuit. This mixture of LCL helps to improve the output voltage gain and also increase the voltage. The S_1 and S_2 switches support ZVS and ZCS support for D_{s3} and D_{S4} switches. During buck operation, the voltage doubler circuit increases the profit twice; the high voltage is originally split into half, and with the assistance of switches S_3 and S_4 is further reduced. The LCL arrangement offers ZCS for diodes DS1 and DS2 and ZVS for switches S_3 and S_4.

The gate pulses of the S1 and S2 switches are complementary to each other during boost operation, while the S_3 and S_4 switches are turned off. Similarly, the door pulses of the S_3 and S_4 switches are complementary to each other during buck operation and the S_1 and S_2 switches are in OFF state.

A. Boost Operation

In boost operation, S_1 and S_2 are conducting and S_3 and S_4 are turned OFF.

Interval-1 (Fig. 4a) (t0 < *t* <*t1*): Initially S_1 and S_2 are not in conduction state. Due to difference in inductor current and resonant current, the parasite capacitor C_{S1} begins discharging. And this in turn charges C_{S2}. Power is transmitted via the output capacitors C_3 and C_4. At time t_1, capacitor C_{S1} releases its energy and the energy is stored in capacitor C_{S2} immediately. The switch current is given as $i_{S1}(t_1)=0$, $V_{S1}(t_1)=0$. and $V_{DS4}(t_1)=0$.

$$V_{S2}(t1)=\frac{V_L}{1-D}$$

(1) $D=\frac{T_{ON}}{T_S}$; T_{ON} = ON time of the main switch and T_S = total time interval. Here current flowing through the inductor i_{LB} and the switch1 are the same ie., $i_{S1}= i_1$

$$V_{Low}=L_B\Delta i_1+C_B\Delta V_{CB} \quad (2)$$

$$L_1\Delta i_{L1}+C_r\Delta V_{Cr}+C_{P2}\Delta V_{CP2}=0 \quad (3)$$

where C_{P2} is the combination of all capacitors.

$$V_{Cr}-V_{C4}-L_2(\Delta i_{DS4}-\Delta i_{L2})+R_4(i_{DS4}-i_{L2})=0 \quad (4)$$

Interval-2 (Fig. 4b) (*t1* < *t* <*t2*): The parasitic capacitor CS1 is completely discharged at t= t1 and CS2 is charged up. Since only the anti-parallel diode DS1 allows the difference between the current through the inductor and the resonant current, there is no voltage through S1. At t= t1, DS4 is biased forward. L1 and Cr start charging concurrently, C3 and C4 provide the load energy. Final values are

$$i_{S2}(t_2)=0, V_{S2}(t_2)=\frac{V_{Low}}{1-D},\ V_{S2}(t_2)=0$$

$$i_{Ds1}(t_2)=i_{LB}(t_2)-i_{L1}(t_2) \quad (5)$$

$$V_{C2}-V_{Low}-L_B\Delta i_B+D_{s1}R_1(i_{L1}-i_{LB})-V_{C1}=0 \quad (6)$$

Interval-3 (Fig. 4c) (*t_2* < *t* < *t_3*): Using ZVS, S_1 is powered ON at t= t2 switch. By switching S1, capacitor CS3, inductor L_1, resonant capacitor Cr and the current through the resonant inductor LB decreases linearly. The conductive diode D_{S4}, charging C_4 and diode D_{S3}, is biased in reverse. Power is supplied via C_3 to the load.

$$i_{S1}(t)=i_{L1}(t)-i_{LB}(t) \quad (7)$$

$$V_{Low}-L_B\Delta i_{LB}-V_{C1}-V_{C2}=0 \quad (8)$$

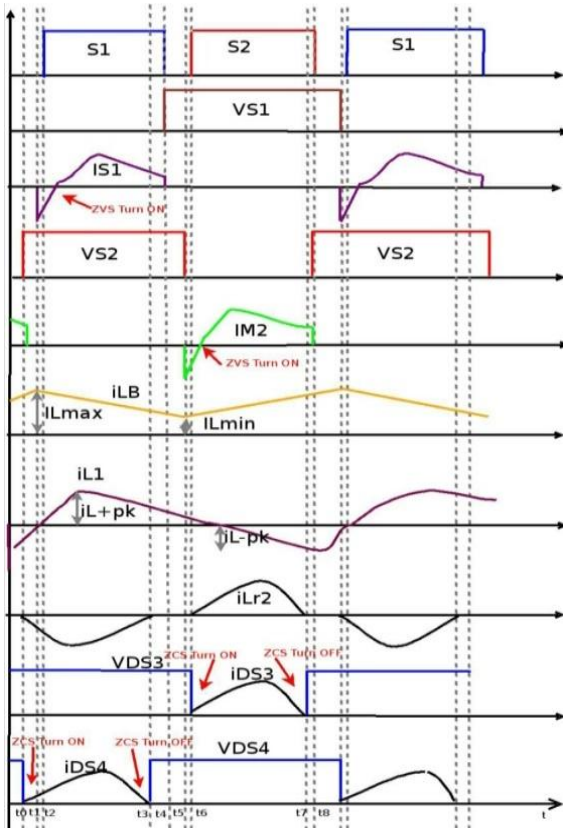
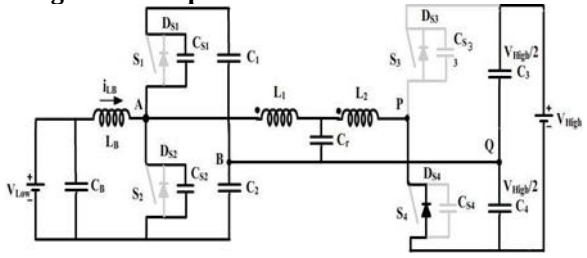
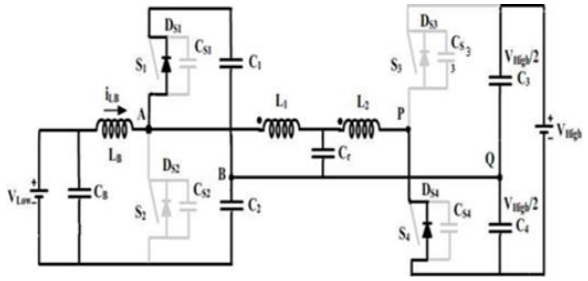


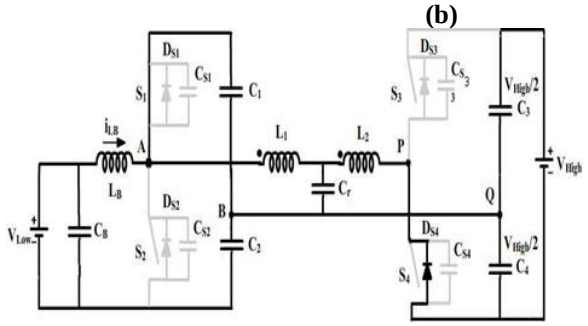
Fig. 3 Boost operation-Theoretical waveforms.



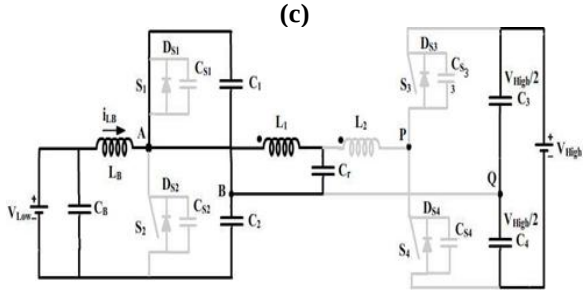
(a)



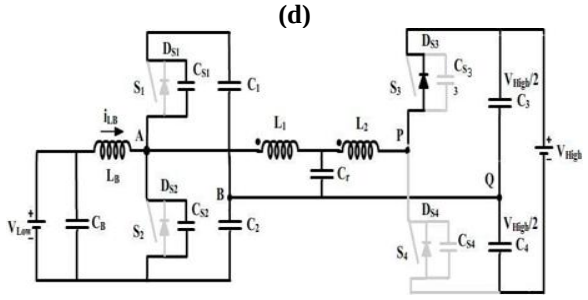
(b)



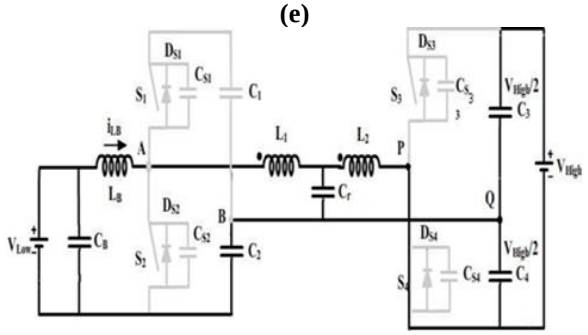
(c)



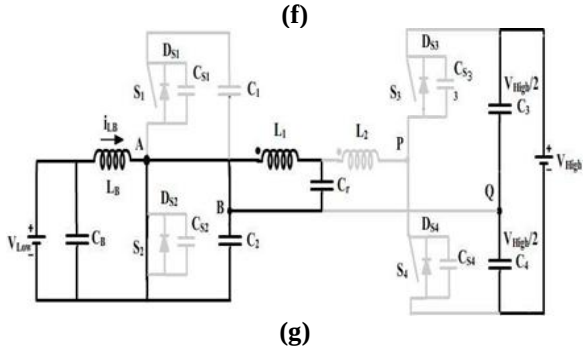
(d)



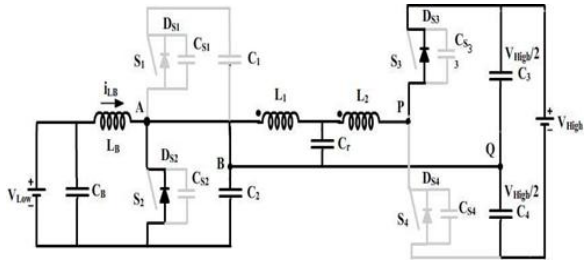
(e)



(f)



(g)



(h)

Fig. 4. Equivalent circuits of the converter operation in boost mode.

Interval-4 (Fig. 4d) ($t_3 < t < t_4$): S_1 is switched ON during this interval. The load side anti-parallel diodes are reverse biased. Switch S1 turns OFF at t= t4. Here you see VD_{S3} = 0, V_{S4} = 0, $V_{S2} = \frac{V_{High}}{1-D}$ Also, $i_{S1} = i_{LB}$

$$i_{LB}(t) = i_{LB}(t_3) - \frac{(V_{LB} - V_{C1} - V_{C2})}{L_B} \quad (9)$$

$$i_{L1}(t_3) = \frac{V_{C1} - V_{Cr}}{L_1} \quad (10)$$

Interval-5 (Fig. 4e) ($t_4 < t < t_5$) :S_1 and S_2 are not in conduction state. The C_{S1} parasitic condenser is fully loaded while C_{S2} is discharged. Since there are no diodes conducting, at the load side, no energy flow occurs from the input end to the output end. The load is therefore driven by C3 and C4. CS2 is discharged at the same moment and CS1 is loaded. $\frac{V_{High}}{1-D}$.

$$V_{High} = V_{High/2} + V_{High/2} \quad (11)$$

$$V_{Cr} - L_2 \Delta i L_2 - D_{S3} R_3 i L_2 - V_{High/2} = 0 \quad (12)$$

Interval- 6 (Fig. 4f) (t5 < t <$t6$): Anti-parallel diode D_{S2} starts conducting due to the difference of i_{L1} and i_{LB} while S_2 is triggered for ZVS turn-ON. All the anti-parallel diodes in the output side are reverse biased. Therefore $i_{S1}(t_6) = 0,\ i_{S2}(t_6) = 0, V_{S2}(t_6) = \frac{V_{Low}}{1-d}$

$$V_{S2}(t_6) = 0.\ i_{Ds2}(t_6) = i_{LB}(t_6) - i_{L1}(t_6) \quad (13)$$

$$V_{Low} - L_B \Delta i_B + D_{S2} R_2 (i_{L1} - i_{LB}) = 0 \quad (14)$$

Interval- 7 (Fig. 4g) (t6 < t < $t7$): S_2 is switched ON via ZVS at t = t2 switch. LB is starting to load. Inductor L_1, Cr and C_{S4} condensers are in resonance. The D_{S3} diode is pushed forward throughout this interval and is in conductive mode. D_{S3} turns off at t= t7.

$$i_{LB}(t) = i_{LB}(t_6) + \frac{V_{LB}}{L_B}(t - t_6) \quad (15)$$

$$i_{L1} = -\frac{(V_{Cr}(t_6) + V_{C2}(t_6))}{Z_r} \quad (16)$$

Where $Z_r = \sqrt{\frac{L_1(C_1 + C_r)}{C_1 C_r}}$

Interval- 8 (Fig. 4h) ($t7$ < t <$t8$): All diodes are turned OFF in the output hand and the C_3, C_4 condensers transfer energy to the load. Switch S_2 is switched on and inductor LB is storing energy and the switch turns OFF at t = t_{S2}.

B. Buck Mode Operation:

The theoretical waveforms in buck mode are shown in Fig. 5. During this mode, S_1 and S_2 are not conducting while S_3 and S_4 are conducting.

Interval 1 (Fig. 6(a); *t0* < *t* <*t1*): Towards the starting of this interval, S_3 and S_4 are switched OFF.

The resonant current iL2 begins to discharge the CS3 parasite capacitor and charges the CS4 condenser.

The energy is transmitted by the output capacitor Cr to be loaded. DS2 completes the resonant inductor current iL1 route. Finally, the CS4 parasitic condenser is fully charged to high. And CS3 is discharged completely.

The definitive values are i_{S3} (t1) =0, i_{S4} (t1) = 0, V_{S3}=V_{High} and V_{S4}=$i_{D_{S_2}} = i_{L_1} - i_{L_B}$ (17)

Interval 2 (Fig. 6(b); *t1* < *t* <*t2*): The capacitor C_{S3} is fully discharged at the beginning of this period, while the parasitic capacitor C_{S4} is charged to the maximum. Current resonant iL2 flows through the D_{S3} anti-parallel diode. This results in a situation of zero voltage throughout the S_3 switch. Diode D_{S2} is still conducted while diode D_{S1} is biased backwards. I_{S3} (t2)=0, i_{S4}(t2)=0, V_{S3}(t2)=0 and V_{S4}(t2)=V_{High} are the final values. The phenomenon current in resonant inductor L_2 is given by

$$\Delta i_{L_2} = \frac{V_{C_r} - 0.5V_{High}}{L_2} \quad (18)$$

$$i_{L_1} D_{S_2} R_2 - L_1 \Delta i_{L_1} - V_{C_r} - V_{C_2} = 0 \quad (19)$$

$$V_{C_r} - L_2 \Delta i_{L_2} - V_{C_{S_4}} - \frac{V_{High}}{2} = 0 \quad (20)$$

$$V_{C_2} + i_{L_2} D_{S_2} R_2 + L_1 \Delta i_{L_B} + V_{C_r} = 0 \quad (21)$$

$$V_{L_B} - L_1 \Delta i_{L_B} - V_{C_2} = 0 \quad (22)$$

$$i_{L_1} = \frac{V_{C_r} + V_{C_2}}{Z_r} \quad (23)$$

$$where\ Z_r = \sqrt{\frac{L_2 (C_s + C_r)}{C_s C_r}}$$

Current through inductor L_B is expressed as

$$i_{L_B}(t) = i_{L_B}(t_0) - \frac{V_{L_B}}{L_B}(t - t_0) \quad (24)$$

Current through diode D_{S_2} is

$$i_{D_{S_2}}(t - t_0) = i_{L_1}(t - t_0) - i_{L_B}(t - t_0) \quad (25)$$

$$V_{low} - L_B \Delta i_{L_B} - L_1 \Delta i_{L1} - V_{C_r} - V_{C_2} = 0 \quad (26)$$

Interval 3 (Fig. 6(c); *t2* < *t* <*t3*): When *t*=*t2*, S_3 is switched ON. A voltage $V_{High\ /2}$ is fed via switch S_3 to the resonant circuit. The capacitor C_3 resonates with inductor L_2 and capacitor *Cr*. The load side energy is transmitted to output along the capacitor C_o. The freewheeling energy accumulated in inductor L_B is achieved by diode D_{S2}. The current flows through inductor (L_2) $i_{L2,}$ continues to flow through diode $D_{S2.}$ This interval terminates at *t*=*t3* as the switch S_3 is turned OFF.

Interval 4 (Fig. 6(d); *t3* < *t* < *t4*): The switches S_3 and S_4 are turned OFF, during this interval. Parasitic capacitor C_4 begins to discharge and capacitor C_3 commences to store energy through current i_{Lr2}. Anti-parallel diode D_2 is forward biased. Output capacitance C_O provides power to the load. At t=t_4 parasitic capacitance C_4 gets discharged completely while parasitic capacitance C_3 gets fully charged to V_H. The final values can be given as i_{S3} (*t4*) = 0, i_{S4} (*t4*) = 0, V_{S3}=V_H **and VS4=0.**

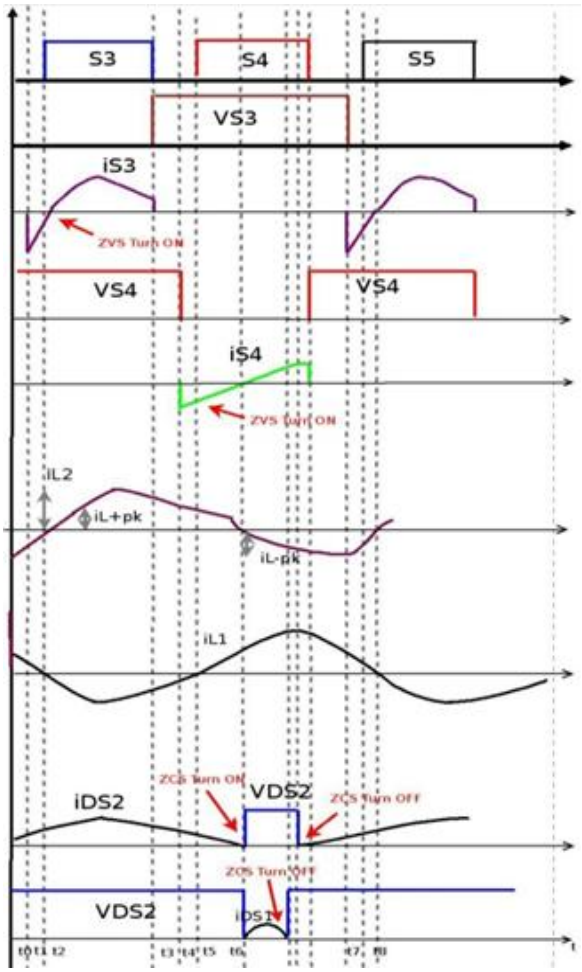
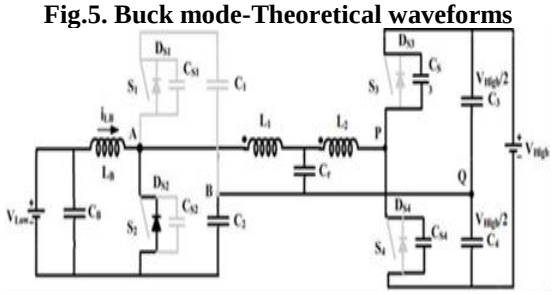


Fig.5. Buck mode-Theoretical waveforms



(a)

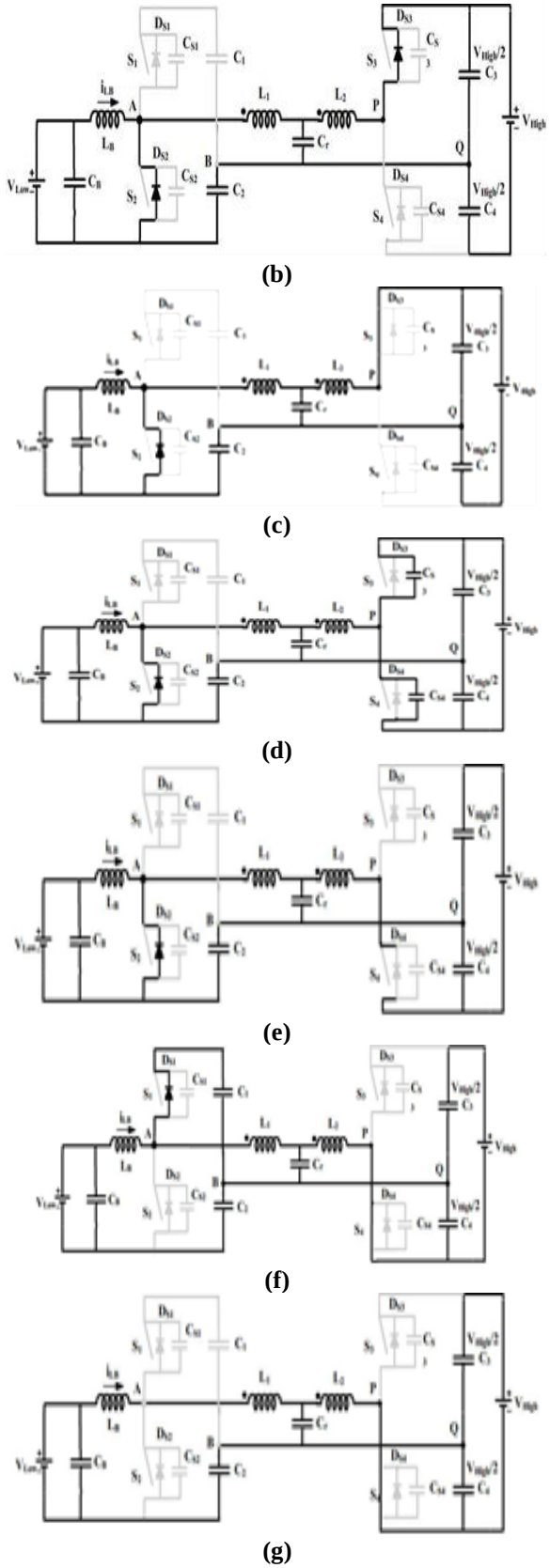


Fig. 6. Equivalent circuits of the converter in buck mode

Interval 5 (Fig. 6(e); *t4* < *t* < *t5*): In this time period, the anti-parallel diode D4 begins conducting due to the resonant inductor current iLr2, so that S4 can be switched on by ZVS. The D2 is still performing on the output side. The anti-parallel diode D2 is switched off by ZCS at the end of this period. These parameter's absolute values are iS3(t5)=0, iS4(t5)=0, VS4(t5)=0, VS3(t5)=VH.

Interval 6 (Fig. 6(f); *t5* < *t* < *t6*): S4 is switched ON at time instant t = t5 with zero voltage across it. Switch S4, turns off the iLr2 resonant current. D1 is pushed forward at the beginning of this interval and the energy storing begins in capacitor C5. The D1 diode switches OFF at t = t6 and the current is null.

Interval 7 (Fig. 6(h); *t6* < *t* < *t7*): Neither of the anti-parallel diodes *D1* and *D2* is conducting in this period. Throughout this time period, S_4 is ON state and at t=t7, S_4 is switched OFF.

III. VOLTAGE RATIO IN DIFFERENT MODES

a. Boost mode gain

The converter achieves its total gain by three stages. The gain contributed by the half-bridge boost converter is V_L/ (1-D), followed by LCL resonant circuit which provides a voltage gain related to the frequency of the switch. The voltage doubler circuit further improves converter gain by 2 times. Therefore, the overall gain is given by

$$V_{High} = \frac{V_{Low} \cdot G_{boost}(f) \cdot 2}{1-D}. \qquad (27)$$

Where $G_{boost}(f) = \frac{(X_{L1} + R_{ac})R_{ac}}{(X_{L1} + X_{CP})(X_{L2} + R_{ac}) + R_{ac}}$

f is the switching frequency, D is the duty cycle, R_{ac} is effective AC load resistance which is $R_{ac} = \frac{2R_{dc}}{\pi^2}$, X_{Cr}, X_{L2}, X_{L2}, X_{c2} are reactance of C_r, L_1, L_2 and C_2 respectively.

Fig.10 (d) demonstrates the differences in output strength and their gain impacts. Load energy is proportional to the increase in direction. It can be noted that frequency influences the conversion gain of the suggested converter.

b. Buck mode ratio:

Only half of the voltage VH is applied to the resonant part due to the voltage divider circuit. The total step-down ratio may be expressed as

$$V_{Low} = 0.5 V_{High} D_{Buck} G_{Buck}(f) \qquad (28)$$

Where $G_{buck}(f) = \frac{X_{CP} R_{acb}}{X_{L1}X_{CP} + X_{C2}X_{CP} + X_{L1}X_{L2} + X_{C1}X_{L1} + X_{CP}X_{L1}}$

Fig. 8(a) shows the load-dependent profit. Compared to a reduced load, the buck percentage for a greater load is much smaller. Fig. 8(b) shows the relationship between the general buck mode ratios when the frequency of switching is diverse.

Clearly, the step-down ratio depends on the rate of switching, which is, the step-down ratio increases with frequency.

IV. CONVERTER DESIGN

The converter design methodology is discussed here using an illustration for the following specifications: VLow=48V, VHigh=380V, energy output, PO=350W. The following are the hypotheses:

(a) Converter efficiency is presumed as 100%.

(b) Voltage ripples across capacitor *C5*, *C6*, *C7* and *C8* to be very insignificant or minute.

(c) The converter elements are considered perfect and lossless. The design equations are derived for the purpose of deciding the component ratings.

The average current through the input inductor is expressed as

$$I_{in} = \frac{P_o}{\eta V_{in}} = 6.25A \quad (29)$$

Duty ratio (D_{Boost}) is selected at input voltage, i.e., V_L = 48V and full load based on maximum voltage of the switch.

$$D_{Boost} = \frac{DV_{High} - V_{low} \cdot G_{Boost}(f).2}{V_{High}} = 0.699 \quad (30)$$

The boost inductor L_B on the input side is expressed as

$$L_B = \frac{V_{in} D_{boost}}{\Delta i_{in} f_s} \quad (31)$$

where Δi_{in} is the ripple current for the boost inductor. For, Δi_{in}=2A, L_B=159.77µH.

Sufficient differences in the energy stored in inductor L and L_B are maintained to achieve ZVS of lower switch S_2 and charge the capacitance C_{S1} and discharge C_{s2}. The same is given by

$$\frac{1}{2} L_B {I_{avg}}^2 - \frac{1}{2} L_1 {i_{L_1}}^2(t_5) > \frac{1}{2}(C_{S1} + C_{S2}) \left(\frac{V_{in}}{1-D}\right)^2 \quad (32)$$

The energy stored in the resonant inductor L1 at the time instant $t = t1$ must be greater than the energy stored in the device capacitances of S1 and S2 in order to ensure ZVS turn-ON of switch S1 and the condition is expressed as

$$\frac{1}{2} L_1 {i_{L1}}^2(t_1) - \frac{1}{2} L_1 {I_{avg}}^2 > \frac{1}{2}(C_{S1} + C_{S2}) \left(\frac{V_{in}}{1-D}\right)^2 \quad (33)$$

In order to make sure ZVS for the switch S3, the energy stored in the resonant inductor L2 at the t = t1 interval must be higher than the energy stored in the S3 and S4 capacities of the device.

$$L_1 {i_{L1}}^2(t_1) > (C_{S3} + C_{S4})(V_H)^2 \quad (34)$$

Similarly, the energy accumulated in the resonant inductor L2 during the interval t = t4 must be higher than the energy in the capacitance of the switches S3 and S4 for the switch S4 ZVS situation.

Table-I Converter Specifications

Parameters	Values/ Part no
Rated power (P_o)	350W
Low side (V_{low}) voltage	48V
High side voltage (V_{high})	380V
L_B	160µH, CM610125
Switching frequency (f_s)	105 kHz
Inductors L_1 , L_2	30µH, PC47RM14Z-12
MOSFET S_1-S_4	FCH041N60F, 600V, 76A
DSP	TMS320F28035
Capacitors C_1 , C_2	100µF
Capacitor C_r	0.1µF
Capacitors C_3, C_4	30µF
Capacitor C_o	330µF

$$L_1 {i_{L1}}^2(t_4) > (C_{S3} + C_{S4})(V_H)^2 \quad (35)$$

The LCL resonant frequency is given by

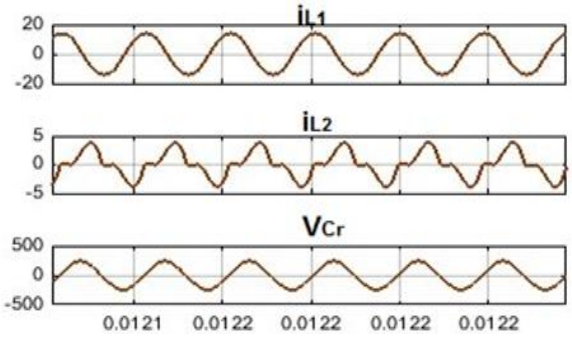
$$w_r = \sqrt{\frac{C_2 + C_r}{LC_2C_r}} \quad (36)$$

The capacitor C_1=C_2=100µF, L=L_1=L_2=30µH, and C_r=0.1µF for resonant frequency of 91.93 kHz.

V. PROTOTYPE RESULTS

The suggested 350W conversion is simulated to test and check the operation, evaluation and layout of the steady-state. The design requirements are shown in Table I. It was tested with V_{low}= 48V and V_{High}= 380V at complete load (350W) for both buck and boost operation. Simulation findings are shown in Fig.7 for boost operation. Fig. 7(b) confirms the switch S1's ZVS turn-ON since the DS1 anti-parallel diode is in conductive mode, resulting in zero voltage in S1 before the firing pulse is applied. The current at input and output end are 0.7A and 8.4A as shown in Fig.7(d). In the Fig.7(c) anti-parallel diodes, D_3 and D_4 can be seen to be conducting and switching with zero current. Therefore, there are no losses of inverse recovery. Fig.7(e) indicates that 48V is increased to 380V with a tiny ripple yield voltage and the ripple current of the boost inductor is also minimal.

Boost operation:



(a)

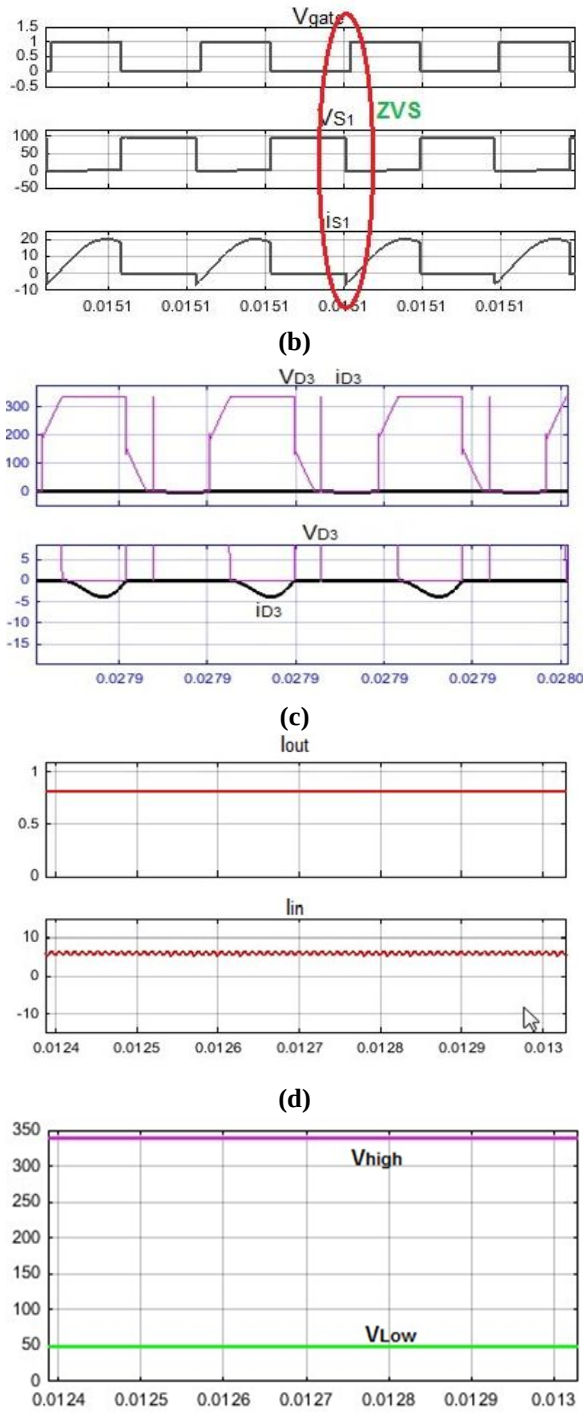
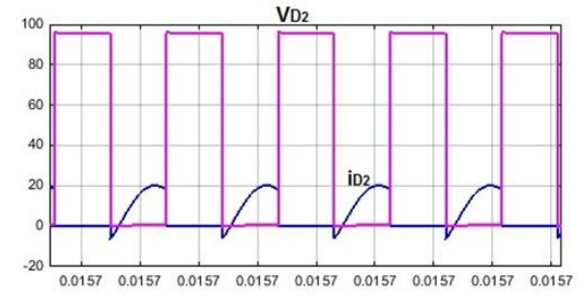


Fig 7:(a)Current through L1 & L2, Voltage across Cr (b)ZVS turn on of S1 (c)Current and Voltage across D2,D3 (d)Output and input current waveforms (e) Step up voltage from 48V and 380V

Buck operation:



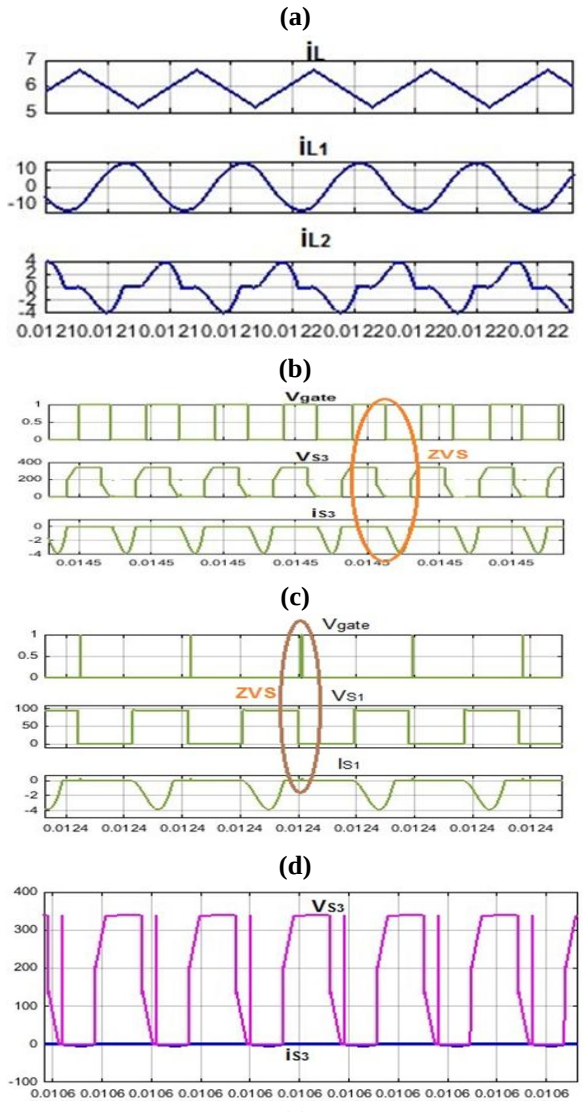


Fig 8:(a) Current and voltage through D2 (b):Current through L,L1,L2 (c) S3- ZVS turn-ON (d) S4- ZVS turn-ON (e)Voltage and current of S3.

The buck operation experimental findings are shown in Fig.8. Fig. 8(c) displays S3 switch gating signals. The anti-parallel diode conducts causing the S3 ZVS turn-on, before its triggering pulse. Similarly for S4, ZVS turn-on is examined in Fig.8(d). In the Fig.8(a), D2 diode anti-parallel switches to zero current. Reverse retrieval losses are therefore not relevant. The experimental waveforms can be observed to coincide with the waveforms operating on the analytically expected steady-state. In various load circumstances, the converter also retains soft-switching.

VI. CONCLUSIONS

A bidirectional dc-dc converter with a transformer-less LCL resonant is suggested. Elevated step-up or step-down ratio, high performance, low device voltage stress, ZVS turn-on for all switches, and ZCS turn-on and turn-OFF for all diodes, both in buck and boost mode, are features of the converter.

The proposed converter can attain ZVS for switching for a different load spectrum. Without any internal snubber circuit, the device voltage is retained. The findings of the simulation are verified to confirm the proposed evaluation, layout and soft-switching as well as validate the converter efficiency. The converter retains high effectiveness, particularly during the two-way energy flow.

REFERENCES

1. Lasseter, R.H. and Paigi, P.,"Microgrid: a conceptual solution," IEEE Power Electronics Specialists Conference, vol.6, pp.4285-4290, June 2004.
2. Ito, Y., Zhongqing, Y., Akagi, H., "DC microgrid based distribution power generation system," IEEE Power Electronics and Motion Control Conference, vol.3,pp.1740-1745,Aug. 2004.
3. Gerber, M., Ferreira, J.A, Seliger, N. and Hofsajer, I.W., "Design and evaluation of an automotive integrated system module," IEEE Industry Applications Conference, vol.2, pp.1144-1151,Oct. 2005.
4. H.-L. Do "Non-isolated bidirectional zero-voltage-switching DC-DC converter", IEEE Trans. Power Electron., vol. 26, no. 9, pp.2563 - 2569 2011.
5. D. Zhang, D. Y. Chen, and F. C. Lee, “An experimental comparison of conducted EMI emissions between a zero-voltage transition circuit and a hard switching circuit,” in Proc. IEEE Power Electron. Spec. Conf., pp. 1992–1997, 1996.
6. W. Li, X. Lv, Y. Deng, J. Liu, and X. He, “A review of non-isolated high step-up DC/DC converters in renewable energy applications,” in Proc.24th Annu. IEEE Appl. Power Electron. Conf. Expo., pp. 364–369, 2009.
7. X. Li and A. K. S. Bhat "Analysis and design of high-frequency isolated dual-bridge series resonant DC/DC converter", IEEE Trans. Power Electron., vol. 25, no. 4, pp.850 -862 2010.
8. S. Han and D. Divan "Bi-directional DC/DC converters for plug-in hybrid electric vehicle (PHEV) applications", Proc. IEEE 23rd Annu. Appl. Power Electron. Conf. Expo., pp.784 -789 2008.
9. Pan Xuewei and Rathore, AK., "Novel Bidirectional Snubberless Naturally Commutated Soft-Switching Current-Fed Full Bridge Isolated DC/DC Converter for Fuel Cell Vehicles," IEEE Transactions on Industrial Electronics, vol.61, no.5, pp.2307,2315, May 2014.
10. R. J. Wai and R. Y. Duan "High-efficiency bidirectional converter for power sources with great voltage diversity", IEEE Trans. Power. Electron. , vol. 22, no. 5, pp. 1986 -1996, 2007.
11. Das, P. and Moschopoulos, G., "Analysis and Design of a Non-Isolated Bidirectional ZVS-PWM Active Clamped DC-DC Converter," IEEE Applied Power Electronics Conference and Exposition, pp.1452-1458, Feb. 2009.
12. Lei Jiang Mi, C.C. Siqi Li et. al. "A Novel Soft-Switching Bidirectional DC–DC Converter With Coupled Inductors," IEEE Trans. on Industry Appl., vol.49, no.6, pp.2730-2740, Dec. 2013.
13. Kwon, Minho et. al.,"High Gain Soft-Switching Bidirectional DC–DC Converter for Eco-Friendly Vehicles.", IEEE Trans. on Power Electron. Vol. 29, no. 4, pp.1659-1666, 2014.
14. Jaisudha S., Sowmiya Srinivasan, Kanimozhi Gunasekaran, “Bidirectional Resonant DC-DC converter for Microgrid Applications,” International Journal of Power Electronics and Drives Systems, Vol.8, No.4, Dec 2017, pp- 1548-1561
15. Yi-Ping Hsieh et. al. "High-Conversion-Ratio Bidirectional DC–DC Converter With Coupled Inductor", IEEE Transactions on Industrial Electronics, vol.61, no.1, pp.210,222, Jan. 2014.
16. Kanimozhi.G, Umayal.C and Dhanasekar.S, “FPGA based Hybrid Resonant Switching DC/DC converter for Electric Vehicles”, International Journal on innovative Technology and Exploring Engineering, Vol .9 issue:9, pp- 334-340 ,July 2019.

AUTHORS PROFILE

Amritha G is perusing her Bachelor’s degree in Electrical and Electronics Engineering in VIT Chennai from 2016. Her research interest includes sensors and Internet of Things.

Kanimozhi.G received her Bachelor of Engineering from Bharathiyar University, Master of Engineering from Anna university and her Ph.D from VIT University, Chennai. She is working as Associate Professor in the School of Electrical Engineering, VIT Chennai. Her research area includes AC-DC converters for Electric vehicles, biomedical equipments, Electromagnetics, Multilevel inverters and DC-DC resonant converters.

Umayal.C, received her Bachelor of Engineering from University of Madras, Master of Engineering and Ph.D from Anna University. She is working as Associate professor in the School of Electrical Engineering, VIT, Chennai, India. She has authored many international and national level research papers on power factor correction in PMBLDC Drives.

Ravi.S,. received his Master of Engineering and Ph.D from Anna university. He is working as Associate Professor, in the department of Electrical Engineering, Botswana International University of Science, Botswana. He has authored many international and national level research papers. His research area of interest includes Intelligent control systems, Power System, Renewable Energy and Smart Grid