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High Speed PS0 Micro-Pipelined Adder

Mansi Jhamb, Hinduja Pudi, Sukant Vats

Abstract: ***For continuous monitoring of individual wellbeing, wearable devices are indispensable. The limitations of cost, utilization of power, delay and restricted device measurements are the basic issues which should be dealt cautiously while designing these battery powered devices. The wearables use high-end processors dedicated for complicated signal processing. Data path plays a key role in every digital signal processor. Adder is the most widely used component in wearable technology. This work proposes a novel architecture for PS0 pipelined adder. The proposed adder is implemented in 65nm TSMC CMOS and its performance has been compared with state-of-art adders. The SPICE level simulations are performed on HSPICE using 65nm TSMC CMOS @ 1.2 V. All the designs have been simulated with extracted wire and layout parasitics. The proposed adder ensures the lowest propagation delay which is 79.33% less when compared to RCA and has a power dissipation of 0.225 mw which is 25.4 % less as compared to CLA. Besides, the proposed adder offers a benefit of having lower transistor count which is 49.6% less as compared to RCA.***

Key words: Adder, pipeline, asynchronous, completion detector circuit (CDC), ripple carry adder (RCA), carry select adder (CSA), carry lookahead adder (CLA).

I. INTRODUCTION

Wireless Body Area Networks (WBANs) play a key role in health care remote monitoring systems and are considered as one of the emerging fields of research in health care systems. The WBAN's [IEEE 802.15.6] include sensors, batteries embedded DSP processor, transceivers [1-4]. While designing these devices, specific absorption rate (SAR) constraints must be taken into consideration and hence a need for energy efficient small-scale devices [5-8]. Adders constitute a significant role in DSPs, embedded processing units and ASICs [9]. The challenge here is to design an adder which shows less propagation delay, lower utilization of power and occupying less chip area for such applications. Asynchronous designs occupy less power as compared to synchronous counter parts due to absence of global clock [10]. This work proposes an asynchronous pipelined adder and its performance has been compared with state-of-art adders[11-14].The pipelining is discussed in section 2. The explanation to the proposed design is given in section 3 with simulations and results in section 4.

II. PIPELINING

In order to achieve high performance, pipelining is being used by almost all digital electronic systems. Since health care applications are powered using batteries,
we need an efficient and low power design at par with the current nanometer technologies [15-16]. Here, we describe two main pipeline styles:

2.1 Synchronous Pipelines

In synchronous systems, pipeline uses complex functional blocks which are sub divided into smaller blocks known as computational blocks. It contains registers for separating them and for attaining synchronization, global clock signal is applied. The Figure 1 illustrates the primary structure of synchronous pipeline. Here R1, R2 etc. signify elementa for storage, CL3,CL4 denote computational block and for global synchronization a clock signal (CLK) is used.

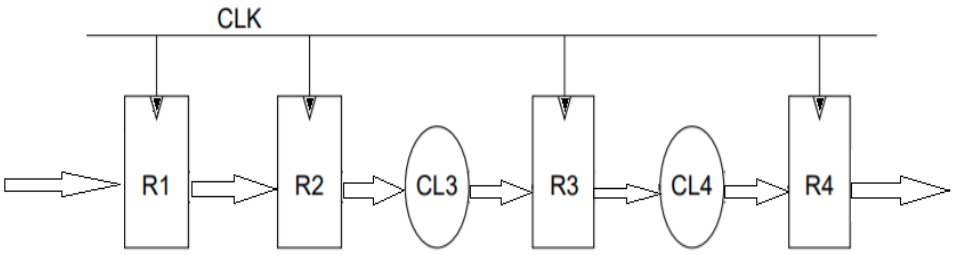

Figure 1- Synchronous pipeline structure

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* Correspondence Author
Mansi Jhamb*, Assistant Professor, University School of Information Communication and Technology,GGSIPU, NewDelhi, India
Hinduja Pudi*, University School of Information Communication and Technology, GGSIPU, NewDelhi, India. hindujaiiit@gmail.com,
Sukant Vats, University School of Information Communication and Technology, GGSIPU, NewDelhi, India

2.2 Asynchronous Pipelines

Asynchronous pipelines do not use clock signals.. It employs communication channel including both control and data. So, this is bidirectional communication and is executed by handshaking protocol. Request (Req) ,Acknowledge (Ack) are handshaking signals. Usually data is sent from transmitter (i.e. left part) and the acknowledge control signal is sent from receiver (i.e. right part).

The Figure 2 illustrates structure of an asynchronous pipeline. Req denotes request for initiating the computational procedure and the ack denotes acknowledgement signal sent by receiver to acknowledge completion of computationMerits of Asynchronous pipeline over synchronous design are lesser dyanamic power dissipation, atomatic flow control[17] as handshaking protocol inherently offers overflow and underflow protection and ease of variation of number of data items as per the need of application.

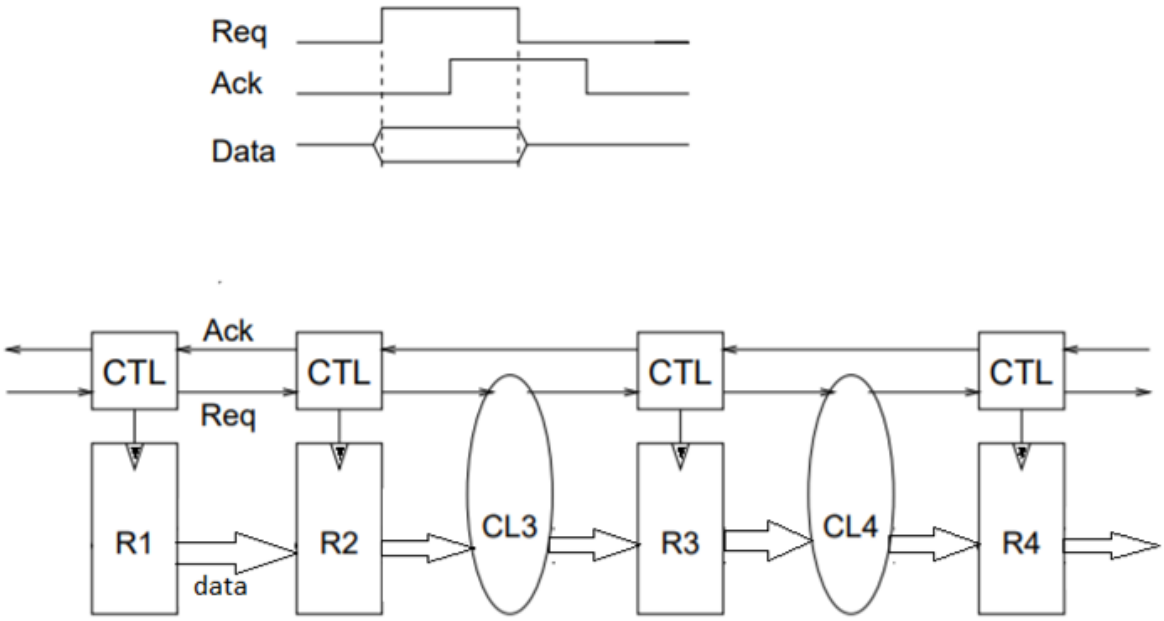

Figure 2- Asynchronous pipeline structure

III. PROPOSED WORK

This work proposes a novel PS0 Pipelined adder. The circuit consists of dual rail AND gate, dual rail XOR gate, dual rail OR gate and a completion detection circuit (CDC). In PS0, each stage comprises of a function block and a completion detector. Each function block alternates between two phases i.e, evaluate phase and a pre charge phase. Primarily, the function blocks are considered to be at reset and in evaluate phase. Once the date input arrives, the function is computed. In the pre charge phase, the function block is reset i.e, output returns to 0. A significant property to be considered about dynamic logic when it is being operated in the pre charge phase is that it can block new inputs that are applied to its function, and the stage's outputs remain reset. The functioning of PS0 Pipeline is as follows. Computation of stage 1, stage2,stage3.

Completion detector circuit (CDC) of stage 3 advances the acknowledgment signal representing the evaluation and completion. It begins the pre charging process for the second stage.The figure 3 shows the block diagram of PS0 Pipeline [18]. F1, F2, F3 represents functional blocks where as D1, D2, D3 represent completion detector circuit. The schematic of 1bit full adder is shown in figure 4 and the waveform is depicted in figure 5. The layout of proposed adder design is shown in figure 6.

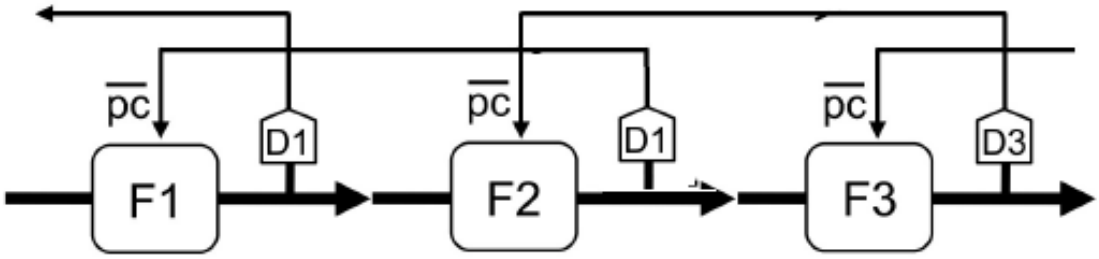

Figure 3- Block diagram of PS0 Pipeline

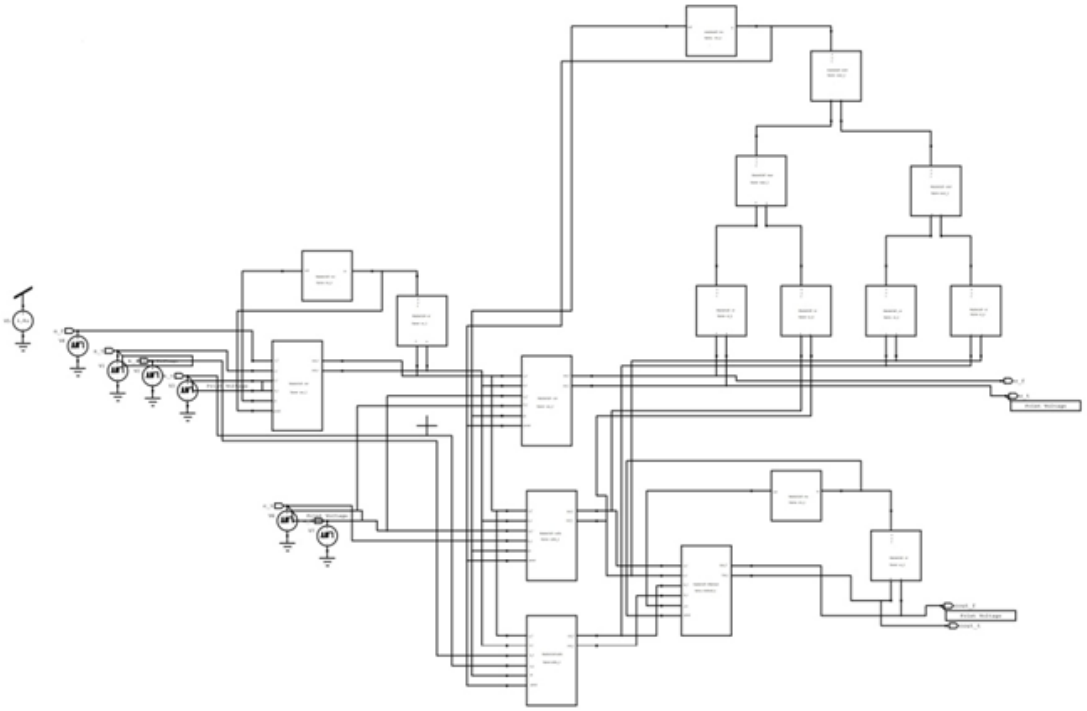

Figure 4- Proposed circuit schematic

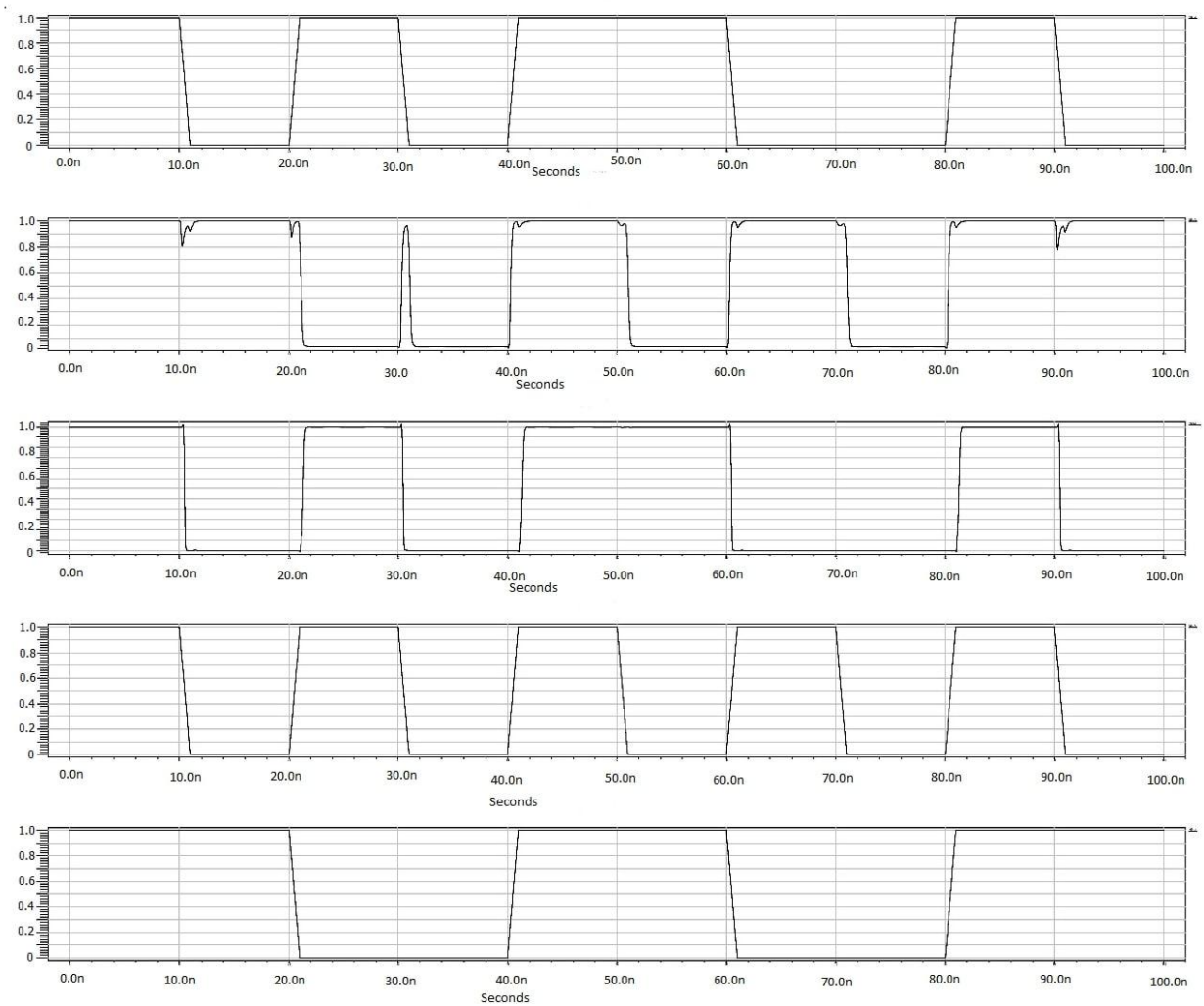

Figure 5- Proposed circuit waveform

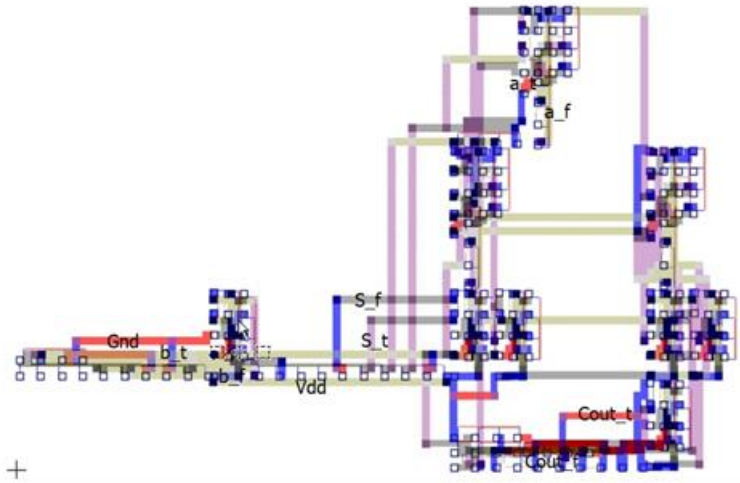

Figure 6- Layout of proposed adder

IV. SIMULATION AND RESULTS

The SPICE level simulations are achieved using HSpice using 65 nm technology with supply voltage of 1.2 V at a constant temperature of 25°C. We have proposed a 1bit PS0 pipeline-based adder and state-of-art adder designs have been compared by evaluating delays, Power dissipation, transistor count of the adders.

4.1 Power Dissipation

Power dissipation values of proposed adder along with state-of-art adders is show in table 1 at voltage supply of Vdd=1.2v. It is observed that the proposed adder shows 25.4 % less power dissipation as compared to CLA and 23.2% less as compared to Dual rail domino logic pipelined adder. Figure 7 shows the graphical representation of power dissipation of various adder designs.

Table 1- Performance analysis of different adders at Vdd= 1.2 V

Types of adder	Power (mw)	Propagation delay (ns)	No of transistors	Power delay product (pJ)
RCA [11]	0.206	4.2	288	0.865
CLA [12]	0.302	3.14	272	0.948
CSA [13]	0.194	1.37	152	0.265
Dual rail domino logic pipelined adder [14]	0.293	1.97	224	0.577
Proposed adder	0.225	0.868	145	0.2213

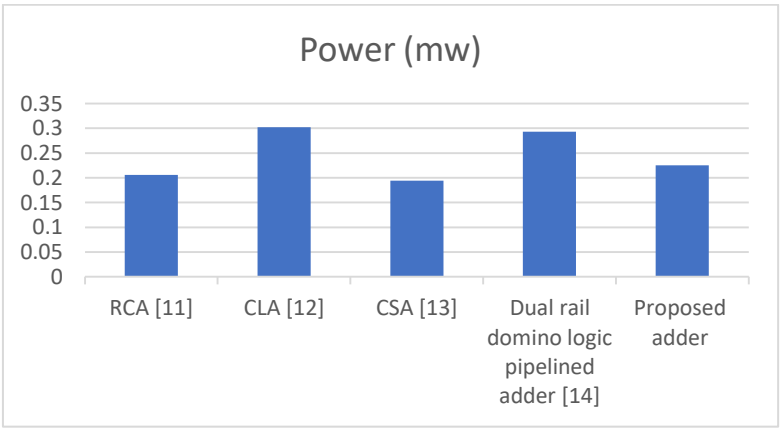

Figure - 7 Power dissipation of Adder designs.

4.2 Propagation Delay

The average propagation delay is computed by calculating tphl and tplh values. The Table 1 illustrates the change in propagation delay of proposed adder along with state-of-art adders with voltage supply of 1.2 v and it is observed that proposed work has least propagation delay and is 79.33% less when compared to RCA and 72.3% less than CLA, 36.6% less than CSA, 55.9% less than dual rail domino logic pipelined adder. So, for high speed operations, proposed circuit should be preferred.

Figure 8 shows the graphical representation of propagation delays of various adder designs.

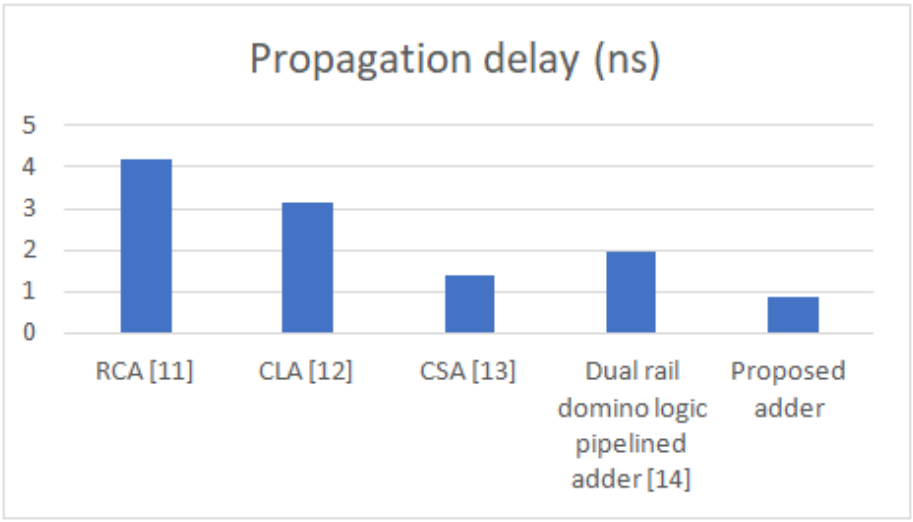

Figure -8 Propagation delay of Adder designs.

4.3 Power delay product

Power-delay product (PDP) helps in determining the performance of a system.The table 1 illustrates the pdp (power delay product) of adder designs. Figure 9 illustrates the PDP variation of proposed and state-of-art adders. Lower the PDP, higher the performance. For analyzing the energy dissipation of a switching event, PDP is computed for a voltage value of vdd=1.2v.

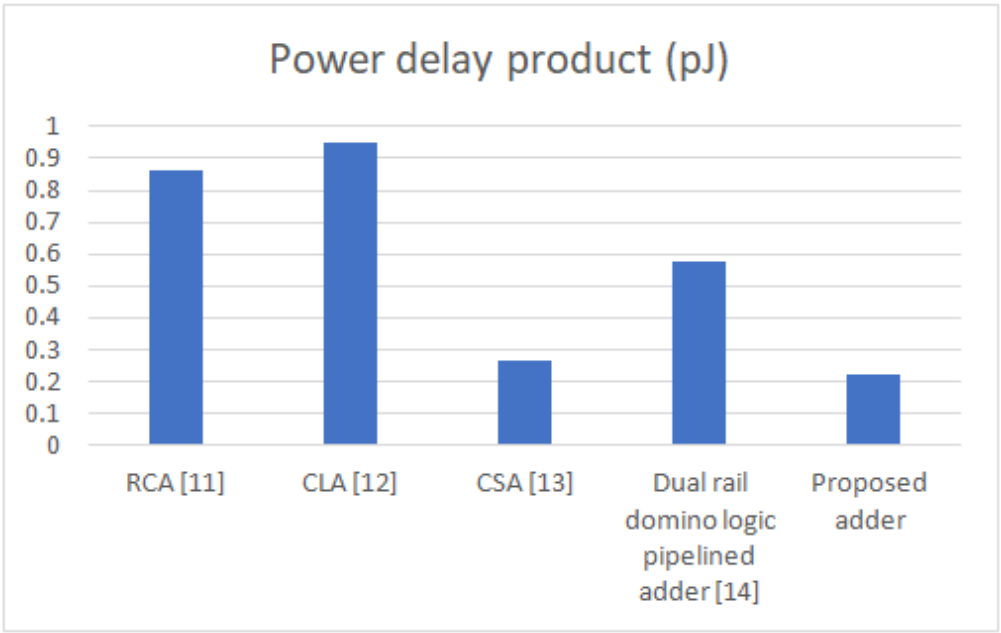

Figure -9 PDP of Adder designs.

4.4 Circuit complexity

In present-time micron CMOS technologies, many numbers of transistors are integrated over a single chip. So, circuit complexity is of a serious concern. This can be calculated in terms of total no. of transistors used to perform a logic function and the layout area required.From table 1, It is observed that proposed adder consumes 49.6% less no of transistors as compared to RCA, 46.6% less compared to CLA, 4.6% less compared to CSA, 35.2% less compared to Dual rail domino logic pipelined adder.Figure 10 shows the graphical representation of transistor count of various adder designs. Table 2 shows the chip area requirement of proposed adder along with state-of-art adders in terms of layout areas of various adder designs

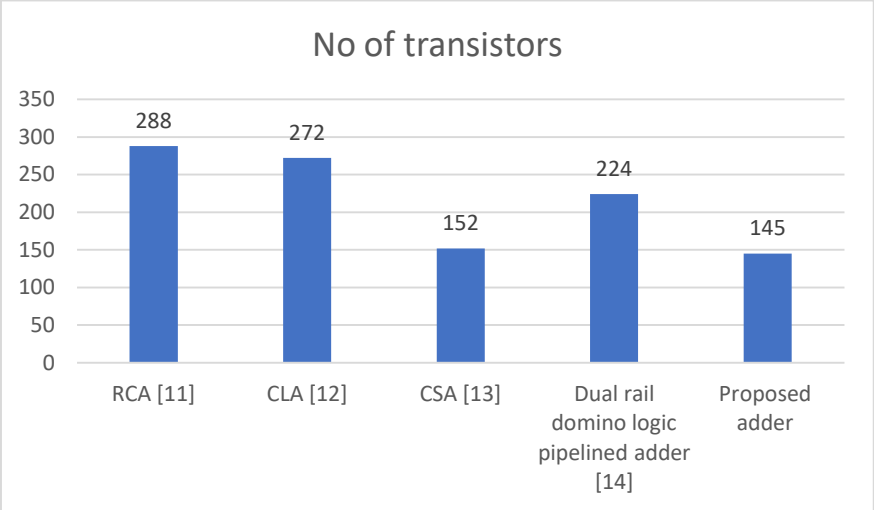

Figure- 10 Transistor count of Adder designs

Table 2- Layout area comparison of different adder designs

ADDERS	LAYOUT AREA (μm^2)
RCA [11]	2214
CLA [12]	2160
CSA [13]	6201
DUAL RAIL DOMINOADDER [14]	298.172
PROPOSED ADDER	1288

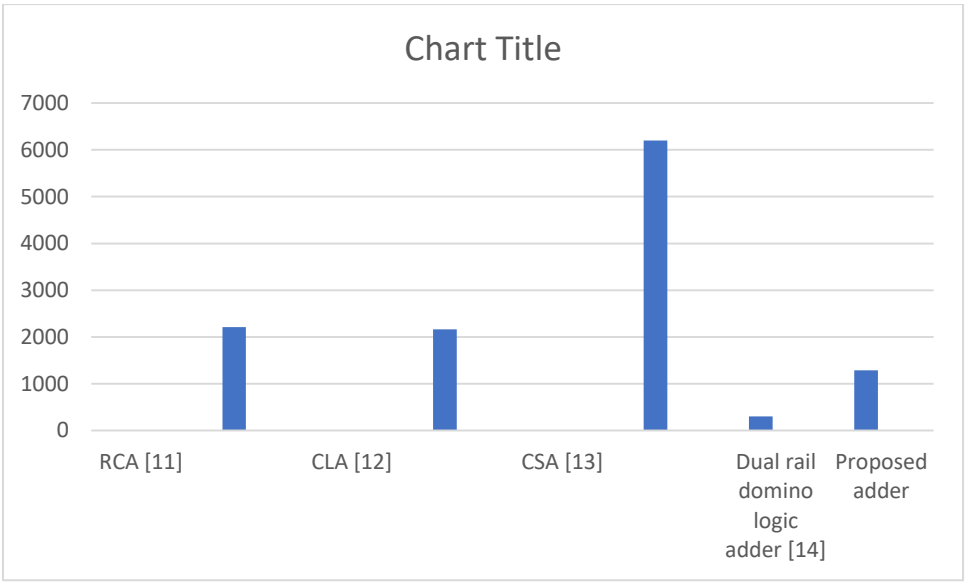

Figure- 11 Layout area of Adder designs

V. CONCLUSION:

This work proposed a PS0 based pipelined adder. The proposed design claims least propagation delay and reduced power consumption. The proposed adder is implemented and its performance has been compared with state-of-art adder designs. The SPICE level simulations are performed on HSPICE using 65nm TSMC CMOS @ 1.2 V. All the designs have been simulated with extracted wire and layout parasitic. It has been perceived that the proposed adder consumes marginal power 0.225 E-03 Watts which is 25.4 % less as compared to CLA. It offers the lowest propagation delay (0.868 E-09) @ 1.2V and has a transistor count of 145 which is49.6% less as compared to RCA.Our design guarantees great savings in power and latency, making it a perfect candidate for low power high speed wearable devices for IoT.

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AUTHOR'S PROFILE

Dr. Mansi Jhamb, is working as Assistant Professor in University School of Information, Communication & Technology. Her Major areas of interest include VLSI, Embedded System, Digital Design. She has Published many research papers in international journals & conferences.

Hinduja Pudi, has done research work in the area of VLSI.

Sukant Vats, has done research work in the area of VLSI.