Physical IC Design Layout of Memory-Based Real Fast Fourier Transform Architecture using 90nm Technology

Rajasekhar Turaka, M. Satya Sai Ram

***Abstract**: In this paper we present a low complexity physical IC layout for memory based Real Fast Fourier Transform (RFFT) architecture using 90nm technology. FFT architectures are the most important algorithms in the modern communication systems like and very high bit rate digital subscriber line (VDSL) asymmetric digital subscriber line (ADSL). In this FFT algorithm is based on radix-2 decimation-in-frequency. In order to meet the real time requirements of very large scale integration (VLSI), we designed a low complexity and high speed FFT architecture. The RFFT architecture was realised using Verilog hardware description language (HDL). This architecture is simulated using Native code launch of cadence and synthesized using RTL code complier of cadence tool. Each step of application specific integrated circuit (ASIC) physical IC design flow was synthesized using cadence Innovus 90nm technology and we optimize the design to reduce the area, power and timing requirements.*

***Keywords**: Fast Fourier Transform (FFT), real FFT, Application Specific Integrated Circuit (ASIC), Verilog HDL.*

I. INTRODUCTION

Recently, more convenient digital signal processors have been implemented on Very Large Scale Integrated (VLSI) circuit platform. Due to the no flexibility of DSP processors, the FFT algorithms are not implemented on DSP processor every time. Because of this less flexibility the total systems throughput was reduced. Now a days FFT algorithms utilized in modern communication systems like digital video broadcasting (DVB), digital audio broadcasting (DAB), ADSL and VDSL which are operated at high bit data rates, and also consume more area, power and operating time [1]. Real time digital signal processing is very important, which is utilized in several fields: radar & communication, satellite communications, etc. Its accuracy and computing speed are directly affecting the system behavior [2]. Though the Xilinx and Altera have implemented the most of the FFT Intellectual Property (IP) core which are used in Doppler blood flow spectrum study, the price of the design is too high so that it is not utilized widely. As a result, now several researchers designed the FFT processors, which are more suitable for themselves. Mostly, hardware implementation techniques are of Digital signal processors DSP, FPGA, and FFT dedicated chip. The essential structure of an FFT processor consists of a Random Access Memory (RAM), Read-Only Memory (ROM) and Butterfly Processing Unit (BPU). It is majorly utilized for storing data, Sequential Control Unit (SU), and Address Generation Unit (AGU). The most significant units involved in the FFT processor are AGU and BPU. Dual-port RAM is majorly utilized to store the input data, intermediate results and twiddle factors. The address used for reading data in butterfly operations is generated utilizing the address generation unit. It is significantly utilized to store the results of outcome data into the RAM. Additionally, control signals used for each and every module are generated utilizing an SCU [3]. Due to the extra configuration of switches and multiplexers reconfigurable devices requires more hardware area and processing time than a dedicated system. Because of this the device performance was limited which are operated at higher frequencies to get the same performance. To support changes in the operating length the reconfigurable devices require extra interconnects. Due to long interconnect paths and delay of passing the signal through switches & multiplexers increases the overall computational time and limits its operating frequency. Dynamic power dissipation increases as the frequency increases, because dynamic power is directly proportional to the operating frequency and static power also increased due to the more area occupied by the cells.

II. RELATED WORK

Ghosh et al. [4] proposed three various FFT architectures to well execute 1024-point fast fourier transform. In this research, the proposed FFT architecture has been simulated in Xilinx ISE 11.1 using very high speed hardware description language (VHDL) and also implemented on FPGA. The proposed FFT processors were designed utilizing various architectures. Using coordinate rotational algorithm and sine&cosine lookup table twiddle factors were generated. The performance of the proposed designs has been achieved better outputs in terms of hardware resource but throughput was poor. Le Ba et al. [5] proposed efficient 1024-point low power radix-2^2 FFT architecture with Feed-Forward MDC (FFMDC).

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This processor is based on radix-2^2 algorithm and this proposes a scheduling algorithm to avoid the memory conflict and intermediate value conflicts. This architecture has been implemented on 65nm complementary metal oxide semiconductor (CMOS) technology.

To achieve high speed it consumes more power and also requires more hardware utilization.

Luo et al. [6] proposed proficient memory addressing methods for FFT architecture design. Using the data relocation technique which can marge all the memory banks to attain less area and low power dissipation. In this paper, proposed FFT processor with memory addressing scheme was effectively perform with merged bank memory. The features of the resulting proposed FFT architecture as follows: Dual Port Merged Bank (DPMB) can be significantly simplified utilizing Single Port Merged Bank (SPMB) memory to minimize the physical size of the needed memory. The merged bank includes only one Address Generation Unit (AGU) for accessing the memory. Only write network logic was required so that the interconnection overhead reduced, respectively. The architecture was implemented on CMOS 180nm technology.

III. RFFT ARCHITECTURE WITH DPRAM AND VEDIC MULTIPLIER

The M-point discrete fourier transform (DFT) of an input sequence x(p) is given by

$$X(k)=\sum_{p=0}^{M-1} x(p)W_M^{pk} \qquad (1)$$

Here k = 0 to M-1 and W_M^{pk} is called twiddle factor.

Fig.1. shows the block diagram of RFFT architecture with dual port RAM and vedic multiplier which is based on the radix-2 decimation-in-frequnecy algorithm.

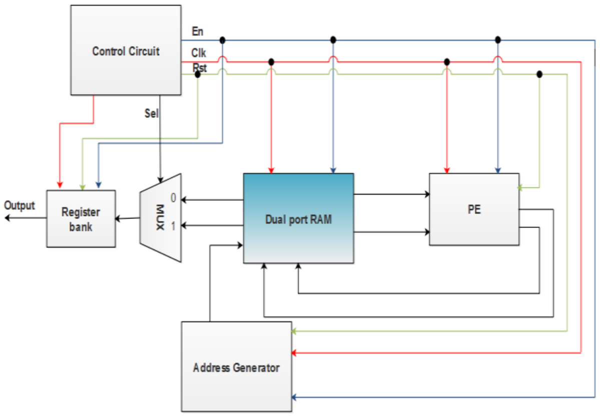

Fig.1. Block diagram of RFFT architecture with DPRAM and Vedic multiplier

The entire architecture is controlled by the control signals which are provoked from the sequential control circuit. The control circuit consists of signals of En, clk, rst and select. Address generator and processing element (PE) are the key elements in the architecture. The architecture is a 32-bit RFFT processor. Initially all the twiddle factor values are stored in the address generator and input values from 1 to 32 are stored in the dual port RAM (DPRAM) by using the address generator. In the 1st clock cycle, inputs are taken from the DPRAM and processed by the PE nothing but the butterfly computation is done and the results are stored back to the DPRAM. In the 2nd clock cycle the 1st stage outputs which are stored in the DPRAM are taken and processed using PE and the results are stored again in the same DPRAM. And this process continues until the last stage nothing but 5 stages are required for 32-point FFT. At the final stage the last stage outputs are stored in the register bank which can be taken as the final output [7]. Addition and multiplications are required for the butterfly computation which is the key operations in VLSI design. Additions are treated as the weak operations and multiplications are considered as the strong operations which will decide the device area and power and also the computation time. Carry look ahead (CLA) adder and vedic multiplier is used for addition and multiplication respectively. We have designed the carry look adder with the ripple carry mechanism which is the fastest for less number of bits and urdhva tiryagbhaym multiplier is designed which is based on ancient vedic mathematics. Urdhava tiryagbhaym is one of the fast multiplication algorithm.

IV. PHYSICAL IC DESIGN IMPLEMENTATION

In this we designed a physical IC layout for the RFFT architecture which is shown in fig.1. This section describes the typical physical IC layout process shown in fig.2. which refers to the backend design style. The number of transistors integrated on a silicon chip doubles and clock speed also doubles for every 18months.

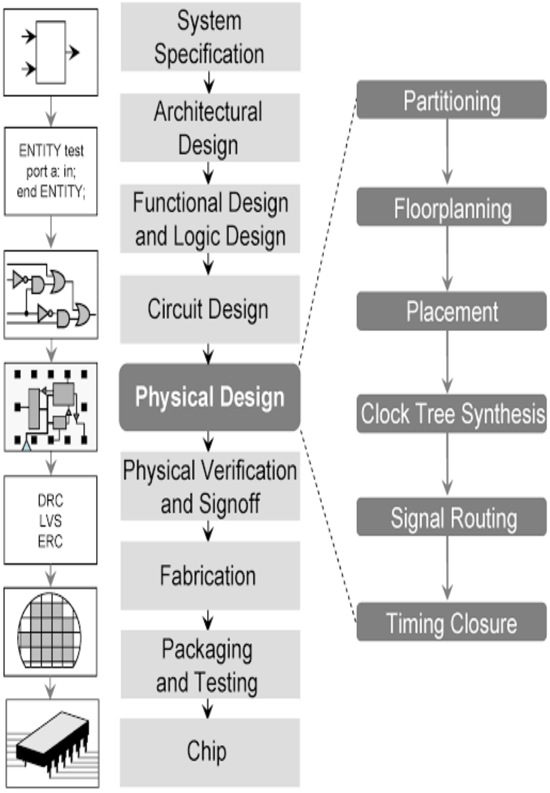

Fig.2. ASIC Physical IC design flow

This rate of improvement will continue and the system complexity also increases. Today integrated circuit (IC) design is divided into two phases: frond-end design using hardware description language and back-end design or physical design followed by fabrication step. Again the physical IC design is divided into full-custom where the designer has full flexibility and semi-custom design which consists of some pre-defined cells. Because of technology driven and market driven requirements we are choosing ASIC rather than FPGAs.

The major processing phases in the ASIC design flow are

- Gate level net-list
- Floor planning
- Partitioning
- Placement
- Clock tree synthesis
- Routing and
- Physical verification

Fabrication manufacturers like Cadence and Synopsys will provide the technology libraries which are based on the standard sizes like 180nm, 130nm, 90nm, 45nm, 22nm, 14nm etc., for the ASIC physical design.

Physical IC design is mainly constructed on the gate level net-list generated after synthesis step, where the RTL compiler converts the HDL code into gate level netlist which is the source file to the physical IC design flow. Floorplan describes how to map the modules onto silicon area and we specify a floorplan with the aspect ratio. In partitioning step, it is a process of partitioning the silicon into smaller logic cells and this step helps other steps make easier. This step done in the RTL design phase itself. Power planning is very important step in the design flow which is performed in four stages: global nets, power rings, power strips and special route.

Placement is done in four levels:

- Pre-placement
- In-placement
- Post-placement before CTS and
- Post-placement after CTS.

Initially the clock circuit was ideal. In the clock tree synthesis, clocks are propagated to the flipflops and clock tree is synthesized using clock inverters and clock buffers. It can minimize the clock skew and propagation delay. The routing process consists of two types: global routing and detailed routing. Allocation of routing resources for the connections was done by global routing and actual connections was done by detailed routing.

The last stage physical verification verifies the functionality and correctness of the designed layout through design rule check (DRC), layout vs schematic (LVS), antenna rule check and electrical rule check (ERC) [8].

V. RESULT AND DISCUSSION

This section describes the results of various steps involved in the physical IC design flow. The area, power and timing reports of various phases are listed below.

All the results are obtained from the Cadence custom IC & Virtuoso tool using 90nm technology library.

A. RTL Schematic

From the NClaunch simulator we can compile the .v files, elaborate the design and finally simulated. Using the Genus synthesis GUI we can map the mapping the design to get the RTL schematic of HDL code which is shown in fig.3.

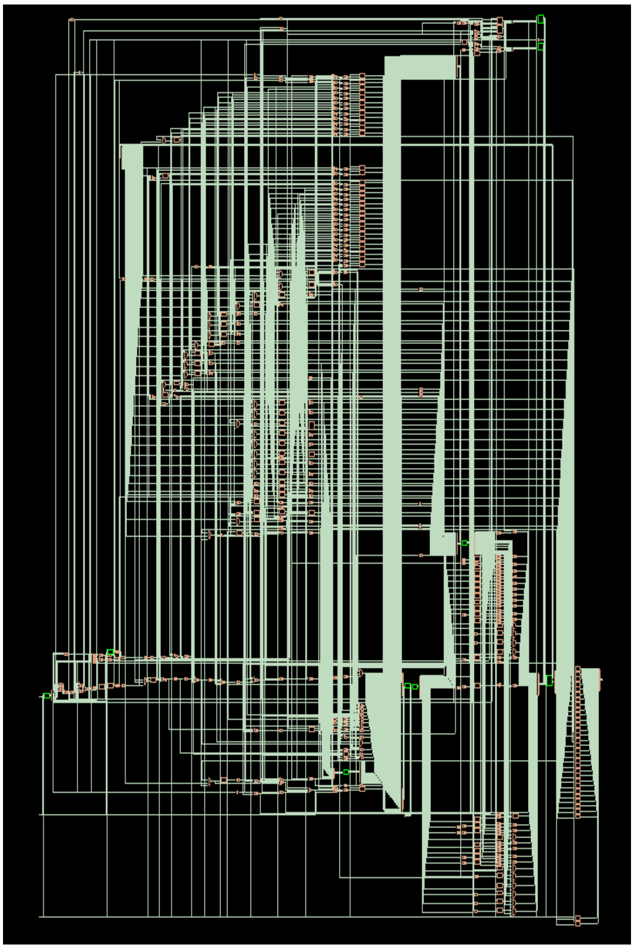

Fig.3. RTL Schematic of RFFT architecture

B. Floorplanning and Power Planning

The inputs for the physical design are: gate level netlist, library (lib) files, library exchange format (lef) files, Default.globals, Default.view, slow.v and block level system design constraints (SDC). Here we used Cadence Innovus implementation tool. We run the design with 90nm technology for the worst case conditions.

Firstly we can load the design using the command init_design. In the GUI, from floorplan we can select specify floorplan with the aspect ratio of 0.98 and core utilization about 70%. Floorplan of the design is shown in fig.4.

Power planning can be done in four stages and power supply rails VDD and VSS are defined as global nets. Metal 9 can be used as horizontal stripe and Metal 8 as vertical strip. The four stages of Power planning are:

- global nets,
- power rings,
- power stripes and
- a special route.

In this the overall resistance is will be reduced. Power planning is shown in fig.5.

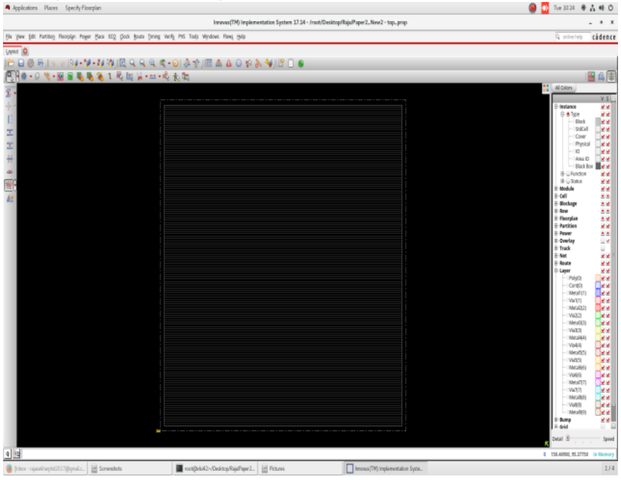
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Fig.4. Floorplanning

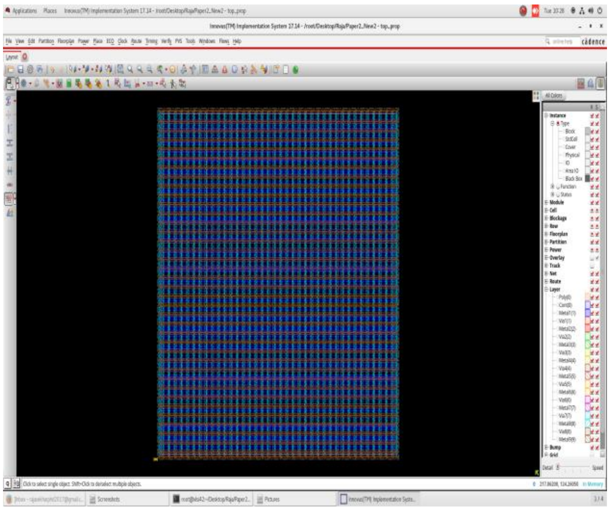
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Fig.5. power planning

C. Placement

In this step, standard cells will be placed on the design along with pins. Every standard cell has same height. End-caps and well-taps are used for the better design. Scan chains are neglected in the design. Fig.5 shows placement of standard cells and fig.6 shows the full placement.

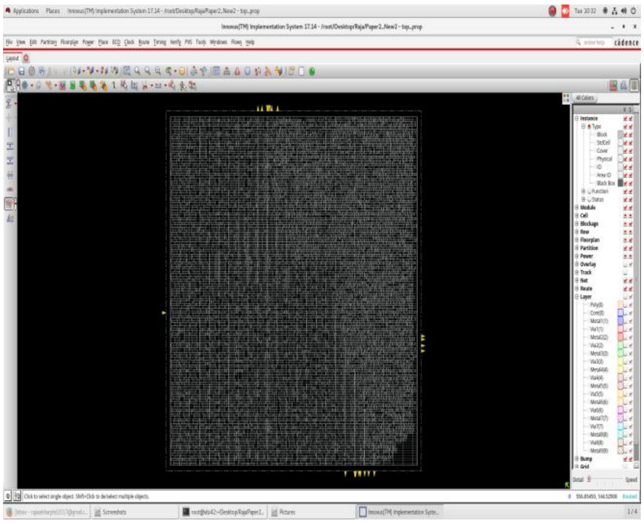
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Fig.5 Placement of stadard cells only

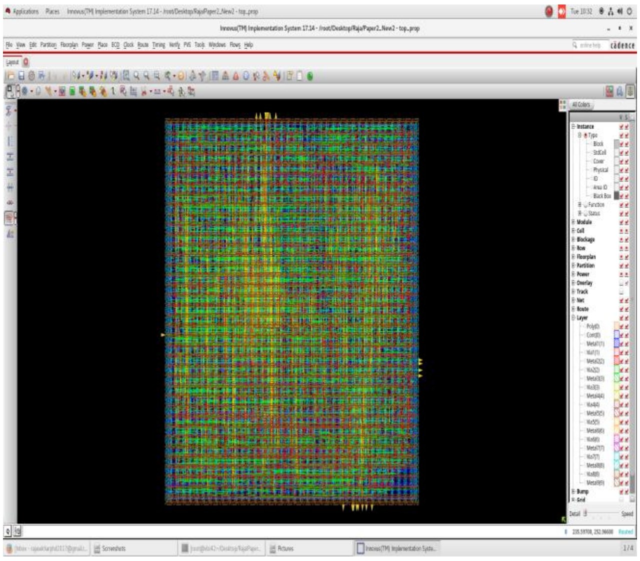
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Fig.6. Full Placement

We can select any cell in the design and press ‘Q’ for their properties.

D. Clock Tree Synthesis (CTS)

We can build a clock tree for CTS by selecting ‘ccopt clock tree debugger’ and this clock tree uses clock buffers and clock inverters for boosting up. Due to this balanced buffers and inverters rise time will be equal to fall time.

E. Routing

This is the final step in the physical design flow. In GUI, we select route>nano route>route and in the window we select timing driven and SI driven then each cell in the core is routed and we check the status of each net by pressing ‘Q’. The routing is shown in fig.7.

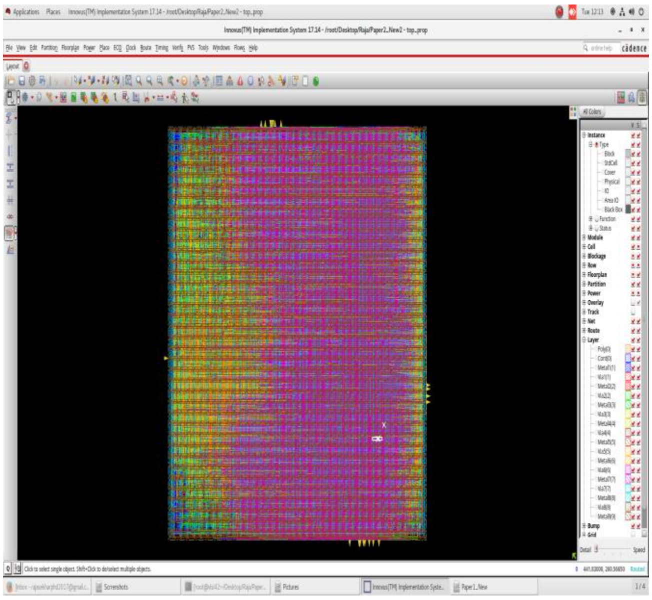
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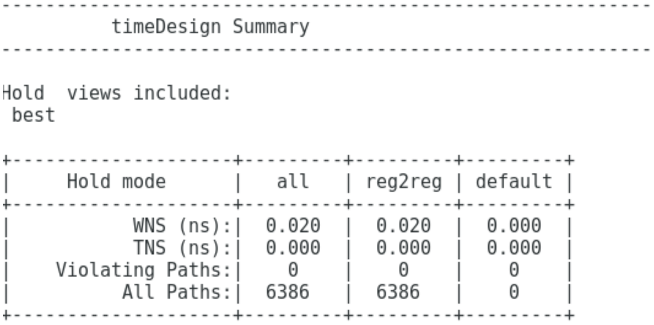
Fig.7 final routing stage

At each and every stage will take the reports of area and power. Timing report for both set-up and hold time can be obtained. Make sure that no violating paths in the design. The timing summary is shown below fig.8.



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------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 best

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.020  |  0.020  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  6386   |  6386   |    0    |
+--------------------+---------+---------+---------+
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Fig.8 Timing report of Hold time.

If there are any violating paths in the design then we optimize the design but due to the optimization area and power will be increased.

Area and power reports at the final step routing are shown in table I and II respectively.

Table I: Area report

90nm Tech	Cell count	Cell area (μm^2)
Area	11241	97646.155

Table II: Power report

90nm Tech.	Value
Cells	11241
Leakage	602877.719 nW
Dynamic	66317069.021nW
Total Power	66919946.740nW

VI. CONCLUSION

In this, initially we have designed Real FFT architecture with the use of only one dual port RAM and urdhva tiryagbhayam multiplier based on the radix-2 decimation-in-frequency algorithm using Verilog HDL. Further the architecture was implemented in Cadence Virtuoso with 90nm technology. Each step in the ASIC physical design flow was completed and we also optimize the design for zero violating paths. At final area, power and timing reports are taken from the cadence innovus tool.

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