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A new architecture for 8-bit Synchronous Counter using Clock Gating and Clock Buffer Network in 45nm CMOS Process

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Abstract: ***Counters play an inevitable role in many VLSI circuits like timers, frequency dividers, memories and ADC/DAC. Integrating timing discriminator, Pulse Swallow and Correlated double sampling are various approaches are used in counters for low power consumption. The main objective is to minimize low power consumption and device count. In this work, a novel clock gating approach is used in 8-bit synchronous counter to improve the performance of conventional counters in different VLSI systems. Clock gating circuit and clock buffer network pattern are used in the proposed algorithm to reduce the power consumption of synchronous counters. The counter gives three fold advantages namely unwanted clock activity of all T FFs are reduced and noise at the clock edges of the master clock is reduced and thereby leads to improvement in power, circuit complexity, and device count. CMOS 45nm technology is used for designing the proposed counter 1.5 supply voltage. Simulated results show the improvement of the proposed approach over other conventional counters in terms of power consumption and device count.***

Keywords— CMOS process, Low Power Consumption,8-bit Synchronous Counter

I. INTRODUCTION

SYNCHRONIZATION is required for activating all stages simultaneously in a circuit. The authors in [1] used embedded a clock gating in carry propagation circuit to minimize switching power and silicon area of their CMOS synchronous counter compared to conventional synchronous counters.

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A novel pipeline partitioning method is reported in [2] for improving the speed of digital parallel counter. It has counting path and state look ahead path and three modules namely first module to generate the counting states, D type FFs module and 2-bit counters module. A power efficient binary counter and the up-down counter are designed in [3].

In this work, power consumption in clock distribution is controlled by a novel combinational logic at the input of all FFs. Correlated double sampling (CDS) method [4] used to reduce the toggling operation in D FF. Thereby, power consumption is reduced, image quality degradation due to self heating and voltage drops in power rails can be reduced in CMOS image sensor (CIS) applications for the CDS counter.

A low power pulse swallow counter is simulated in 180nm technology [5]. It consists of a divide by 2/3 pre-scaler, a programmable counter to work in high frequency to reduce power consumption and a swallow counter. The programmable counter is designed to work in different frequencies. Quantum dot cellular automata (QCA) for synchronous counters are implemented in [6]. There are two types of QCA namely 45^{o} cells and 90^{o} cells. A level sensitive innovative idea with majority and inverter gates are designed for QCA in [6] and then it is converted from edge-level converter for the counters to reduce power consumption. A coulter counter which works on potential change detection is implemented in [7]. Microcells/particles are passed through sensing channel to obtain the potential change principle. Sensor arrays are required to obtain high throughput in coulter counter [7]. Countercurrent chromatograph works with 2D and 3D model in helical columns and provides better phase mixing [8]. Rather than the spiral column, the helical column gives centrifugal force and helps in the optimized design of helical columns. Scintillation counters along with comparator and multi-vibrator act as a precise time discriminator [9]. A normalized value of input is applied at the zero crossing point rather than a dynamic wide range of input to increase the precision of the scintillating counters. A synchronous control over the speed of rotors is analyzed in [10] by cross coupling and electromechanical dynamic coupling model. A correlated double sampling (CDS) approach was used in the parallel column of counters [11]. Two's complement arithmetic with 16 transistors is used and obtained 34% reduction in power consumption and 2.4 times improvement in speed of the counter. Deterministic algorithms with fast state-optimal characteristics are designed for synchronous counting [12].

The propositional satisfiability (SAT) problems are solved by either time-optimal algorithms or non-optimal algorithms. A low power parallel sampling technique which achieves delay resolution for counter assisted PLL is implemented in [13].

In this, 2 bit asynchronous counter and a 6 bit synchronous counter are combined to form a hybrid counter to operate at high speed above 4GHz frequency. CMOS analog counter with the programmable input voltage to produce proportional output with respect to input phase is designed in [14] for SPAD pixel arrays. It used high-resolution avalanche photodiode for image sensors to obtain a factor 3 improvement than the previous designs. Quantum synchronous counters (QSC) with direct mapping flip-flop designs and Quantum dot cellular automata (QCA) inherent characteristics are combined [15] to overcome long wire and area related constraints and to improve cost function and delay in QCA. Exponential smoothing and counter based algorithms are combined to form counter synchronization (C-Sync) in changing neighboring conditions in wireless sensor networks (WSN) [16]. Synchronization leads to the reduction in duty cycle thereby reducing energy consumption in WSN. A pre-amplifier with 12 channels is designed in ASIC for gas counters and avalanche photo diode [17]. Gain and Equivalent low optimum noise charge (ENC) are analyzed for the pre-amplifier.

An observation of the literature works reveals the scope for improvement in the architecture of synchronous counter. In this work, a modified clock buffer network is proposed for 8-bit synchronous counter. The novelty lies in the clock gating circuit and clock buffer network which uses three levels clock distribution from the master clock to the respective T FF stage to appropriately activate the single T FF to get the next count of 8-bit synchronous counter. Clock buffer network is changed suitably to eliminate the unwanted activity of all FFS all the time in the counter operation, remove noise in the clock edges of the master clock and thereby obtaining the substantial improvement in power, device count and circuit complexity for the synchronous counter. CMOS 45nm technology is used for designing the 8-bit counter and simulated results show promising results for the proposed approaches.

The rest of this paper is organized as follows: Section 2 deals with various conventional methods for counter design. Section 3 illustrates the proposed methodology for 8-bit synchronous counter. Section 4 describes the simulated results obtained for the proposed 8-bit counter and the comparison with other works. Section 6 concludes the work done.

II. CONVENTIONAL SYNCHRONOUS COUNTERS

A. Clock Gating embedded into Carry Propagation Circuit

The circuit diagram of Clock Gating embedded into Carry Propagation Circuit [1] is shown in the Fig1. A 16 bit synchronous counter is designed with 16 FFs and 4 local clock generators. It works on synchronous timing principle and conditional pulse. At each stage output of FF is given to local clock generator and its output is inverted and fed to the input of FF for toggling operation. The 16-bit synchronous counter is obtained by four sub-blocks where each sub block has 4 FFs and one local clock generator to maintain the speed and decrease the number of pass transistors required in the design. The speed of the counter decreases if more than five pass transistors are used in each sub-block. The clock gating counter is also compared with conventional non-clock gated counter and conventional clock gated counter where the device count decreased by 15% and power consumption is 64% by embedding the clock gating in carry propagation circuit. Redundant transitions are reduced in this method by decreasing the number of transistors in the design.

The Clock Cycle Time (T_{CYCLE}) of Clock Gating embedded into Carry Propagation circuit synchronous counter is

$$T_{CYCLE} \geq T_{D\_MAX} + T_{P\_MIN} + T_{CQ\_MAX} \quad (1)$$

T_{D_MAX} is the worst case propagation delay, T_{CQ_MAX} is the worst case clock. storage elements clock to output delay and T_{P_MIN} is the minimum pulse width.

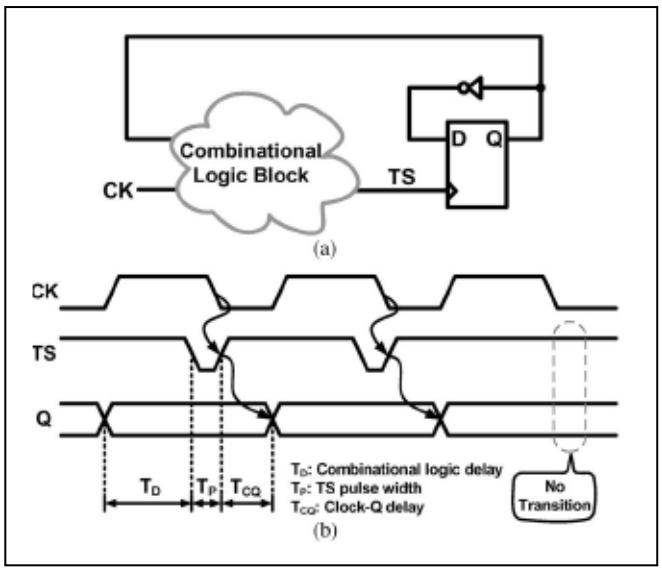

Fig. 1 Conditional pulse-based synchronous timing principle [1].

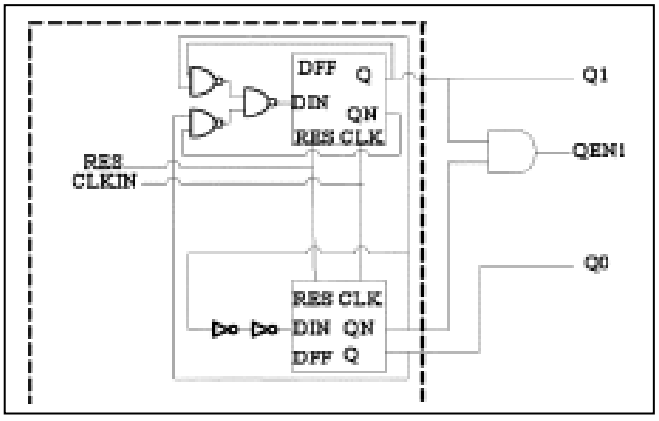

Fig. 2 Hardware schematic –

Counting path

B. State Look-Ahead based Digital Parallel Counter

Counting operations are done by the logic in counting path (shown in Fig2.) and look-ahead path generates future states and prepares the counting path for future counting [2].

Decoders in look-ahead path initiate the early overflow and state look-ahead logic is responsible for pipelining the early overflow detection. State equation for the counter is derived from early overflow pipelining equation.

The maximum allowable m-bit counter size (CS) is given by

$$CS = m + (2*(2m-1)) \quad (2)$$

The number of early overflow (EO) states is

$$EO = 2^m - 1 \quad (3)$$

The clock period (T_{CLKIN}) of 8-bit parallel counter with counting path and look-ahead path is given by

$$T_{CLKIN} > T_M + T_{AND} + T_{setup\text{-}hold} \quad (4)$$

Where T_M is the module access time, T_{AND} is the delay of AND gate and $T_{setup\text{-}hold}$ is the DFF setup time plus hold time. Pipelined counting path and state look-ahead path concurrently activates all modules and provides all counting states without rippling effects. The design avoids long chain detectors for larger width parallel counter. Increase in fan-out leads to drop in counter frequency at the rate of $\log_{6.5}N$ where N is the width of the parallel counter. The drop in the logarithmic frequency makes the parallel counter a faster counter. However, the area requirements and power requirements increase for each doubling of the clock frequency. In this design clock frequency is made independent of the width of the counter, thereby all modules are activated simultaneously by the clock frequency. The parallel counter has three modules separated by D FFs. The counter output is in radix-2 representation and can be read without any decoding process. The counter designed does not have any count latency as in other normal counters.

C. Clock Gating Cascaded T Flip-flop Synchronous Counter

A cascaded T FF arrangement which concentrates on the next state output is designed. Power contribution is controlled by properly designing the excitation of T FF [3]. Thereby power consumption during transitions of T FF output can be controlled. A clock buffer network with number of repeaters provides the master clock to all T FFs. This not only distributes the clock to all T FFs in the arrangement but also controls the clock skew. The clock buffer network has three fold advantages namely decreasing the load on master clock, the number of buffer levels is reduced and power dissipation is minimized. By placing an additional clock gating circuit consisting of OR gates, the logic is extended for the up-down counter. The design can also be extended to the digital block of successive approximation register type ADC.

The clock activation and input for T FF for up-down arrangement is given as below.

$$Clk_n = T_n . (Q_{n-1} + Q_{n-1}') \quad (5)$$

$$T_n = UP \prod Q_i + DOWN' \prod Q_j' \quad (6)$$

D. Correlated Double Sampling (CDS) Low Power Counter

The counter is proposed by D FF (master and slave). The output of master INT toggles in the conventional counter whereas in CDS counter by using an AND gate and pulse generator, the togging operation is controlled [4]. This technique reduces the power consumption by 50%. Multiplexers are used to provide up-down counting operation. Edge triggering is followed for D FFs in CDS low power counter for CMOS image sensor (CIS) applications. The single slope in Column-Parallel ADC provides digital CDS operation. The non-uniformities of CIS pixels and ADC leads to fixed pattern noise and can be reduced by digital correlated double sampling method.

A detailed investigation of counter obligates before considering the power reduction. This survey gives way for the deeper perspective of various approaches to cope up with power advancements in the fields. The counter investigation mandates the following parametric requirements that arise to be factors of consideration in various Problems related to counters as discussed below in Table 1. Evolutionary approaches such as correlated double sampling and look-ahead path in addition to counting path are used for counters in circuit complexity problems. But, the power consumption is very large in those approaches compared with other algorithms. In our work, an improved clock gating and clock buffer network from master clock is proposed and simulated using CMOS 180nm technology. In this design, a 3 level buffer network is proposed to distribute clock for each T FF stage in 8-bit counter. These methods save power than the other conventional schemes without clock gating.

Table1. Various Techniques in Synchronous counters

Technique used	Switching Power	Area/ Device Count	Latency	Technology
Clock gating embedded in Carry propagation circuit[1]	Minimized	Minimized	-	180nm
Pipeline methodology with counting path and look-ahead path[2]	Increases	Increases	Minimized	180nm
Cascaded Structure of T FFs, Clock Buffer Network[3]	Low	Minimized		45nm
Correlated Double Sampling, Column- Parallel CMOS, 2's complement arithmetic[4]	Low	-	Reducing toggling, Speed increases	180nm
N Pulse Swallow Counter[5]	Low	-	High Frequency	180nm
Quantum dot Cellular Automata counter[6]	Low	More	High Speed	-
Coulter Counter[7]	-	-	High throughput	-
Scintillating Counter with integrating timing discriminator[9]	-	-	Time walk 200ps	180nm
Fractional N counter Assisted PLL[13]	Low	Jitter Less	High Speed	65nm
Programmable Voltage Step[14]	Low	Low	High spatial resolution	350nm
12 Channel Pre-amplifier shaper[17]	Low	-	Low noise charge	350nm

III. PROPOSED METHOD

In this work, cascaded structure of T FFs for the core functionality of the counter is proposed. Transmission gate FFs are used in the design. A control transistor and AND gate works as an efficient combinational circuit for clock gating of the FFS in the proposed synchronous counter to obtain the substantial gain in power consumption. In conventional counters, D FFs are used to latch input state to output state. But, in the proposed counter T FF concentrates on the activity of the next state output.

Power consumption occurs at both T=0 and T=1 transitions of the T FF in which the power consumption of T FF at T=0 is eliminated by properly designing the characteristic function of T FF. This controls the clock of the counter and hence for low power consumption T FF is a preferred choice in synchronous counters.

This combinational circuit with control transistor and AND gate act as the clock gating for the counter. The master clock is controlled by the control MOS transistor which in turn is activated by the preceding FFs.

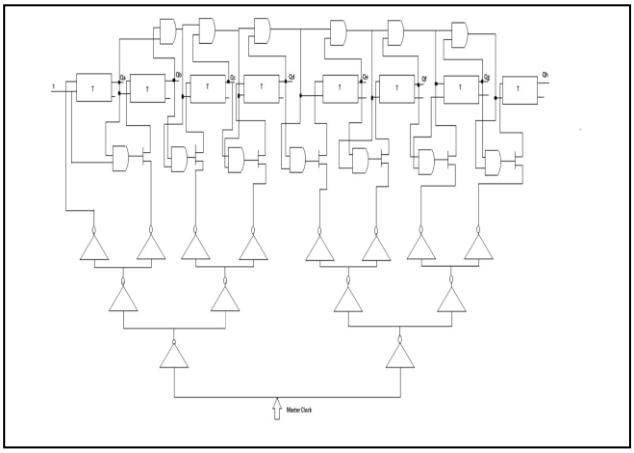

Fig.3 Block diagram of 8-bit counter

The block diagram of the proposed 8-bit counter is depicted in Fig 3. TA, TB, TC, …. TH are the 8 stages T FFs in the counter. The AND gates from 1 to 7 take inputs from the previous stage output and next stage input clk respectively. i.e. AND1 inputs are from FF1 output and TB clk input, AND2 inputs are from FF2 output and TC clk input, AND3 inputs are from FF3 output and TD clk input, AND4 inputs are from FF4 output and TE clk input, AND5 inputs are from FF5 output and TF clk input, AND6 inputs are from FF6 output and TG clk input, AND7 inputs are from FF7 output and TH clk input. The active condition of the clock and the respective FF status is given in Table2 and Table3 for all 256 states of the counter.

The clock gating is introduced by MOS transistors with the high threshold by which any unwanted electrostatic charges can be eliminated. Hence the clock equations for each stage in the proposed 8-bit counter is given by

$$Clk_2 = T_1 . Q_1 \quad ; \qquad Clk_6 = T_5 . Q_5$$
$$Clk_3 = T_2 . Q_2 \quad ; \qquad Clk_7 = T_6 . Q_6$$
$$Clk_4 = T_3 . Q_3 \quad ; \qquad Clk_8 = T_7 . Q_7$$
$$Clk_5 = T_4 . Q_4 \quad ; \qquad T_{i+1} = Q_i . Q_{i-1}$$

(7)

Table 2 Flip-flop active transitions (count: 0 to 127) for 8-bit counter

Output	Active FF	Output	Active FF	Output	Active FF	Output	Active FF
00000000	FF 1	00100000	FF 1	01000000	FF 1	01100000	FF 1
00000001	FF 2	00100001	FF 2	01000001	FF 2	01100001	FF 2
00000010	FF 1	00100010	FF 1	01000010	FF 1	01100010	FF 1
00000011	FF 3	00100011	FF 3	01000011	FF 3	01100011	FF 3
00000100	FF 1	00100100	FF 1	01000100	FF 1	01100100	FF 1
00000101	FF 2	00100101	FF 2	01000101	FF 2	01100101	FF 2
00000110	FF 1	00100110	FF 1	01000110	FF 1	01100110	FF 1
00000111	FF 4	00100111	FF 4	01000111	FF 4	01100111	FF 4
00001000	FF 1	00101000	FF 1	01001000	FF 1	01101000	FF 1
00001001	FF 2	00101001	FF 2	01001001	FF 2	01101001	FF 2
00001010	FF 1	00101010	FF 1	01001010	FF 1	01101010	FF 1
00001011	FF 3	00101011	FF 3	01001011	FF 3	01101011	FF 3
00001100	FF 1	00101100	FF 1	01001100	FF 1	01101100	FF 1
00001101	FF 2	00101101	FF 2	01001101	FF 2	01101101	FF 2
00001110	FF 1	00101110	FF 1	01001110	FF 1	01101110	FF 1
00001111	FF 5	00101111	FF 5	01001111	FF 5	01101111	FF 5
00010000	FF 1	00110000	FF 1	01010000	FF 1	01110000	FF 1
00010001	FF 2	00110001	FF 2	01010001	FF 2	01110001	FF 2
00010010	FF 1	00110010	FF 1	01010010	FF 1	01110010	FF 1
00010011	FF 3	00110011	FF 3	01010011	FF 3	01110011	FF 3
00010100	FF 1	00110100	FF 1	01010100	FF 1	01110100	FF 1
00010101	FF 2	00110101	FF 2	01010101	FF 2	01110101	FF 2
00010110	FF 1	00110110	FF 1	01010110	FF 1	01110110	FF 1
00010111	FF 4	00110111	FF 4	01010111	FF 4	01110111	FF 4
00011000	FF 1	00111000	FF 1	01011000	FF 1	01111000	FF 1
00011001	FF 2	00111001	FF 2	01011001	FF 2	01111001	FF 2
00011010	FF 1	00111010	FF 1	01011010	FF 1	01111010	FF 1
00011011	FF 3	00111011	FF 3	01011011	FF 3	01111011	FF 3
00011100	FF 1	00111100	FF 1	01011100	FF 1	01111100	FF 1
00011101	FF 2	00111101	FF 2	01011101	FF 2	01111101	FF 2
00011110	FF 1	00111110	FF 1	01011110	FF 1	01111110	FF 1
00011111	FF 6	00111111	FF 7	01011111	FF 6	01111111	FF 8

Clock buffer network is designed to apply clock to individual stage of the proposed counter with the help of a master clock. This clock buffer network supplies the clock to the clock gating circuit which minimizes the clock skew of the entire counter. Clock buffer network along with the clock gating circuit reduces the power consumption of the proposed 8-bit counter.

Table3 Flip-flop active transitions (count: 128 to 255) for 8-bit counter

Output	Active FF	Output	Active FF	Output	Active FF	Output	Active FF
10000000	FF 1	10100000	FF 1	11000000	FF 1	11100000	FF 1
10000001	FF 2	10100001	FF 2	11000001	FF 2	11100001	FF 2
10000010	FF 1	10100010	FF 1	11000010	FF 1	11100010	FF 1
10000011	FF 3	10100011	FF 3	11000011	FF 3	11100011	FF 3
10000100	FF 1	10100100	FF 1	11000100	FF 1	11100100	FF 1
10000101	FF 2	10100101	FF 2	11000101	FF 2	11100101	FF 2
10000110	FF 1	10100110	FF 1	11000110	FF 1	11100110	FF 1
10000111	FF 4	10100111	FF 4	11000111	FF 4	11100111	FF 4
10001000	FF 1	10101000	FF 1	11001000	FF 1	11101000	FF 1
10001001	FF 2	10101001	FF 2	11001001	FF 2	11101001	FF 2
10001010	FF 1	10101010	FF 1	11001010	FF 1	11101010	FF 1
10001011	FF 3	10101011	FF 3	11001011	FF 3	11101011	FF 3
10001100	FF 1	10101100	FF 1	11001100	FF 1	11101100	FF 1

10001101	FF 2	10101101	FF 2	11001101	FF 2	11101101	FF 2
10001110	FF 1	10101110	FF 1	11001110	FF 1	11101110	FF 1
10001111	FF 5	10101111	FF 5	11001111	FF 5	11101111	FF 5
10010000	FF 1	10110000	FF 1	11010000	FF 1	11110000	FF 1
10010001	FF 2	10110001	FF 2	11010001	FF 2	11110001	FF 2
10010010	FF 1	10110010	FF 1	11010010	FF 1	11110010	FF 1
10010011	FF 3	10110011	FF 3	11010011	FF 3	11110011	FF 3
10010100	FF 1	10110100	FF 1	11010100	FF 1	11110100	FF 1
10010101	FF 2	10110101	FF 2	11010101	FF 2	11110101	FF 2
10010110	FF 1	10110110	FF 1	11010110	FF 1	11110110	FF 1
10010111	FF 4	10110111	FF 4	11010111	FF 4	11110111	FF 4
10011000	FF 1	10111000	FF 1	11011000	FF 1	11111000	FF 1
10011001	FF 2	10111001	FF 2	11011001	FF 2	11111001	FF 2
10011010	FF 1	10111010	FF 1	11011010	FF 1	11111010	FF 1
10011011	FF 3	10111011	FF 3	11011011	FF 3	11111011	FF 3
10011100	FF 1	10111100	FF 1	11011100	FF 1	11111100	FF 1
10011101	FF 2	10111101	FF 2	11011101	FF 2	11111101	FF 2
10011110	FF 1	10111110	FF 1	11011110	FF 1	11111110	FF 1
10011111	FF 6	10111111	FF 7	11011111	FF 6	11111111	FF 8

IV. RESULTS AND DISCUSSION

Synthesis and simulation results for the 8-bit synchronous counter designed in 45nm CMOS process is depicted in Fig4. Functional verification using HDL representation and performance verification using Cadence Virtuoso simulation of our synchronous counter is shown in Fig5. The NMOS transistors in the proposed 8-bit counter are designed with W/L as 120nm/45nm.

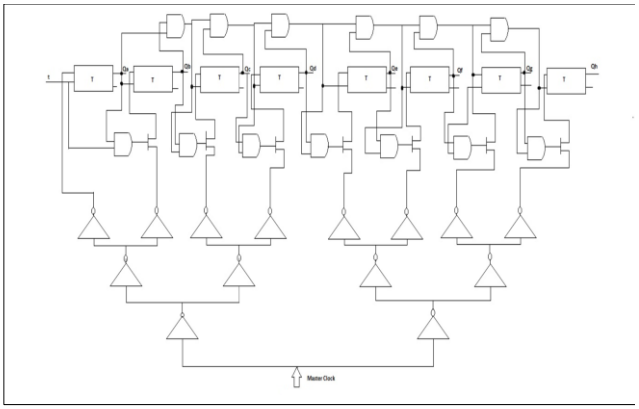

Fig. 4 Schematic of 8-bit counter

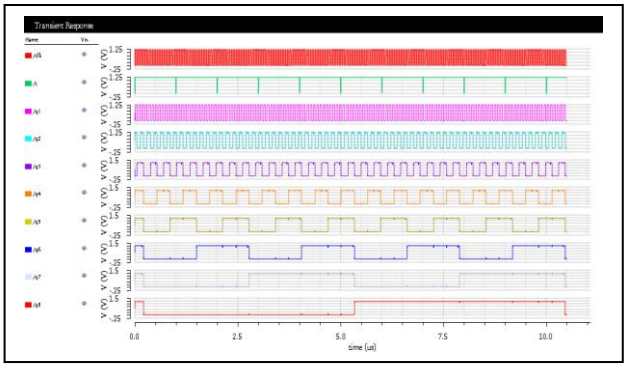

Fig. 5 Simulation of 8-bit Counter

The simulation result is shown in Fig5. For the proposed 8-bit counter is performed using HSPICE with a supply voltage of 1.5 V at room temperature with process parameters of frequency 1GHz and observed a power consumption of 69.07µW. The master clock supplies the clock to all stages of T FF in the 8-bit counter through clock buffer network. This technique activates only the required T FF stage to generate the next counter state output as depicted in Table2 and Table3. For next count 00000010 in the proposed counter, FF2 clock is provided from the master clock and appropriately FF2 comes to active condition. Similarly for next count to be 00100000 in the proposed counter FF6 clock is provided from master clock via clock buffer network and appropriately FF6 comes to active condition. But this methodology all T FFs need not be active all the time and hence power consumption of the proposed 8-bit counter is reduced.

The proposed counter is simulated for various supply voltages from 0.8V to 1.5V and the respective power consumption is shown in Table4. As the VDD value is increased the power consumption also increases in the 8-bit counter with clock gating circuit and clock buffer network connected to a master clock to activate appropriate T FF for sequential counting.

Table4. Simulated Results for Proposed 8-bit Counter

VDD (V)	Power Consumption
0.8	337.8nW
0.9	714.1nW
1.0	2.123µW
1.1	5.76µW
1.2	12.06µW
1.5	69.07µW

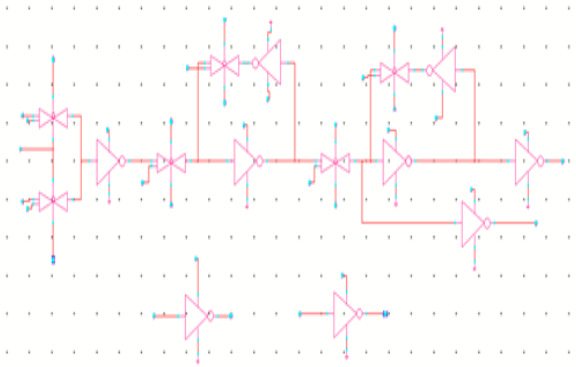

Fig.6 Schematic of each Flip- flop using transmission gates

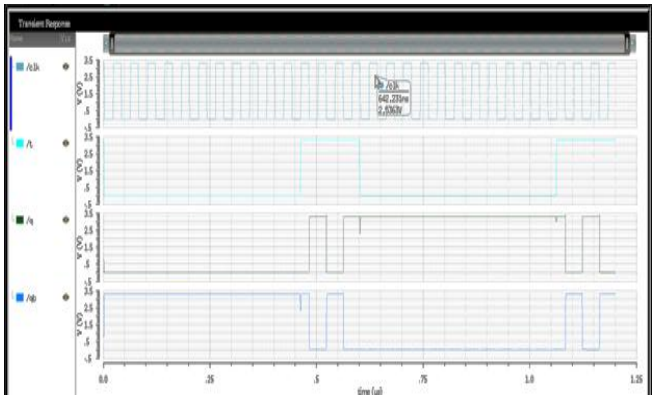

Fig.7 Simulation of each Flip flop

Thus the master clock which drives the 8 stages of T-FF offers three fold advantages in the proposed synchronous counter. For 8-bit counter, it needs 3 level clock buffer networks as repeaters to activate the respective T-FF for the next state count of the counter. By this technique, the edge rates of the clock are avoided at the input of the clock gating network. This, in turn, reduces the noise at rise time and fall time of the clock. The combination of clock buffer network and clock buffer network act as the combinational network to reduce the power consumption at all stages of T-FFs are not active all the time. By multi-level clock buffer network, power optimization takes place in the proposed 8-bit clock gating synchronous counter. Thereby unwanted flip-flop clock activity is reduced, device overhead is reduced and circuit complexity is reduced. Fig. 6 shows the internal schematic of each stage T FF using transmission gates. Fig.7 shows the output waveform of T FF using transmission gates.

V. PERFORMANCE COMPARISON OF VARIOUS SYNCHRONOUS COUNTERS

The comparison for power consumption and device count of various counters is shown below. The results show that conventional counters with clock gating technique show reduced device count overhead compared with conventional counters with non- clock gating. Meanwhile, the proposed counter provides a significantly reduced power consumption and device count.

Table5. Comparison of our proposed 8-bit Counter with other works

Work	Technology	VDD (V)	Power Consumption	Device Count
Saleh et.a l [2]	150nm	1.5	13.89mW	510
Alioto et.al [18]	180nm	1.8	2.21mW	160
Kakarountas et.al [19]	600nm	5	21.3mW	286
Yeh et.al [20]	150nm	1.5	7.64mW	373
Proposed Counter	45nm	1.2 1.5	12.06µW 69.07µW	- 346

In the proposed counter, the clock buffer network is efficiently merged with clock-gating logic for better performance. There is the substantial improvement in power consumption as compared with conventional counters with no clock gating. Table5 shows the comparison results for the power consumption of various counters. Among counters designed with different FFs, the proposed counter with T FFs provides comparative power consumption reductions than many other conventional clock-gated and non-clock-gated counters.

VI. CONCLUSION

In this work, a novel clock gating technique is proposed for the synchronous counter. It is a fusion of clock gating network with clock buffer network. Master clock is driven by three levels of repeaters for the 8-bit counter. The clock gating technique in the synchronous counter is introduced with an objective to obtain the benefits of minimum power consumption and device count in synchronous counters. The proposed 8-bit counter at 1.5V supply consume a power of 69.07µW in 45nm CMOS Process. Simulated results show significant positive results for the proposed 8-bit synchronous counter. Proposed clock gated 8-bit counter is much efficient than many of the conventional counters with and without clock gating circuit and may be used in many data-path applications.

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