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Implementing Logical Circuits with Four Phase Quantum Dot Cellular Clock using QCA Designer

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Abstract*: Quantum Dot Cellular Automata (QCA) is treated as a most promising technology after CMOS techniques. The major advantages of QCA techniques are faster speed, lower energy consumption and smaller size. The implementation of clocks play very big role in the effective design of QCA circuits. In this paper, a QCA circuit is designed using the concept of QCA clocks. The proposed study describes a new method of implementing the logical function with power depletion analysis. The proposed logical function uses total number of 57 cells in which the area of each cell 372 nm2. The energy dissipation in this implementation is 18.79 meV and the total acquired area is 0.192 µm2. The proposed circuit is implemented utilizing QCA Designer. The proposal is excellent in the realization of nano-scale computing with minimal power utilization. The results are compared with the existing approaches and improvements of 6% in the area required and 7% in the number of cells are achieved.

***Keywords*: QCA, Single Electron Tunneling (SET), Complementary Metal-Oxide-Semiconductor (CMOS), QCA Designer, Tunnel Phase Logic (TPL)**

I. INTRODUCTION

Initially, CMOS technology was very popular in the manufacturing of Integrated Circuits (ICs) which includes micro-processor, micro-controllers, memory chips (CMOS-BIOS) etc. CMOS is basically a type of MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistors) fabrication process [1]. To overcome with the problems of the CMOS technology, various nano-scale technologies have been developed. One of the important nano-scale technology is Single Electron Tunneling (SET) [2,3]. In this technique, the charge existing on a capacitor is not quantified. There exist polarization charges which are created by displacing the electron gas considering positive lattice ions and can acquire arbitrary magnitudes. One of the other important techniques is Tunnel Phase Logic (TPL) [4]. In this technique, phase locking of electron tunneling is used in ultra small junction by the device. QCA technique is also a very promising nano-technology in this regard [5, 6, 7]. QCA works on the theory of columbic communication of electrons which are in quantum dots under trapping condition.

The concept of clocks plays vital role in QCA circuits development [8]. The advantages include faster speed, lower energy consumption and smaller size.

The clocking fields can be used for clocking the molecular QCA. It can be implemented using an array of conductors [9] which is further used to determine the flow of data and calculations. Another advantage of using QCA clocks is to provide power gain for strengthening weak signals, enabling latching and permits adiabatic operations [10-11]. Also, the clocks must be designed in accordance to consume very less power. It is one of the important design parameters for designing the circuits.

The paper has 6 sections. Section I is the introduction and Section II is concerned with related work. The introduction about clocking concept in QCA circuits is given in Section III. Section IV is the implementation of the proposed model supported with a discussion on result analysis in Section V. The conclusion and future scope are addressed in section VI.

II. RELATED WORK

Several implementations are carried out in the development of QCA technology. A new approach of designing XOR gate using QCA technology is proposed and implemented in [12]. The proposed approach is found competitive with other approaches in terms of latency, area, cell count and complexity. The approach is implemented using QCA designer and QCA Pro.

Similarly JK, T and D flip flop circuits are implemented using a derivated formulation (expression) of SR flip flop in [13]. The robustness of the flip flop is calculated in terms of Kink Energy and Energy dissipations. The application of partially reversible pipelines is demonstrated for designing energy efficient QCA circuit in [14]. A new coplanar design of Full Adder/ Substractor using QCA technology is proposed in [15]. An improvement in occupation area is done by implementing a new technique using reversible ALU using QCA in [16]. 28% of reduction in cell count and 51% in area is noted in this work. The major role of clocking [23] is to control the flow of data and calculations. In [17], it is shown that the molecular QCA control results into enabling the feedback loops, versatile circuit grid and the support of feedback and memories.

A coplanar QCA full adder is studied and implemented in [18] for low energy dissipation. The efficient 3 input XOR gate are implemented as a coplanar QCA technique in [19]. This approach basically implements 4 bit QCA Ripple Carry Adder.

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A single clock zone based carry propagation delay and radix 8 full adder is implemented in [20] using QCA. The issue of power dissipation is addressed in [21] by implementing an even parity generator circuit.

The parameters; cell counts, area and power consumptions are addressed in this implementation. D flip flop and memory structures are implemented in [22, 23] with efficient and dense QCA design.

An aluminum tunnel junction based single-electron transistor technology has been used to develop QCA circuits in [25]. A concept of dual phase clocking is implemented in [24] for improving line based QCA memory cell.

QCA technology is used in [25] for designing the full adder using QCA Designer Simulation Tool. Further the full adder is used for the implementation of three sizes of Ripple Carry Adders with acceptable number of results.

A new QCA based technique for implementing non-restoring divider is presented in [26] which are further used to implement coplanar QCA exclusive –OR gate and full adder. The parameters for the result analysis are cell count, latency and area.

III. QCA CLOCKS AND LAYERED ARCHITECTURE

In a QCA architecture, the most important component is a Four-Dot QCA Cell where a total of four quantum dots are settled which results into the development of a square. Subsequently, these Quantum Dots are considered as a small semiconductor.

Using electron tunneling two electrons can be loaded into the cell and can move from one quantum dot to another.

Columbic repulsion is the reason for electrons to occupy only the (Fig. 1) opposite QCA corners of the cells which results into two specific polarization states.

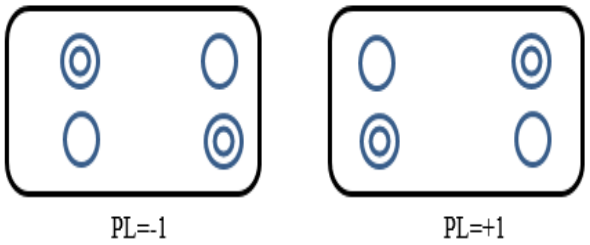

Fig. 1 Two stable configuration states in a QCA Cell for free electrons (Polarizations) [6]

Potential barriers will completely control the electronic tunneling and which will be managed by capacitive plates.

The concept of clocking in QCA follows the rule of multi-phased. Further an every QCA cell is not timed individually and the extraordinary wiring is required for every clock cell (Fig. 2). However, it is suggested to subdivide an array of QCA cells into number of sub arrays which resulted into the benefits of multiphase clocking and pipelining.

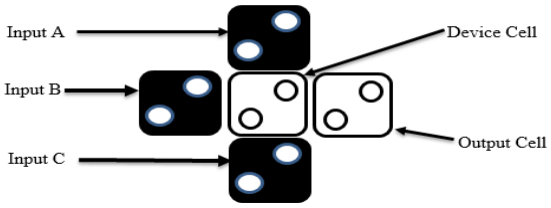

Fig. 2 QCA Logical Device [6]

This is important for each sub array, the inter dot barriers in all cells of array modulates a single potential.

It is important to consider that during the stage of computation, the successor arrays are set to un-polarized states, which are resulted into passive participation in the computation.

Further, there are four QCA phase clock [9] (Fig. 3).

1. First Clock Phase- Switch Phase

QCA cells start to be un-polarized and further the concerned inter dot potential barriers are going to reduce. This is basically the phase of actual computation where the barriers are considered to be low.

The barriers become high enough to compress cell states and electron tunneling at the end which is fixed.

2. Second Clock Phase-Hold Phase

The barriers are set to high which results into inputs which are further used in the next stage.

3. Third Clock Phase – Released Phase

On this stage, the barriers are treated to be lowered and cells are allowed to relax to an unpolarized state.

4. Fourth Clock Phase – Relax Phase

In this stage, cell barriers reduced to be lowered and cells sustains in an unpolarized state.

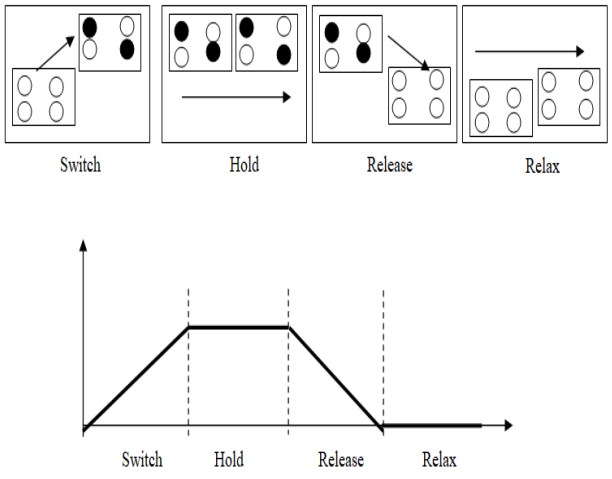

Fig. 3 The concept of QCA Clock [9].

IV. EXPERIMENTS AND RESULT ANALYSIS

The methodology of the work is as follows,

1. Identification of logical function
2. Implementation using QCA Designer

3. Analysis of the concerned outcomes
4. Comparison with other approaches and finalizing the findings.

The implementation of clocking is done by dividing the adjacent cells into number of groups. Following logical function is implemented using QCA Designer.

$$F = AB + A'B' + A'B$$

The QCA designer is the tool for rapid and accurate simulation of QCA based electronic circuits. The default experimental parameters are as follows for QCA Designer.

Table Isimulation Para Meters Of A Qca Designer

Simulation Parameter	Value
Value of Cell size	18nm
Value of Convergence of tolerance	0.0000100
Radius of effect	65.000000nm
Relative permittivity	12.900000
Value of Clock high	9.800000e-022J
Value of Clock low	3.800000e-023J
Value of Clock shift	0
Value of Clock Amplitude Factor	2.000000
Value of Layer separation	11.500000
Value of Cell size	18nm

The above logical function is implemented and simulated on the QCA Designer which is shown in the Fig. 4. In this implementation 5 majority gates are used for generating the required output. The desired simulation results are expressed in Fig. 5, 6 and 7.

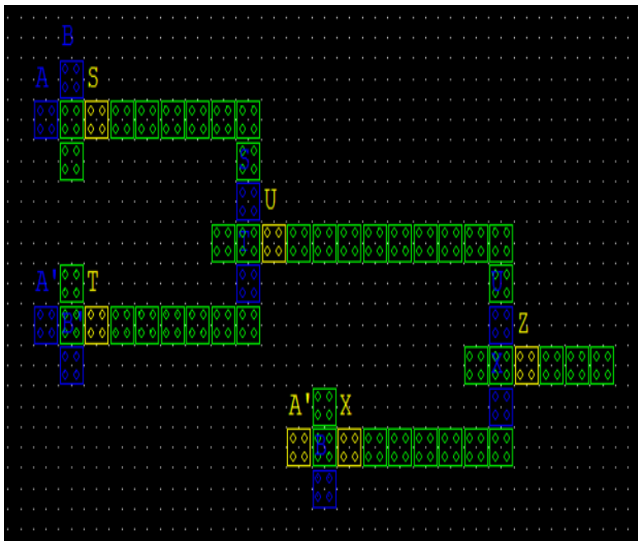

Fig. 4 QCA Circuit using QCA Designer

The simulation has been done and results are given in Table II.

Table II Results of Simulation

Parameters	Values
Total Number of Cells	57
Each Cell Area	324 nm^2
Space between Cells	2 nm
Total area*	0.192 micro-meter^2

Total area = Number of cells Size of each cell +gap area

Fig. 5 Simulation Result 1 from QCA Designer

Kink Energy [27] is calculated as the difference between two adjacent cells' energy. This energy depends on the measurement between two cells.

The Kink Energy is calculated as follows,

$$KE = P\frac{R_1 * R_2}{s} \quad \text{.....(1)}$$

Here, *KE*=Kink Energy.

P is a constant which is calculated using the Eq. (2).

$$P = \frac{1}{4\pi\varepsilon_0} = 9*10^9 \quad \text{.....(2)}$$

R_1 and R_2 are denoted as electronic charges and *s* is the distance measured between them.

Hence *KE* is calculated as follows,

$$KE = \frac{23.04\times10^{-29}}{s} \quad \text{.....(3)}$$

The KE for different values of *s* are given in Table III.

Table III Kink Energy Values

Value of *s*	Value of KE
2 nm	1.15 × 10^{-20} J
4 nm	5.76 × 10^{-20} J
6 nm	3.84 × 10^{-20} J

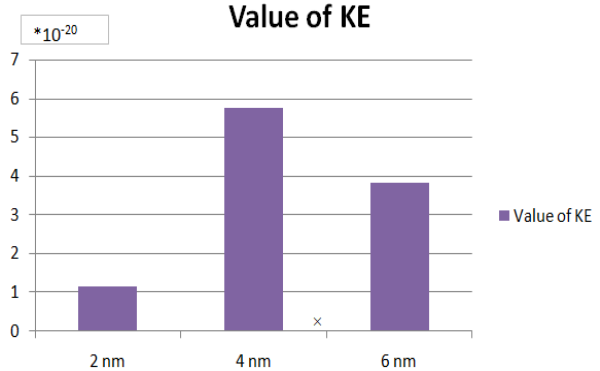

Fig. 6 Kink Values

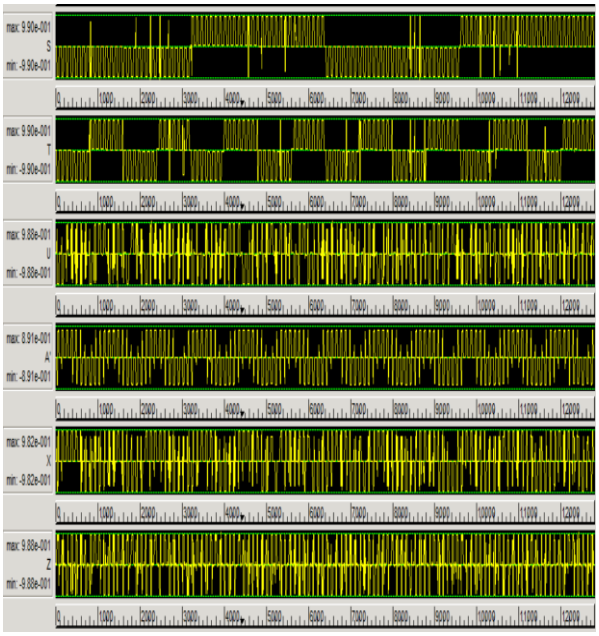

Fig. 7 Simulation Result 2 from QCA Designer

The implementation is also compared with the designed strategy as given in [34]. It is found that there is an improvement of 6% in the area required and 7% in the number of cells. In this implementation the area was 0.203 μm^2 as per the simulation results of the QCA Designer.

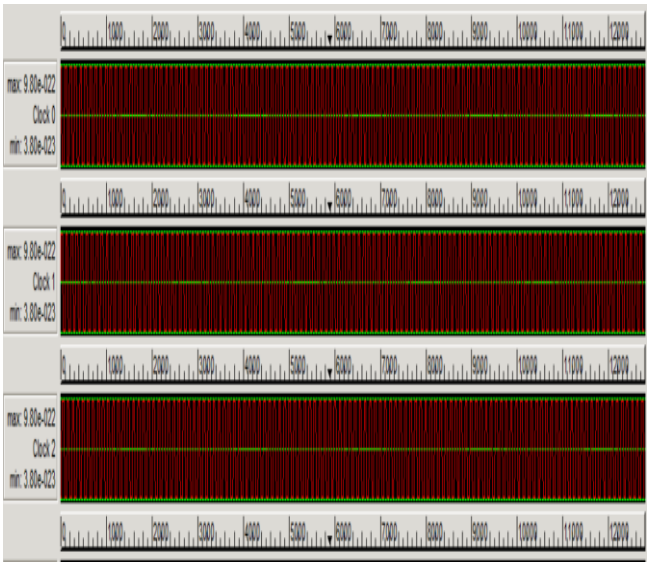

Fig. 8 Simulation Result 3 from QCA Designer

V. DISCUSSION

The number of cells, approximate area and latency in clock cycle are the important parameters to analyze the results of our experimentation with existing techniques.

Comparative results are shown below in Table III.

TABLE IV Comparative Result Analysis

Other Approaches	Number of Cells	Approximate Area (μm^2)
Approach 1 [11]	77	0.0878
Approach 2 [12]	125	0.105
Approach 3 [34]	150	0.203
Proposed Approach	57	0.192

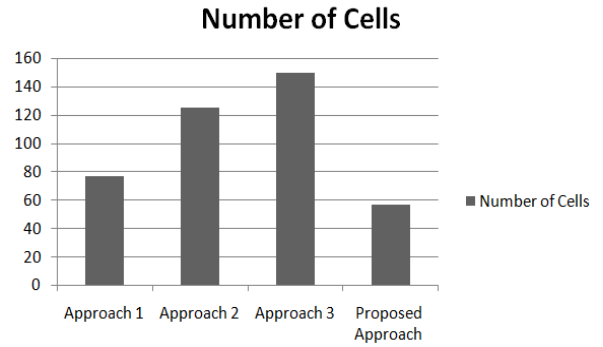

Fig. 9 Comparative Chart for number of cells

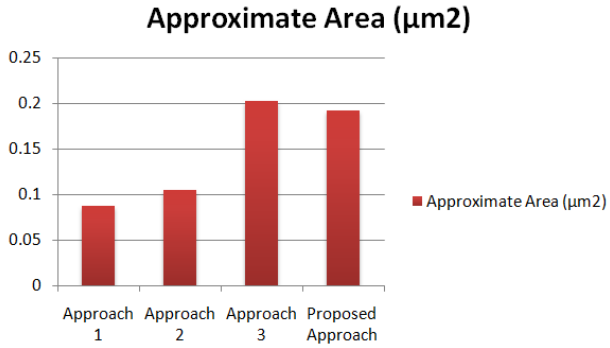

Fig. 10 Comparison Chart for Approximate Area

The proposed approach is proved to be better in number of cells and approximate area including clock cycle as per above comparative result analysis. Also total power consumption is 18.79 meV which is less power consumption in the proposed implementation compared to other.

VI. CONCLUSION

The design and implementation of sequential and combinational logic circuits is presented in this paper. The implementation has been done with four clocking zones. The crossover and multilayer design is examined. The implementation of proposed logical circuit uses 57 cells in the QCA Designer. The approximated area in the implementation is 0.192 μm^2 which is better than the other results in the comparative analysis. Total power consumption is 18.79 meV in the design of proposed logical circuit.

The shortcomings of the QCA technology are operating frequency issue and the estimation of actual propagation delay. The optimization of proposal can be done in terms of the complexity parameter and count of clock zones. In future, we are interested to design a evolutionary multi-objective optimization system for designing QCA systems with optimized parameters.

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