Enhancement of Commercial Grade VLSI Chips into Industrial Grade using a Novel Thermal Monitoring and Control Technique

Sachin Magadum, Hansraj Guhilot

Abstract: ***The aerospace and military applications demanding low cost, high performance, reliable computing chips at low operating temperature environment. In the proposed work a cost-effective solution has developed with novel mechanism to enhance use of commercial grade VLSI chips for industrial grade applications. Here the commercial grade FPGA worked satisfactorily beyond its lower temperature range typically up to -15°C. A thermoelectric cooler is used for temperature grade extension along with temperature sensor and TDC. A fully digital onchip temperature sensor based on delay line is implemented on FPGA. The TDC used, provides a digital equivalent of variation in delay due to change in temperature with time resolution of 213ps and temperature resolution of 0.06°C throughout the operating range.***

Key words: Commercial grade, Industrial grade, Onchip Sensor, FPGA, TDC, TEC

I.INTRODUCTION

Thermal management plays a vital role in the field of VLSI due to high density of transistors, complexity of system, speed grade, power dissipation and ambient environment. Design, implementation and deployment of critical thermally sensitive applications require a better thermal management system to prevent the chip from damage. The commercial grade VLSI chips have a limitation on operating temperature from 0ºC to 85ºC and the industrial grade VLSI chips have operating temperature range of -20ºC to 125ºC [1],[2]. The industrial grade VLSI chips are expensive compared to commercial grade chips. But as per the datasheet [2], except operating temperature range, all AC and DC electrical parameters are same for a particular speed grade commercial and industrial FPGAs. The maximum and minimum temperature ranges are set by manufacturers during testing and validation phase of chips. However, an application needs to operate beyond the specified lower temperature range, then the chip must replace with a higher-grade. This makes the system expensive in terms of economic and engineering effort though existing chip is providing ample amount of on-chip resources.

Chips fabricated from same wafer exhibit variation in parameters. Hence the process of testing and validation decides feasibility, quality, reliability and durability of chips. Therefore, industrial and defence grade chips undergo the process of testing and validation to guarantee the faithful performance of chips at a specified temperature range. While assessing the chip performance, many factors like best and worst case

timing information, density of transistor, transistor to transistor delay and cell to cell delay are considered for verifying operating temperature characteristics. But the commercial grade chips do not guarantee satisfactory performance beyond temperature range. If an FPGA part is operated outside it's allowed temperature range, then it creates timing failures. At low temperature silicon tends to work faster but affects static timings and many other parameters and chip may malfunction. Hence, it is not feasible to target less than or equal to 0ºC temperature to meet high speed. If an application demands to reduce temperature range further, then the only option available is extended temperature range with speed grade limitations in this part version.

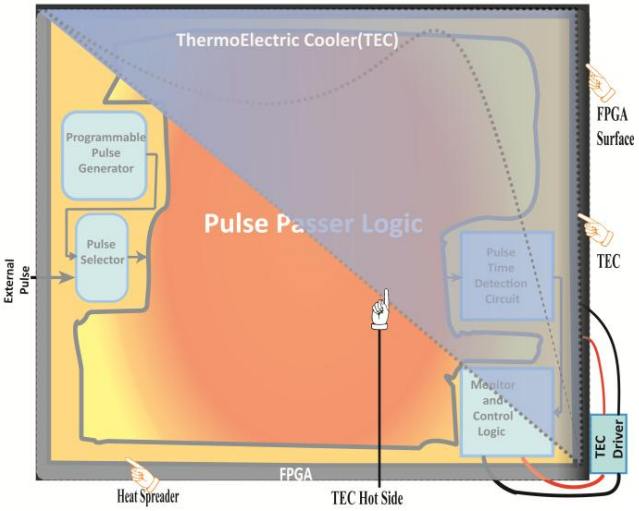

Fig.1. The proposed mechanism of enhancement of commercial grade FPGA into industrial grade

Another important observation is that most components tolerate low temperature and exhibit negligible loss in characteristics. The transistor at low temperature exhibits increased gain, high speed, low leakage, low parasitics in interconnection, reduced noise and improved heat transfer. Apart from all these harmonies, there are some specifics that should be accepted at low temperature with respect to the FPGA. They are as follows: There may be a crack in plastic packages and on-board SMCs due to low or differential temperature during power on, violation of minimum timing requirements and the problem of condensation.

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The low temperature impacts oscillator frequencies inside VLSI chips or FPGA. Other than these, most of the modern chips come up with Ball Grid Array (BGA) package. The detaching of BGA chip from the PCB for replacement and reattaching industrial grade BGA chips on board is a tedious task. This process requires expertise, dedicated equipment and is time consuming. Hence it is not feasible to use commercial and industrial grade chips in a different operating temperature environment alternately. However many researchers have proposed different methods to cooling the chips at high temperature. The author [3] suggested to use heatsink, heat pipes, solid state materials to manage the temperature of chip in his review paper. The method of reducing the temperature of chip with heatsink, heat pipes and thermal interface material(TIM) reported in [4,5]. The design of solid state cooling devices for cooling VLSI is proposed in[6]. The use of thermoelectric cooler(TEC) to cool the chip is reported in[7]. The double side cooling of chips to restrict chip temperature within the specific range of positive side is depicted in [8]. The use of TEC for cooling electronics in 3D with heat spreader is shown in [9]. In [8,9] heat dissipation at the other side of the TEC is managed with heat sink and heat dissipation mechanism. All mentioned techniques, moreover extending the operating temperature of chip at positive extreme end. However commercial grade chips' temperature range could be extended below 0°C with an appropriate mechanism.

In the presented work, a methodology is developed to enhance the lower operating temperature range of commercial grade chips into industrial grade chips. The workflow of this paper is as follows; Section II depicts methodology, Section III depicts results and discussion, Section IV concludes the proposed work.

II. METHODOLOGY

VLSI chips always exhibit differential temperature from onchip to the ambient environment. As per experimental observations with various FPGAs, this difference varies from 6ºC to 3ºC at room temperature based on internal architecture and steady state power dissipation of VLSI chips. As ambient temperature decreases, on-chip temperature reduces. For commercial grade chips the lower temperature limit is 0ºC. Beyond 0ºC uncertainty of chip operation and inconvenience caused during chip migration (as discussed in section I) calls for a novel attempt of enhancing commercial grade chip to industrial grade without harming the chip parameters.

The proposed work is carried out on Xilinx VIRTEX5 and BASYS3 FPGA boards. The methodology of the proposed work is depicted in Fig.1. The known width pulse passed through the temperature sensing logic and at the output of logic, the pulse width is monitored and compared with inputted pulse width to identify the temperature. The on-chip temperature measurement and monitoring performed by extracting timing information from TDC. The whole setup is divided into following building blocks.
i.Programmable Pulse Generator (PPG) ii.Pulse Selector Circuit (PSC) iii.Pulse Passer Logic (PPL) iv.Time Detection Circuit (TDC) v.Temperature Monitor & Control (TMC) vi.Thermo Electric Cooler(TEC).

A. Programmable Pulse Generator (PPG)

The programmable pulse generator generates a pulse of required width[10]. The conceptual diagram of PPG is shown in Fig.2. The Dynamic Series Pulse Generator generates oscillation of pulses with various periods based on pulse programmer. The principal block of this circuitry is tapped delay line and ring oscillator made up of inverters. This utilizes less resources as compared to [11]. The PPG generates pulses of 43.92ns, 83.77ns, 127.9ns, and 157.1ns based on selection at room temperature. These pulses are used to sense the temperature. The advantage of PPG circuitry is that it allows measuring the temperature through multiple pulses with high accuracy. Additionally, it also provides the flexibility to generate the number of pulses just by increasing the number of tapings on delay line and corresponding select lines in pulse programmer. The single pulse generator serves the purpose of collecting enough temperature information by accumulating multiple pulses and creates one single pulse when triggered with enable signal. This pulse applied to the PSC.

B. Pulse Selector Circuit (PSC)

The PSC is a simple logic circuitry, that selects one pulse either from PPG or the external pulse. This provides flexibility to verify on-chip temperature with options.

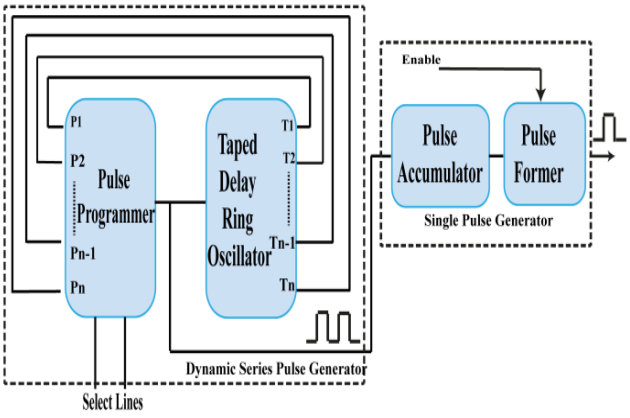

Fig. 2. Programmable Pulse Generator

C. Pulse Passer Logic (PPL)

Pulse accumulation technique of PPG extracts ample amount of temperature information. Moreover, temperature sensitivity is improved by PPL. PPL is a combinational circuitry depicted in Fig.3 has a set of temperature sensitive elements. Each element of PPL adds delay to the pulse proportional to temperature on the element through which the pulse is traveling. The propagation delay of each element of PPL logic affected by temperature with the relation is as shown in (1).

$$T_D = \frac{(\frac{L}{W})C_L}{\mu C_{ox}(V_{DD} - V_T)} \ln\left(\frac{1.5V_{DD} - 2V_T}{0.5V_{DD}}\right) \quad (1)$$

μ-mobility of electron, L- Length of channel, W -Width of channel, C_L- Load capacitance, V_T - Threshold voltage, V_{DD}- Supply voltage

The total delay provided by the PPL is shown in (2).

$$T_{PPL} = \sum_{k=1}^{n} Td_k, inv + Td, wire \quad (2)$$

Td_k,inv -Propagation delay of k^{th} inv, Td,wire -Wire delay

This T_{PPL} is very sensitive to +/- temperature changes with reference to room temperature. The proposed work initially records T_{PPL} in digital form at room temperature and keeps a watch on changing T_{PPL}. However, with little overhead of resources, instead of accumulating pulses, a pulse from PPG can be cycled through PPL to obey high temperature sensitivity. Either one among these two techniques, namely, pulse accumulation at PPG or single pulse cycling many times in PPL gives sufficient temperature information to act upon.

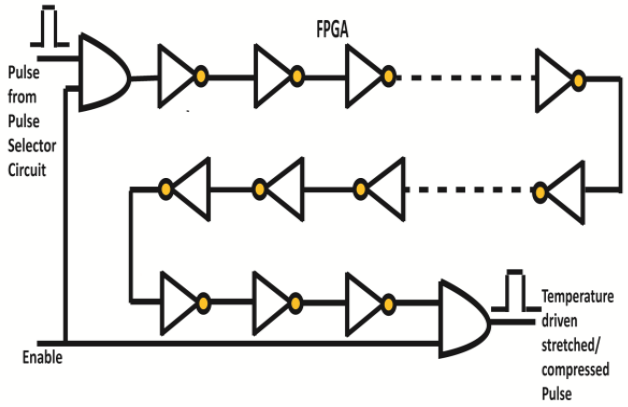

Fig.3. Pulse passer logic

D. Time Detection Circuit (TDC)

The time domain sensors exhibit various benefits on the electrical domain(voltage/current) sensors. Sensing of various parameters and conversion in digital format as proposed in [12] utilized on-chip ADC. On-chip ADC has limitations on measurement range, accuracy and linearity over the large measurement range at low operating reference voltage. The combination of PPG and PPL carries adequate temperature information in terms of time. The TDC circuitry converts time into digital form with better accuracy. This process is performed by the combined effort of PLL, DCM, Array of counters and Adder shown in Fig.4. TDC used in [13] has dual PLL for time measurement with 4 phases and has an error of ¼ of time pulse. The 4 channel TDC implemented in [14] has time resolution in terms of ns. The proposed TDC utilizes 8 phase clock to convert temperature sensitive pulse time into digital form with worst case time error of 1/8 of CLK period at the start and stop of temperature pulse. This TDC provided a time resolution of 213ps. With the PPG, PPL and 8 phase TDC, we achieved temperature detection with a resolution of 0.06°C.

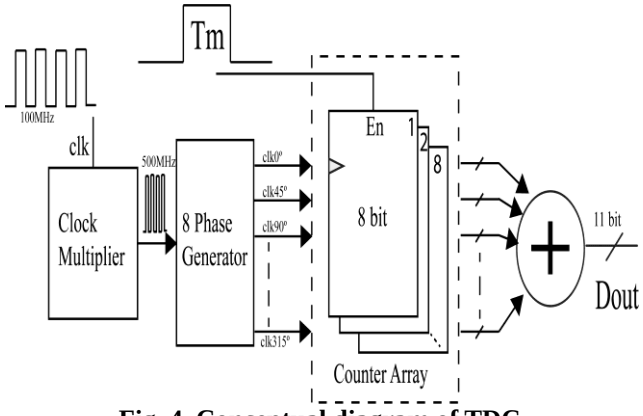

Fig. 4. Conceptual diagram of TDC

E. Temperature Monitor & Control (TMC)

TMC unit has algorithmic block, register, comparator and signal generator to operate TEC driver.

The register of TMC unit loaded with fixed threshold temperature value in digital form or the digital equivalent pulse used for temperature measurement. The TMC unit continuously reads digital data from TDC circuit and compares it with predetermined temperature values present in the register. The digital data of TDC proportional to on-chip temperature is valid till 0ºC for commercial grade FPGA. The algorithmic TMC unit operates FPGA well within the minimum temperature level. The value stored in the register of TMC unit decides the lowest temperature point. Once this temperature value is reached the TMC unit takes corrective action and triggers the control unit to uplift on-chip temperature to minimum specified level. Here above 0.5°C is considered as a golden temperature point during the experimentation of proposed work. The system of such mechanism is shown in Fig.5.

During testing of proposed work the temperature difference at two points of FPGA i.e. onchip (internal) and ambient (external to the chip) significantly varies as testing environment changes. This is depicted with two different cases.

Case1: When FPGA operating at external environment: The ambient temperature was lower than internal on-chip temperature. The typical value of this temperature difference varies with architecture of the FPGA, default static timings of chips, steady state power dissipation etc. Typical temperature differences observed with VIRTEX 5 and BASYS3 FPGAs are 4ºC and 3ºC respectively.

Case2: When FPGA at the testing chamber: FPGA kept inside temperature controlled testing chamber, and created clod environment. The two point temperature difference observed typically are, 2.5ºC for VIRTEX 5 FPGA, 2ºC for BASYS 3 with reference to the internal environment of testing chamber and onchip temperature. As time elapses at low ambient temperature, on- chip temperature starts diminishing and causes a temperature difference to fall in a short period of time as compared to case1. This means that in a cold environment, even if the ambient temperature is below 0ºC the commercial FPGA works satisfactorily for some time since its internal temperature is still above 0ºC. But if the same ambient temperature continues, commercial FPGA does not guarantee to work adequately since its internal temperature reaches 0ºC or below. This scenario of low internal temperature is monitored and controlled by TMC unit as discussed in the initial paragraph of Section II.E.

The main component of temperature controlling mechanism is ThermoElectric Cooler (TEC) and it works on the principle of Peltier effect. The TMC unit continuously monitors internal temperature of the chip. If the temperature goes below 1ºC, it passes signal to control unit. The control unit releases the current to TEC in the proper direction through TEC driver such that FPGA chip surface experiences the heat from the hot side of the TEC.

The firm contact between TEC, heat spreader & FPGA surface without air gap effectively serves the purpose of heating FPGA through TEC based on external current. The heat spreader is a component that spreads heat uniformly over the surface of FPGA [9]. As applied heat is not enough to boost the temperature inside the FPGA, the TMC unit increases the current through TEC to raise the temperature above the required level. The control unit is smart enough to start releasing current through TEC well before the 0°C junction temperature. This eliminates the failure of chips due to two facts. i. TEC current is not quick enough to boost internal temperature, ii. Risk of malfunction of FPGA at low junction temperature. The response of TMC with 3ºC ambient temperature is shown in Fig. 8. The internal temperature is measured through on-chip digital temperature sensor and inbuilt system monitor.

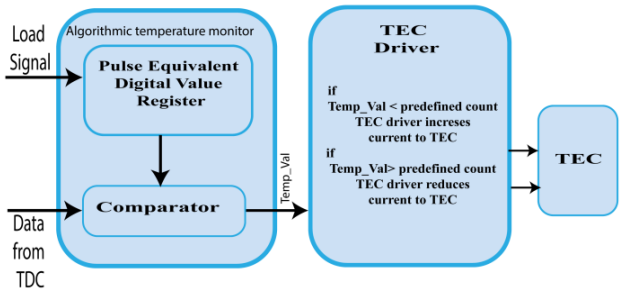

Fig. 5. Temperature Monitoring & Control Unit

The TMC unit plays key role at low on-chip temperature and at room temperature. As internal on-chip temperature reaches room temperature the control logic stops/slows down the current through TEC and keeps monitoring internal temperature to avoid overheating of chip. This mechanism maintains chip junction temperature always in a positive range even at negative ambient temperature. Hence the commercial grade chip operates in industrial grade without compromising the functionality of the chip.

The TEC is capable of cooling and heating the chip with proper mechanism and control. Hence another useful purpose exhibited by proposed mechanism is cooling of chip in hot environment. By releasing proper directive current through TEC, properly designed heat sink and fan for heat dissipation serve the purpose of cooling.

III. RESULTS AND DISCUSSION

The PPG generates predetermined pulses based on configuration by the user. It uses a pulse accumulation technique to generate a single pulse. This technique helps to achieve high sensitivity and accuracy of on-chip temperature measurement. On the other hand, the pulse neither generated by the pulse accumulation technique and nor cycled in PPL exhibits insignificant temperature sensitivity. The temperature sensing with pulse accumulation technique shown in Fig.6 (a) reveals the pulse sensitivity to change in temperature over the range of room temperature to beyond lower commercial grade temperature. With experimentation the pulse width variation observed over the range is 75ns and 2.51ns/°C. Fig. 6(b) shows the sensitivity of single pulse generated without pulse accumulation technique. The width variation observed, in this case, is ~1.2ns from the initial 156.1ns over the said temperature range. This exhibits very low temperature sensitivity. Therefore, the pulse generated through pulse accumulation technique and PPL logic contributes significantly to measure onchip temperature. Two sets of results depicted in Fig.7, demonstrates the change of operating temperature of commercial grade FPGA into industrial grade with TEC. Here both results take nearly equal time to manifest specific temperature into the chip at given current through TEC. Fig. 8 shows the experimental results of the proposed mechanism at ambient temperature of 3°C. When temperature reaches 0.5°C, TMC unit triggers TEC driver. TEC driver releases sufficient current through TEC such that TEC surface in contact with FPGA surface gets hot. Heat flux through heat spreader uniformly spread over the surface and heats the chip. Here the on-chip temperature varied when with different TEC current applied for t=60sec. Looking at Fig.8, as the ambient temperature decreases, cold flux resists to dominate hot flux, hence requires more effort at deep negative ambient temperature range to heat the chip. Even high current flows through the TEC, temperature variation is not rapid enough as compared to positive ambient temperature when same amount of current through TEC elapse same time.

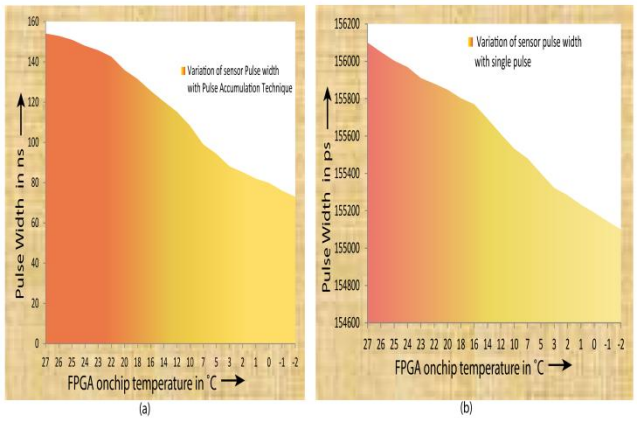

Fig.6. Delay variation of pulses over the range of room temperature to negative temperature.

Table I: Ambient temperature and onchip temperature at different TEC current

Ambient Temperature (in°C)	TEC Current to heat the chip (in Amps)	Onchip temperature (in°C) @t=60sec
3	0.5	0.88
0	1	1.38
-2	1.5	2.00
-4	2	2.13
-6	2.5	2.31
-8	3	2.44
-10	3.5	2.69
-15	4	3.10

Table I shows the ambient temperature and onchip temperature after heating chip with TEC current. When ambient temperature reaches 3°C the onchip temperature reaches very close to lower operating temperature range of commercial grade chips. As temperature goes below 0°C, chip may malfunction due to violation of minimum required temperature. Hence here 0.5°C is considered as lower threshold value of temperature. At 3°C ambient temperature, the 0.5 A of current though TEC for 60sec has raised the onchip temperature to 0.88°C. Similarly as temperature reduces below 0.5°C the TMC unit drives more current into TEC to heat up the chip and keeps onchip temperature above 0.5°C. The chip is tested up to -15°C and corresponding TEC current and increase in onchip temperature is shown in Table I. At -15°C ambient temperature, the TMC unit has maintained onchip temperature above 3°C with 4A current. The current though TEC can be reduced by maintaining moderate value of current though TEC for long time to heat the chip. For quick heating of chip wide current rage TECs can be used. The availability of TECs with low voltage high current ratings reduces the overhead of power consumption during heating.

IV. CONCLUSION

The proposed temperature grade enhancement technique fulfills the need for low cost high computing chips at low operating temperature environment. This mechanism utilizes less than 2% resources of FPGA leaving 98% resources for an application. The commercial grade FPGA woks satisfactorily in industrial grade lower temperature range till -15°C and this is tested and verified. As per this work, further use of wide operating current range TEC's expands the range towards negative temperature region. For the appropriate working tight coupling between TEC, effective heat spreader and FPGA is required. Care must be taken towards package & pins at low temperature. Thus the given technique contributes significantly in building cost effective application in low temperature range.

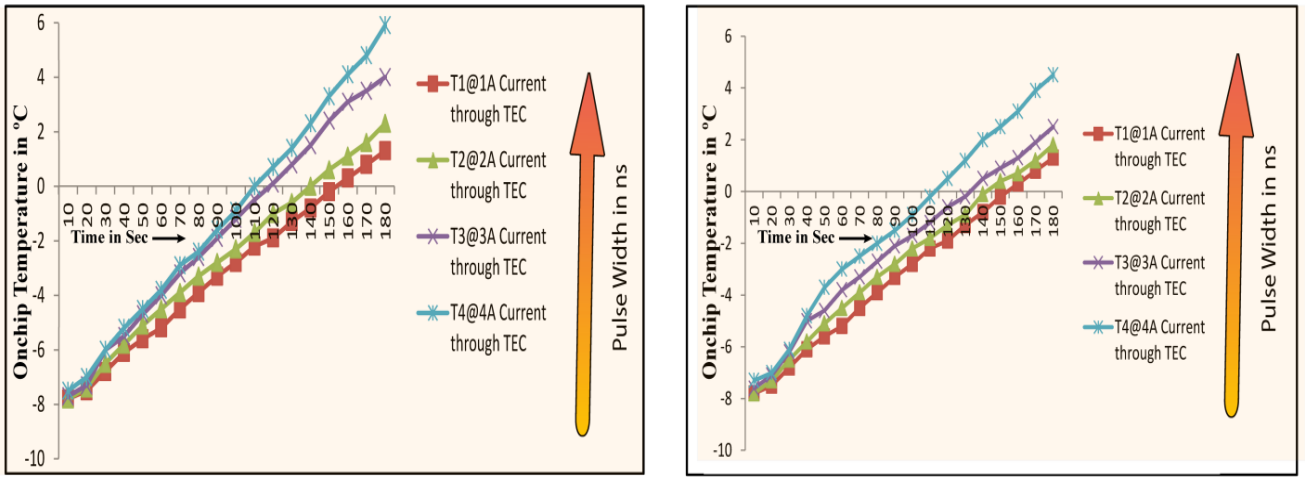

Fig.7. Experimental results of on-chip temperature variation of FPGA based on TEC current and Time

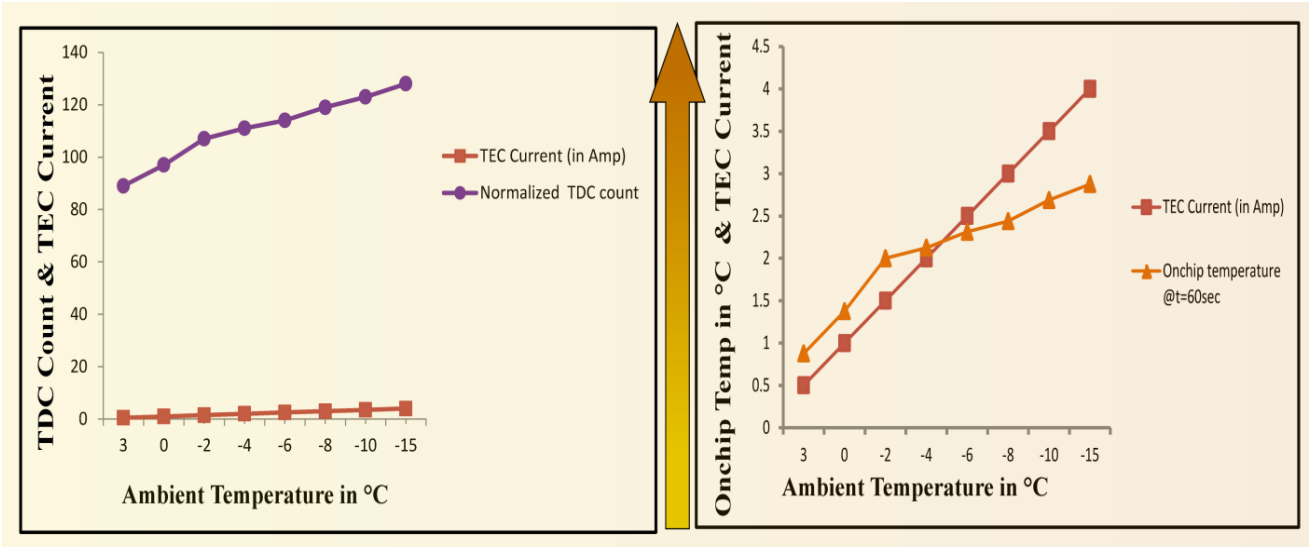

Fig. 8. Variation of TEC current, corresponding TDC count, onchip temperature w.t.r ambient temperature.

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