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Ambipolar Reduction Methodology for SOI Tunnel FETs in Low Power Applications: A Performance Report

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Abstract**:** *Continuous device scaling of tunnel field effect transistors (TFET) faces real challenges in low power VLSI applications. Here in this article, the major limitation of TFET i.e. Ambipolar conduction behavior has been thoroughly discussed and remedies to suppress the leakage current (I_{OFF}) has also been investigated. A thin pocket layers is incorporated in source and drain regions separately at Silicon on Insulator (SOI) TFET, keeping supply voltage (V_{DD}) at 0.5 V. The detail analytical modeling of surface potential distribution along the channel, electric field and tunneling current is derived in this paper. Using two-dimensional numerical device simulator, the various designs are modeled and validated with our proposed methodology. Non-local Band-to-Band tunneling (BTBT) is used for simulation purpose. It is observed that a drain pocket actually helps to reduce the ambipolar conduction and provide better drive current (I_{ON}) for fast switching. This further improves the I_{ON}/I_{OFF} ratio and also results better subthreshold swing (SS) as 27.43mV/decade to optimize the device characteristics.*

Keywords**:** *SOI, TFET, Drain pocket, Source pocket, Ambipolar conduction, Band-to-Band tunneling (BTBT), Drive current (I_{ON}), Leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio, Subthreshold swing (SS).*

I. INTRODUCTION

The continuous degradation of conventional metal oxide semiconductor devices faces real challenges in low power applications. In recent times, the device parameters are scaled down from milli-meter to nano-meter scale in order to meet ultra-large-scale integration (ULSI) applications. Since, the conventional metal oxide semiconductor field effect transistors (MOSFET) can provide a limited subthreshold swing (SS) of 60mV/decade, therefore a different device physics need to be incorporated for better swing [1]. Field effect transistors with band-to-band tunneling mechanism i.e. tunnel field effect transistors (TFET) can provide better swing compared to earlier [2]. But the drive current (I_{ON}) produced by TFET devices are not sufficient enough for fast switching. The major limitation appeared with low ON current is ambipolarity of tunnel FETs [3, 4].

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Here in this paper, a complete study report has been made on the ambipolarity issues commonly appeared on tunnel FETs. Dawit Abdi and Jagadesh Kumar has introduced gate on drain overlapping on conventional TFETs, could suppress the ambipolarity up-to certain extent [5]. The proposed model got debacle consequences due to outer fringe capacitance effect. Sneh Saurabh and Mamidala Jagadesh Kumar discussed the ambipolarity behavior in detail in 2016. The ambipolarity means a same tunnel FET shows the electrons and holes transport movement at the same drain voltage (V_{DS}). Due to this ambipolar current, the leakage current (I_{OFF}) gets increased [6]. K. Nigam et. al gave a useful insight for ambipolar reduction by introducing work function engineering [7], described in their literature published in 2016. The chance of more leakage current may appear for smaller band gap materials used in tunnel FET. Michael Graef et. al also investigated the ambipolar issues in their research article in 2018, where the ambipolar behavior has been suppressed by using a reduced drain doping concentration [8]. This approach has also been introduced in Multigate silicon on insulator (SOI) tunnel FET structures.

II. DEVICE STRUCTURES WITH PHYSICAL MODELS FOR SIMULATION

A. Device modeling with specifications

The conventional two-dimensional device structure of tunnel FET is designed, further modified and investigated on the adverse effect of ambipolar conduction in TFET [9-12]. In order to boost the ON state current, the band-to-band tunneling phenomenon is introduced by modeling TFET structure, where it can be observed that the source and drain regions are doped with P-type and N-type carriers for n-channel TFET. The middle section is called intrinsic region which is less doped compared to other two regions.

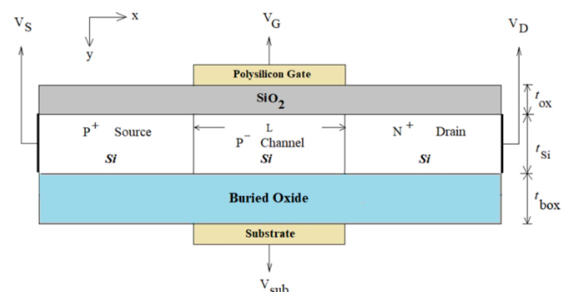

Fig. 1. 2-D device structure of SOI Tunnel FET.

The figure 1 depicts the cross-sectional view of conventional two-dimensional silicon on insulator (SOI) tunnel FET structure. Now in order to suppress the ambipolar conduction in SOI TFET structure, a thin 2 nm pocket layer is stitched with source region.

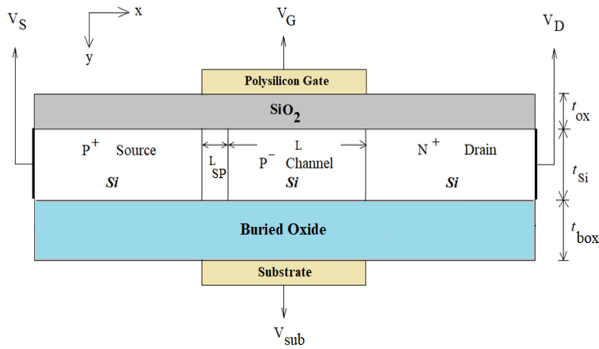

Fig. 2. 2-D device structure of SOI Tunnel FET with Source Pocket doping.

The length of source pocket region is denoted as L_{SP}, where the effective length of the channel gets reduced to 48 nm shown in figure 2. Similarly, many researchers' study compelled us to review the drain side doping in SOI tunnel FET structure. Similarly, a thickness of 2 nm drain pocket (L_{DP}) has been incorporated for obtaining better I_{ON} as well as subthreshold swing (SS). As shown in figure 3, the drain pocket layer has been placed accordingly.

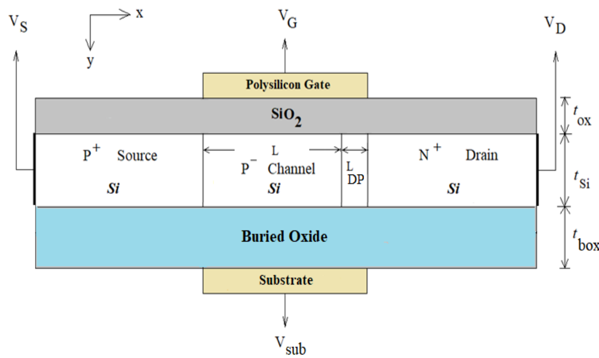

Fig. 3. 2-D device structure of SOI Tunnel FET with Drain Pocket doping.

B. Device parameters and Electrical parameters

The detail comparison study is performed by referring the recent literature surveys. Wherein, the typical device as well as electrical parameters have been successfully used for simulation and implemented in laboratories. We have used a homogeneous model by using material Silicon (*Si*) commonly in source – drain and the channel regions of the tunnel field effect transistors.

Table- I: Typical device and electrical parameters of all the SOI tunnel FET structures used in this work

Parameters	SOI Tunnel FET with *Si* channel
Intrinsic channel length / Effective channel length (L)	50 nm
Source doped region length (L_{SP})	2 nm
Drain doped region length (L_{DP})	2 nm
Gate oxide thickness (t_{ox})	2 nm
Body thickness (t_{si})	10 nm
Buried oxide thickness (t_{BOX})	10 nm
Source doping (N_s)	1×10^{20} cm^{-3}
Drain doping (N_d)	5×10^{18} cm^{-3}
Channel doipng (N_i)	1×10^{17} cm^{-3}
Metal workfuction	4.8 eV
Gate voltage (V_{GS})	1 V
Supply voltage (V_{DD})	0.5 V – 1 V

C. Simulation

The design of physical models of SOI tunnel FET are simulated using two-dimensional numerical device simulator. The quantum tunneling has been modeled as non-local band-to-band tunneling (BTBT) for numerical simulation.

III. PROPOSED METHODOLY

In this section, the mathematical analysis steps are discussed. All the device structures are designed by a device simulator software, which further assessed and validated by analytical modeling of the designed structure. In this article, the major limitation of a tunnel FET i.e. ambipolarity issues have been studied. Therefore, to reach our final objective, the essential parameters need to be obtained viz. drain current or tunneling current (I_{ON} or I_{tun}), leakage current or OFF state current ($I_{leakage}$ or I_{OFF}), subthreshold swing (SS). Therefore, the regions need to be identified first, then the individual boundary conditions are to be made. To capture the quantum effect of carrier transport across the channel two-dimensional nonlinear Poisson's equation is used to determine the surface potential [13].

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = \frac{qN_i}{\varepsilon_{Si}} \; for \; 0 \le x \le L, 0 \le y \le t_{Si} \quad (1)$$

Where, $\psi(x,y)$ is the electrostatic potential, q is the electronic charge, ε_{si} is the permittivity of silicon and N_i is the doping concentration of the intrinsic channel region considered. The total channel length is L and t_{si} is the channel thickness.

The surface potential along the channel is approximated by segregating the channel region into effective regions. Young's approximation is used to obtain $\psi(x,y)$ by assuming the necessary boundary conditions [14].

For the electric field modeling, the lateral electric field E_x and the vertical electric field E_y can be written as:

$$E_x = -\frac{\partial\psi(x,y)}{\partial x} \text{ and } E_y = -\frac{\partial\psi(x,y)}{\partial y} \quad (2)$$

So, total e-field is:

$$E = \sqrt{{E_x}^2 + {E_y}^2} \quad (3)$$

Now the drain current can be obtained by using Kane's model [15] to determine the local band-to-band tunneling generation rate per unit volume (G_{BTBT}).

So, the ON-state tunneling current (I_{tun}) [16] can be written as,

$$I_{tun} = q \iint G_{BTBT}\, dx\, dy \quad (4)$$

Where the band-to-band tunneling generation rate can be written as:

$$G_{BTBT} = A_K \frac{|E|^D}{\sqrt{E_g}} exp\left(-\frac{B_K E_g^{3/2}}{|E|}\right) \quad (5)$$

Here, A_K and B_K are the parameters which depend on effective mass of valence band and conduction band electrons determined by device dimensions. D is a material dependent constant. E_g symbolizes the energy band gap of silicon channel whereas, E denotes the local electric field.

Finally, now the tunneling current I_{tun} is computed by equation (4), which is the ON state current across the tunneling region. By varying the gate bias potential, the leakage current can also be obtained.

IV. RESULTS AND DISCUSSIONS

All the simulations were performed in Silvaco Atlas device simulator. In this work, non-local band-to-band-tunneling (BTBT) model is used to consider the lateral direction tunneling movement of carriers [17-19].

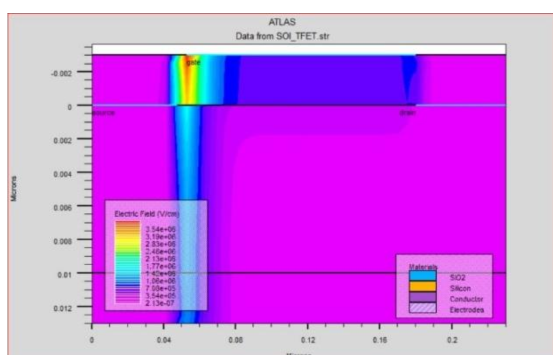

Fig. 4. Electric field variation contour of SOI Tunnel FET.

With the source doping concentration of 1×10^{20} cm^{-3} and drain doping of 5×10^{18} cm^{-3}, the electric field contour plot is shown in figure 4.

The surface potential contour plot is depicted in figure 5, where the contour is plotted at supply voltage V_{DD} = 1V and variable gate voltage V_{GS} = 0.5V to 1.5V.

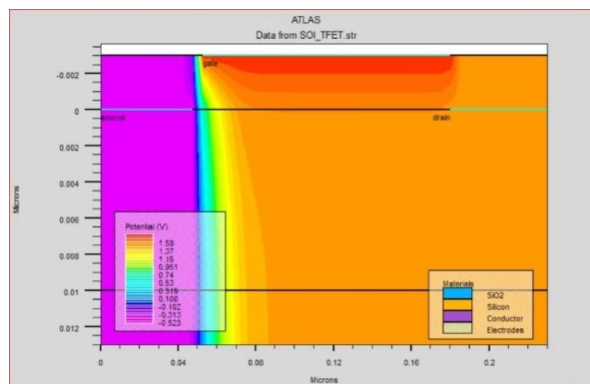

Fig. 5. Surface potential contour of SOI Tunnel FET.

The transfer characteristics is shown in figure 6, where the OFF-state current has been suppressed considerably by varying the device structures of tunnel FET. The 2nm thick drain pocket SOI TFET provides the better ON state current and most importantly better suppressed ambipolar current (I_{OFF}). Here the drain current is taken in logarithmic scale whereas, the gate voltage is considered as normal scale.

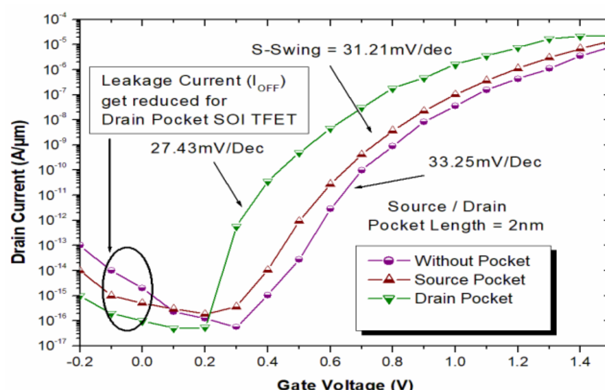

Fig. 6. Transfer characteristics of different device structures of SOI TFET at supply voltage V_{DD}=0.5V

Finally, the simulated data is validated by the analytical modeling of tunneling current and leakage current obtained from our proposed methodology. The comparison between the simulated and analytical data is depicted in figure 7. In this graph, the solid lines are used for simulation data both for Source Pocket tunnel FET (SP TFET) and Drain Pocket tunnel FET (DP TFET). Whereas, the dotted lines are denoted for analytical data for both device structures.

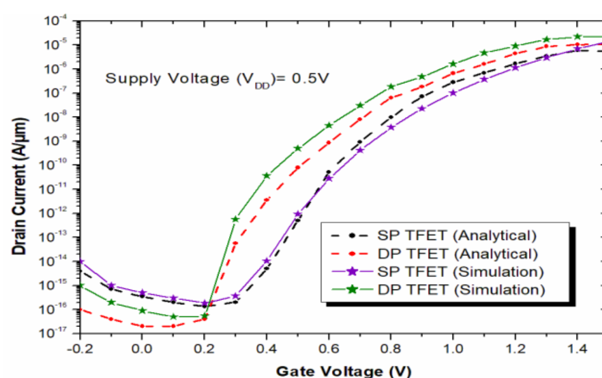

Fig. 7. Drain current versus V_{GS} at supply voltage (V_{DD}) = 0.5V (Simulation and Analytical)

From figure 7 it is evident that among all type of pocket layered tunnel FET structures, the drain pocketed SOI tunnel FET provides better control in leakage current, where I_{OFF} recorded best at 8.93×10^{-16} A/µm. Also, the ON current is obtained best at 7.62×10^{-5} A/µm compared to source pocket and without pocket SOI tunnel FET. This further improves the I_{ON}/I_{OFF} switching ratio, that can be useful for fast switching applications. The ambipolar conduction suppression can open the door of low power applications.

Besides the above positive findings, the slope obtained by the drain pocketed tunnel FET becomes steep. Therefore, a subthreshold swing (ss) of 27.43 mV/decade is recorded best for DP TFET shown in figure 6. Table II details the subthreshold swing (ss) of all designed models.

Table- II: Subthreshold swing of different TFET models.

Device models	Subthreshold swing (SS)
Conventional SOI TFET without pocket	33.25 mV/decade
Source pocket TFET	31.21 mV/decade
Drain pocket TFET	27.43 mV/decade

V. CONCLUSION

This work mainly focuses on ambipolar current suppress methods, that can be implemented in silicon on insulator tunnel FETs. Therefore, a rigorous recent literature survey is made, followed by different device structure modeling. The structure modeling is performed using two-dimensional numerical device simulator. Then the simulation data is matched with proposed semi-analytical model of tunnel FET. Wherein, we could find the best drive current or ON state current as 7.62×10^{-5} A/µm and the minimum leakage current as 8.93×10^{-16} A/µm. This minimum leakage current actually signifies the ambipolarity suppression. The better ambipolar reduction has been achieved for drain pocket SOI TFET compared to all other SOI TFET device models. This may further be helpful for low power logic applications. Besides this, DP TFET produces best subthreshold swing as 27.43 mV/decade, which is considerably less compared to conventional 60 mV/decade at room temperature. The process has been performed at 0.5V supply voltage, further varied till 1V, can be worth for low power applications.

REFERENCES

1. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic", Proc. IEEE, Vol.98, No.12, pp.2095–2110, 2010.
2. N. Thomas, H.S. Philip Wong, "The end of Moore's Law: a new beginning for information technology", IEEE J. Comput. Sci. Eng. 19(2), pp.41–50, 2017.
3. C. Anghel, Hraziia, A. Gupta, A. Amara and A. Vladimirescu, "30-nm Tunnel FET With Improved Performance and Reduced Ambipolar Current," IEEE Transactions on Electron Devices, vol.58, no.6, pp.1649-1654, 2011.
4. R. Narang, M. Saxena, R.S. Gupta and M. Gupta, "Assessment of Ambipolar Behavior of a Tunnel FET and Influence of Structural Modifications", Journal of Semiconductor Technology and Science 12(4), 2012.
5. D.B. Abdi and M.J. Kumar, "Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain", IEEE Journal of the Electron Devices Society, 2(6), pp.187-190, 2014.
6. S. Saurabh and M.J. Kumar, "Fundamentals of Tunnel Field-Effect Transistors", ISBN 9781498767132, CRC Press, 292 pages, 2016.
7. K. Nigam, P. Kondekar and D. Sharma, "Approach for ambipolar behavior suppression in tunnel FET by work function Engineering," Micro & Nano Letters, vol.11, no.8, pp.460–464, 2016.
8. M. Graef, F. Hosenfeld, F. Horst, A. Farokhnejad, F. Hain, B. Iñíguez, and A. Kloes, "Advanced Analytical Modeling of Double-Gate Tunnel-FETs-A Performance Evaluation", Solid-State Electronics, vol.141, pp. 31–39. Elsevier, 2018.
9. G.D. Das, G.P. Mishra, and S. Dash, "Impact of source-pocket engineering on device performance of dielectric modulated tunnel FET", Superlattices and Microstructures, vol.124, pp-131-138, 2018.
10. R. Dutta and N. Paitya, "Electrical Characteristics Assessment on Heterojunction Tunnel FET (HTFET) by Optimizing Various High-κ Materials: HfO_2/ZrO_2", Int. J. of Innovative Technology and Exploring Engineering, vol.8, no.10, pp.393-396, 2019.
11. S. Garg and S. Saurabh, "Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis", Superlattices and Microstructures, vol.113, pp-261-270, 2018.
12. R. Dutta and N. Paitya, "Effect of Pocket Intrinsic Doping on Double and Triple Gate Tunnel Field Effect Transistors", Proceedings of the 2nd Int. Conf. on Communication, Devices and Computing. Lecture Notes in Electrical Engineering, vol 602. Springer, 2020.
13. C. Shen, S.L. Ong, C.H. Heng, G. Samudra, and Y.C. Yeo, "A variational approach to the two-dimensional nonlinear Poisson's equation for the modeling of tunneling transistors", IEEE Electron Device Lett., vol.29, no.11, pp.1252–1255, 2008.
14. K.K. Young, "Short-channel effect in fully depleted SOI MOSFETs," IEEE Trans. Electron Devices, vol.36, no.2, pp. 399–402, Feb.1989.
15. E. O. Kane, "Theory of tunneling", J. Appl. Phys., vol.32, no.1, pp. 83–91, 1961.
16. A. S. Verhulst, D. Leonelli, R. Rooyackers, and G. Groeseneken, "Drain voltage dependent analytical model of tunnel field-effect transistors", J. Appl. Phys., vol.110, no.2, pp.024510-1–024510-10, 2011.
17. TCAD Atlas Manual, Silvaco, Inc., CA 95054, USA, 2015.
18. R. Dutta, S.C. Konar, N. Paitya, "Influence of Gate and Channel Engineering on Multigate Tunnel FETs: A Review", In: K. Maharatna, M. Kanjilal, S. Konar, S. Nandi, K. Das (eds) Computational Advancement in Communication Circuits and Systems. Lecture Notes in Electrical Engineering, vol 575. Springer, 2020.
19. R. Dutta and N. Paitya, "TCAD Performance Analysis of P-I-N Tunneling FETS Under Surrounded Gate Structure", *SSRN-Elsevier*, 2019.

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