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Parallel Connected Common DC-Link Fed DSTATCOM for Power Quality Improvement

P. V. V Satyanarayana, P. V. Ramana Rao

Abstract*: Power quality is a comprehensive term used to estimate the caliber of the power system in delivering high-grade supply and is an interesting study to ensure customer satisfaction. DSTATCOM is one of the custom power devices used to refine the power system parameters especially to ensure that the source current contains acceptable harmonic limit. Parallel connected DSTATCOM is a topology with two parallel DSTATCOMs connected to the point of common coupling for harmonic reduction in source current and improving the power quality. Each of the two parallel DSTATCOMs has its individual DC storage source to adjust the real power deficit to the system (during load transients). This paper presents a common DC-Link fed parallel DSTATCOM topology for power quality improvement. Unlike the conventional parallel DSTATCOM topology, common DC-Link fed parallel DSTATCOM topology employs only one DC-Link source reducing the number of DC sources, cost and increases reliability. The single DC storage source adjusts the real power deficit to the system. In this paper, IRP control methodology delivers the control pulses to parallel DSTATCOM. The proposed system is tested with variable and constant load operations and the results are presented using MATLAB/SIMULINK software.

***Keywords* : Power quality, common DC-Link, harmonics, parallel DSTATCOM..**

I. INTRODUCTION

Power quality is a general phrase in saying about the annoyance in power supply parameters. Power quality associated issues are increasing in recent years. Any divergence in current/voltage waveforms from the original shape is termed as power quality (PQ) disturbance. PQ disturbances range from few nanoseconds (short duration) to several minutes (long duration). PQ issues mainly arise due to brisk expansion of non-linear loads like switched-mode power supplies (SMPS), power electronic converters, variable speed motor drives, etc [1-2].

Harmonics are one of the power quality issues that affect the power system generating adverse reactions. The current or voltage signals having frequencies that are integral multiples of fundamental quantities are termed as harmonics and these harmonic currents/voltages when superimposed on fundamental signal cause the current/voltage signal to deform the fundamental wave shape. Most of the end-user or industrial types of equipment like power converters, variable speed motor drives are non-linear in nature and induce harmonics in power system.

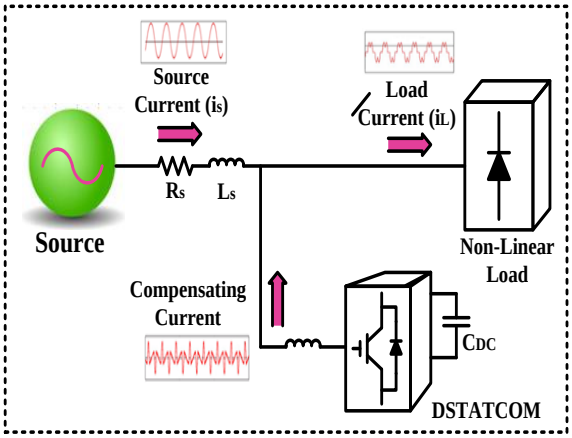

Figure 1: Block diagram of DSTATCOM in the distribution system

Harmonic currents present in the power system are classified as odd and even harmonics. Even order harmonics do not add up to the deformation of the system parameters but odd harmonics have adverse effect on power system. Lower order odd harmonics are present to a large extent in power system while higher-order harmonics can be easily filtered out. Due to inherent limitation of passive filter operation, power electronics-based active filters came into existence.

DSTATCOM (Distribution Static Compensator) [3-5] is a shunt active filter connected in parallel to the power system designed to filter harmonics in source current. Figure 1 illustrates the DSTATCOM connected to the power system. Harmonics generated by non-linear loads deform the source current. The DSTATCOM connected at the point of common coupling induces equal and opposite harmonic components to compensate harmonics and refine source current waveform [6-7]. In the power system, the real power requirement is to be supplied from the source. During load transients, the real power required by the load varies and there will be dissimilarity in real power balance. A DC-Link source in DSTATCOM provides real power stability maintaining the power balance during load transients. In a parallel connected DSTATCOM topology with two parallel DSTATCOMs connected to point of common coupling for harmonic reduction in source current, each has its individual DC storage source. This paper presents a common DC-Link fed parallel DSTATCOM topology for power quality improvement. The single DC storage source adjusts the real power deficit to the system.

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Unlike the conventional parallel DSTATCOM topology, common DC-Link fed parallel DSTATCOM topology employs only one DC-Link source reducing the number of DC sources, cost and increases reliability.

Control pulses for parallel DSTATCOM are generated from instantaneous reactive power theory [8-10].

II. PARALLEL DSTATCOM TOPOLOGY

DSTATCOM is a FACTS device used to offset the current harmonics in the system by injecting equal and opposite compensating currents. DSTATCOM is a current infusing source adding compensating currents which are 180^0 apart from the load counterpart. DSTATCOM is a power converter with power switches and a DC source. Power switches of DSTATCOM are triggered by control signals. The output of DSTATCOM is infused to point of common coupling through a filter. Harmonic compensation from DSTATCOM depends on the number of harmonics present in the system. Filtering of high quantity of harmonics insists on high rated power switches and DC source.

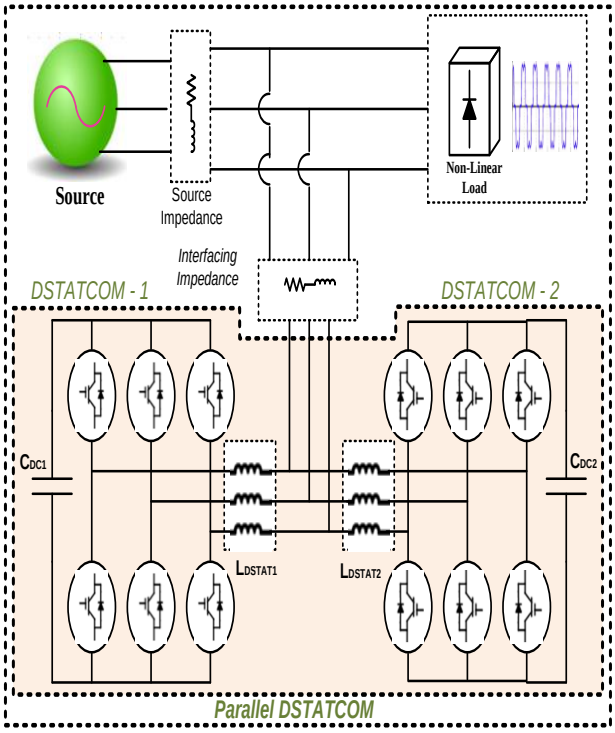

Figure 2: Parallel DSTATCOM topology in a power system

Figure 2 shows the schematic arrangement and structure of Parallel DSTATCOM in the power system. Parallel DSTATCOM is a topology introduced to share the burden of generating compensating signals. Parallel DSTATCOM topology also reduces the burden on power switches and the switching losses. Conventional parallel-connected DSTATCOM topology consists of two DSTATCOMs in parallel connected at point of common coupling. Each of the two parallel DSTATCOMs has its individual DC storage source.

III. COMMON DC-LINK FED PARALLEL DSTATCOM TOPOLOGY

DC storage source is one of the important active components in DSTATCOM connected power system which acts as a driving force to DSTATCOM and also balances the real power in the system. Under steady-state operations of the power system, the real power supplied by the source meets the load demand and some losses. Under transient conditions of the power system, real power balance is not maintained between the source and the load and this DC storage source in DSTATCOM acts as an active element delivering the deficit real power in the power system maintaining the real power balance in the power system.

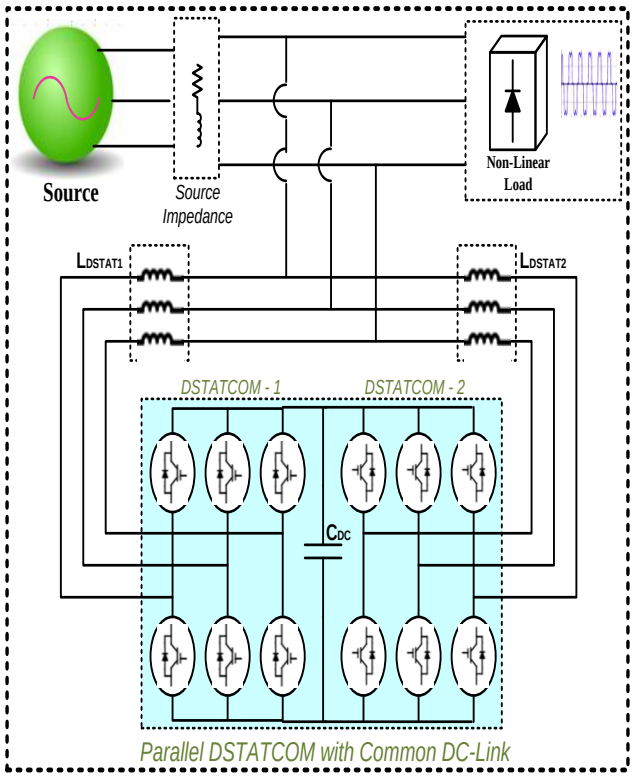

Figure 3: Common DC-Link fed parallel DSTATCOM

Conventional parallel DSTATCOM structure consists of two DC sources connected to two individual DSTATCOMs. Two individual DC sources for parallel DSTATCOM topology need two voltage sensors for controlling the DC-Link voltage. If one sensor malfunctions or if one storage source is inactive, the parallel DSTATCOM topology might be ineffective to pull out the harmonics. This phenomenon reduces the reliability of the system. Having two DC sources increases the cost too. On the other hand, parallel DSTATCOM topology can be driven using a single DC source (common DC-Link). Figure 3 describes the common DC-Link fed parallel DSTATCOM topology.

The common DC-Link fed parallel DSTATCOM topology reduces the number of sensors, reducing the cost and increasing the reliability.

IV. CONTROL OF PARALLEL DSTATCOM

A) Control of conventional parallel DSTATCOM

Current harmonics are compensated using instantaneous reactive power (IRP) theory. Clarke's transformation of three-phase terminal voltage and load current signals transform voltage/current signals to stationary quadrature signals as presented in equations (1) and (2).

$$\begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} I_0 \\ I_\alpha \\ I_\beta \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad (2)$$

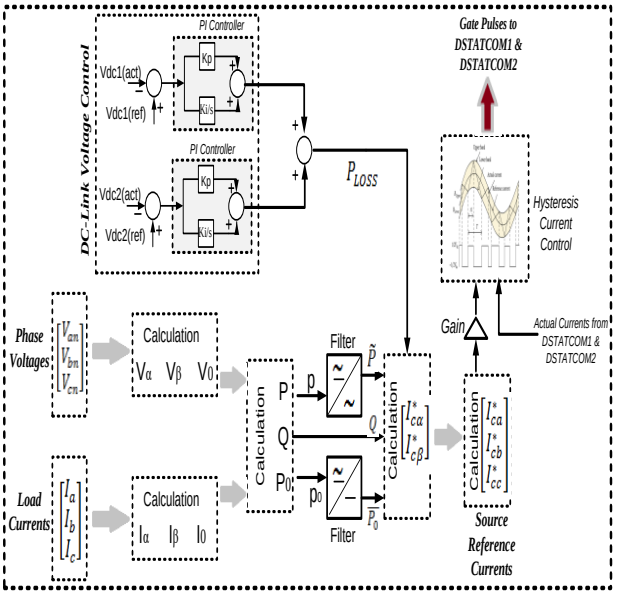

Figure 4: Control of conventional DC source parallel DSTATCOM

The three-phase instantaneous active power components can be illustrated as in (3)

$$P_{3\emptyset} = V_0 I_0 + V_\alpha I_\alpha + V_\beta I_\beta \quad (3)$$

If the power components are to be separated with respect to their average and oscillating components:

Zero-sequence power, $P_0 = \overline{P_0} + \tilde{P_0}$ (4)

Real power, $P = \bar{P} + \tilde{P}$ (5)

Reactive power, $Q = \bar{Q} + \tilde{Q}$ (6)

The two DC source voltages of two DSTATCOMs (V_{DC1} and V_{DC2}) are sensed and compared to the reference DC component. The error signals are processed through PI controllers to give out power loss component. The active power component in equation (5), reactive power component in equation (6) along with the power loss components are processed to obtain reference source current (in α-β) signals as presented in equation (7).

$$\begin{bmatrix} I^*_{c\alpha} \\ I^*_{c\beta} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2 + V_\beta^2}} \begin{bmatrix} V_\alpha & V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \quad (7)$$

Inverse Clarke's transformation of reference source current signals in α-β components yields reference source current signals in a-b-c components as in equation (8).

$$\begin{bmatrix} I^*_{ca} \\ I^*_{cb} \\ I^*_{cc} \end{bmatrix} = \frac{\sqrt{2}}{3} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I^*_{c0} \\ I^*_{c\alpha} \\ I^*_{c\beta} \end{bmatrix} \quad (8)$$

The reference current signals in a-b-c terms are processed to the hysteresis controller through gain. Actual currents from DSTATCOM1 and DSTATCOM2 (of parallel DSTATCOM topology) are processed to hysteresis controller along with reference current signals to generate controlled gating pulses to the power switches of DSTATCOM1 and DSTATCOM2. The complete schematic algorithm of controlling conventional DC source parallel DSTATCOM is shown in figure 4.

b) Control of common DC-Link fed parallel DSTATCOM

The IRP control methodology (presented in section 4.1) is extended to control common DC-Link fed parallel DSTATCOM. Clarke's transformation of three-phase terminal voltage and load current signals transform voltage/current signals to stationary quadrature signals as presented in equations (1) and (2).

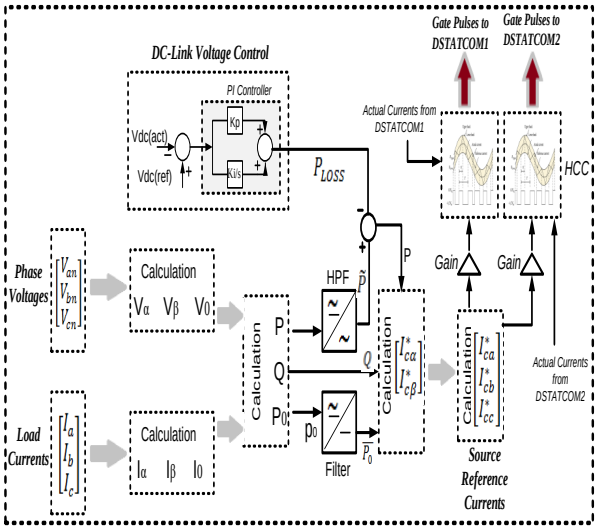

Figure 5: Control of common DC-Link fed parallel DSTATCOM

Only one sensor is required in controlling the DC-Link voltage of common DC-Link fed parallel DSTATCOM. The power loss component is calculated by sensing common DC-Link voltage and comparing the same with reference value generating an error signal. PI controller generates power loss component of power taking the error signal as input. The active power component in equation (5), reactive power component in equation (6) along with the power loss components are processed to obtain reference source current (in α-β) signals as in equation (7).

Reference current signals in a-b-c terms are calculated and processed to the hysteresis controller. Reference current signals with added gain are processed to hysteresis controller along with actual DSTATCOM1 currents to generate control pulses to power switches of DSTATCOM1. Similarly, Reference current signals with added gain are processed to hysteresis controller along with actual DSTATCOM2 currents to generate control pulses to power switches of DSTATCOM2. Control of common DC-Link fed parallel DSTATCOM is illustrated in figure 5.

V. RESULTS ANALYSIS AND DISCUSSIONS

a) Parallel DSTATCOM with separate DC Sources and fixed load condition

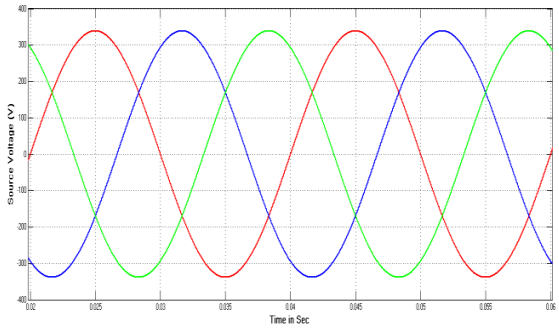

Figure 6: Three-phase source voltage

Figure 6 depicts the three-phase balanced source voltage waveform of 340V peak with no harmonic distortion.

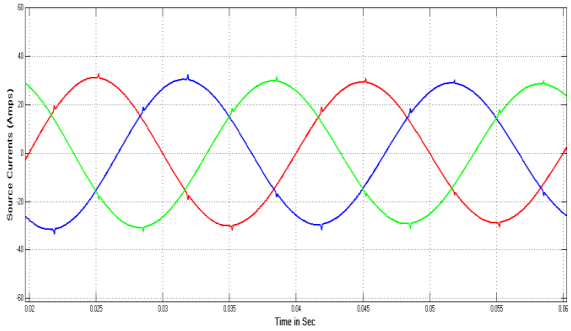

Figure 7: Three-phase source currents

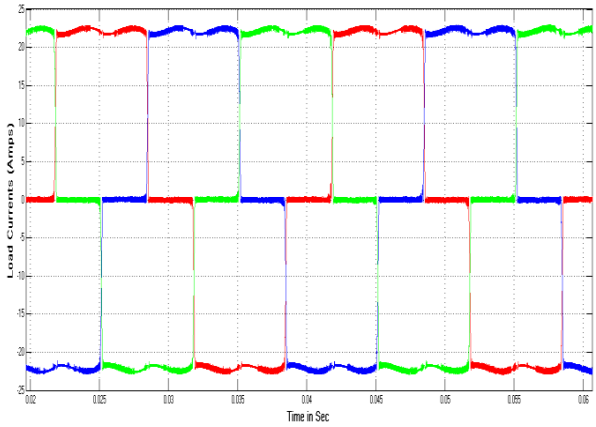

Figure 8: Three-phase load currents

Three-phase source currents are shown in figure 7. Source currents are balanced with a peak magnitude of 30A. Figure 8 shows the three-phase currents drawn by the load. The load is non-linear in nature and hence load current is distorted. The non-linear currents drawn by the load distorts the source current.

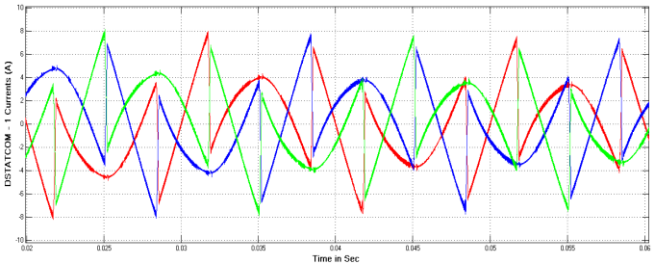

Figure 9: Compensating currents from DSTATCOM-1

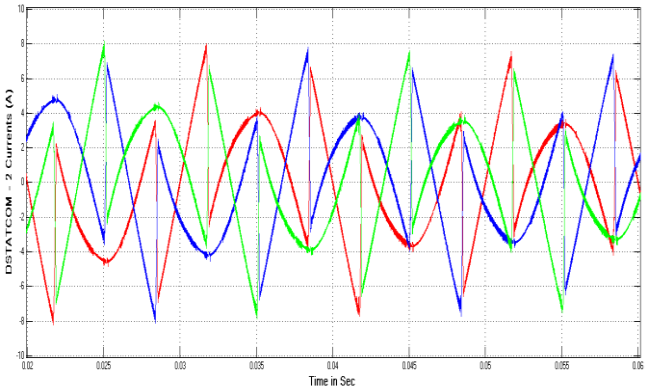

Figure 10: Compensating currents from DSTATCOM-2

Figure 9 and figure 10 illustrate the compensating currents induced to point of common coupling by DSTATCOM-1 and DSTATCOM-2 respectively, to refine the source current and ensure that the distortion of source current is within standard limits.

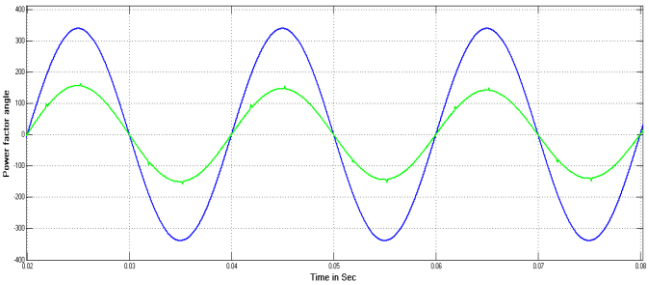

Figure 11: Power factor angle between the source voltage and source current

Figure 11 shows the power factor angle between the source voltage and source current which tends to near unity.

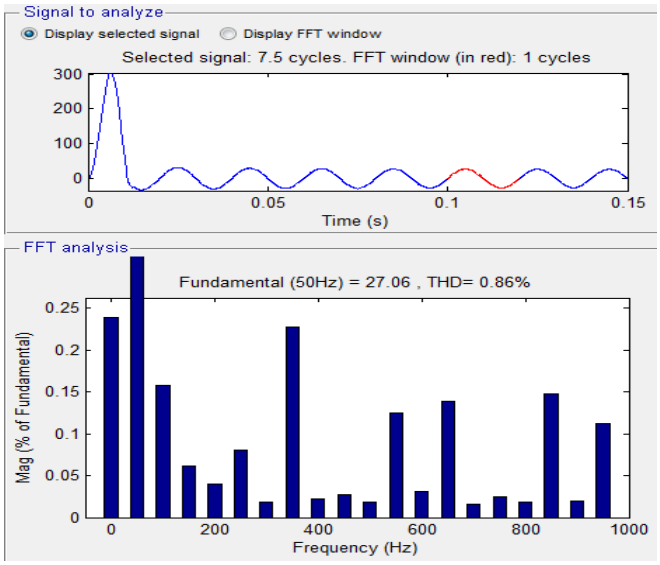

Figure 12: THD in source current

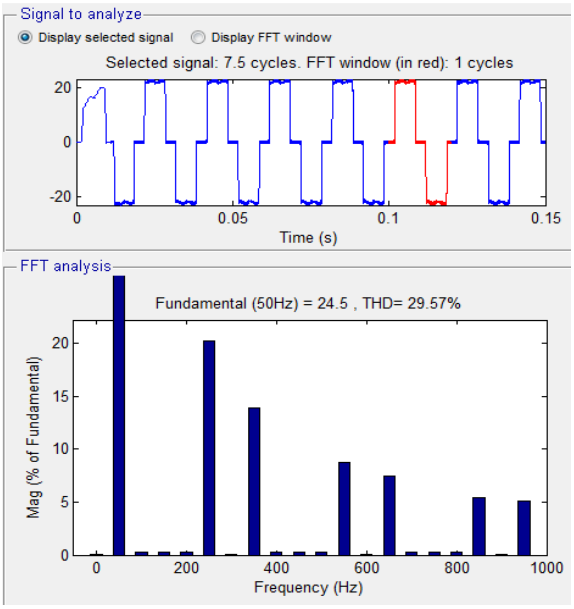

Figure 13: THD in load current

Harmonic distortion (with respect to fundamental) in source current and load current are shown in figure 12 and figure 13 respectively. The load is non-linear in nature and distortion is 29.57% and distorts the source current too. Compensating signals from parallel DSTATCOMs refine the source current and distortion in source current is 0.86%.

b) Common DC-Link fed Parallel DSTATCOM and fixed load condition

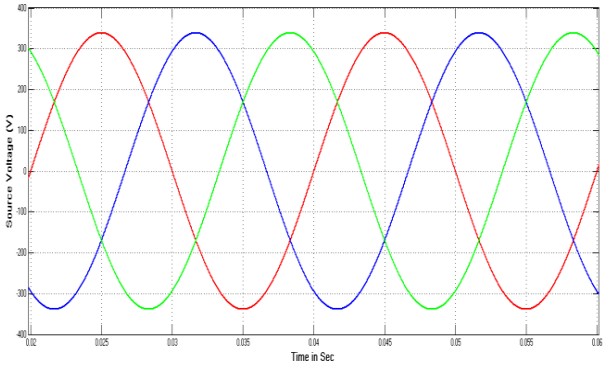

Figure 14: Three-phase source voltage

In Figure 14 is shown the balanced three-phase source voltage waveform of 340V peak with no harmonic distortion.

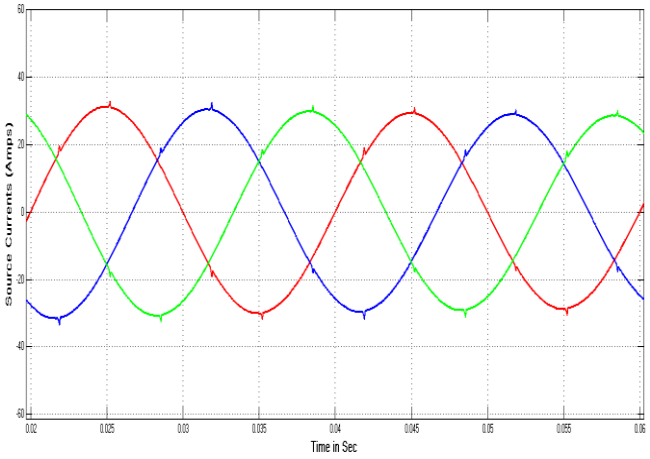

Figure 15: Three-phase source currents

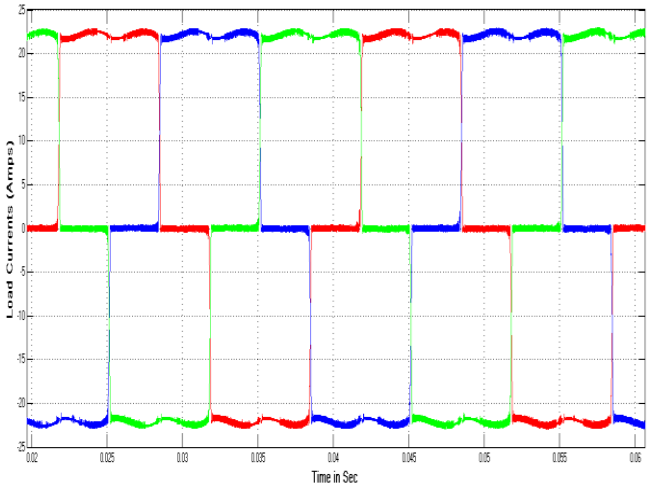

Figure 16: Three-phase load currents

Three-phase source currents are shown in figure 15. Source currents are balanced with a peak magnitude of 30A. Figure 16 shows the three-phase currents drawn by the load. The load is non-linear in nature and hence load current is distorted. The non-linear currents drawn by the load distorts the source current. The power system is operated under constant load condition; source current and load current have constant peak magnitude.

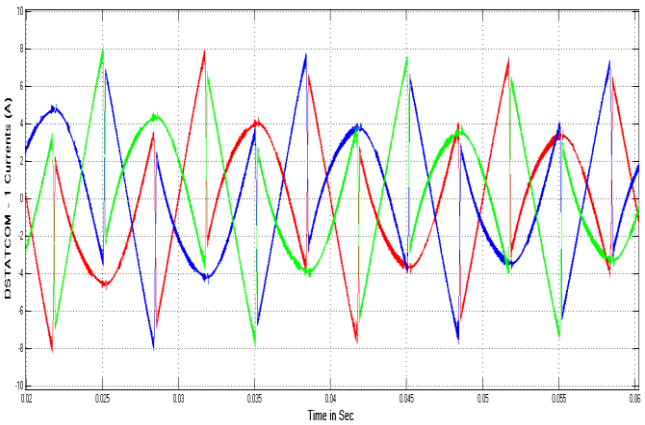

Figure 17: Compensating currents from DSTATCOM-1

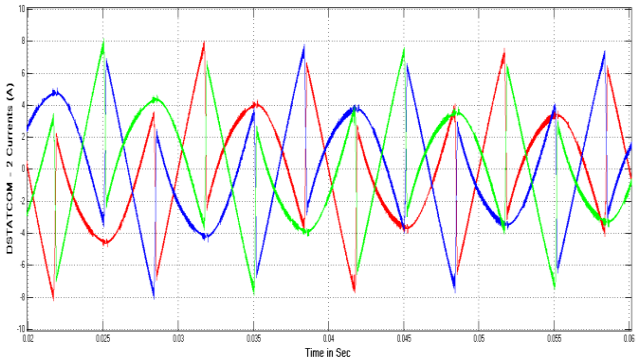

Figure 18: Compensating currents from DSTATCOM-2

Figure 17 and figure 18 illustrate the compensating currents induced to point of common coupling by DSTATCOM-1 and DSTATCOM-2 respectively, to refine the source current and ensure that the distortion of source current is within standard limits.

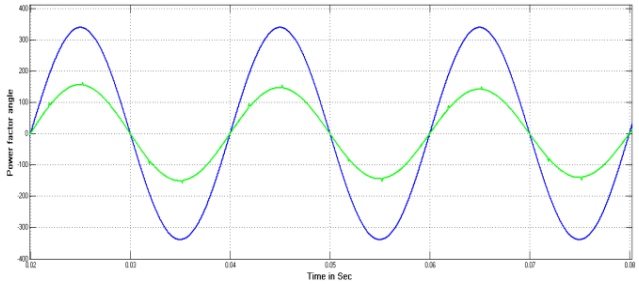

Figure 19: Power factor angle between the source voltage and source current

Figure 19 shows the power factor angle between the source voltage and source current. Source voltage and source current are not displaced with respect to phase angle and power factor tends to nearer unity.

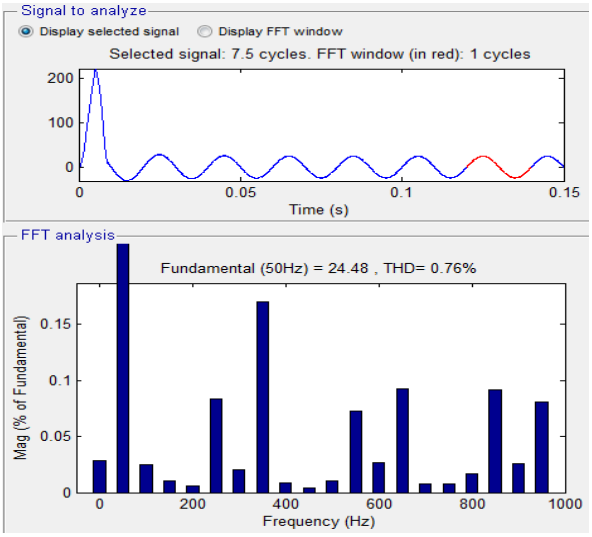

Figure 20: THD in source current

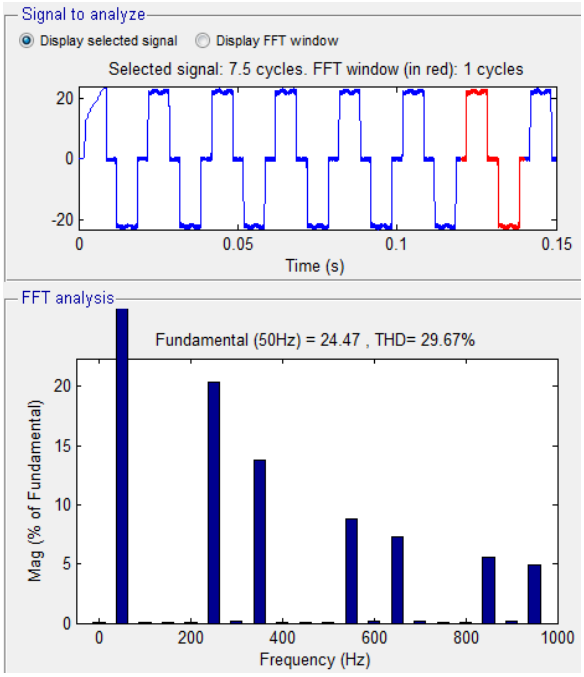

Figure 21: THD in load current

Harmonic distortion (with respect to fundamental) in source current and load current are shown in figure 20 and figure 21 respectively. The load is non-linear in nature and distortion is 29.67% and distorts the source current too. Compensating signals from parallel DSTATCOM refines the source current and distortion in source current is 0.76%.

c) Common DC-Link fed Parallel DSTATCOM and variable load condition

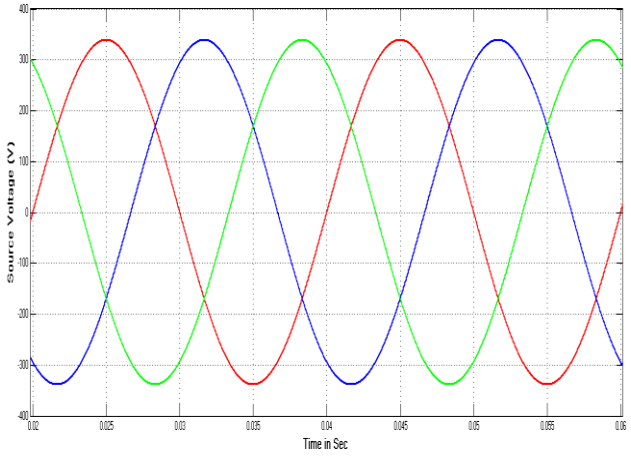

Figure 22: Three-phase source voltage

Figure 22 shows the three-phase source voltage waveform. The source voltage is balanced with no harmonic distortion though the load is varied. Source voltage has peak magnitude of 340V.

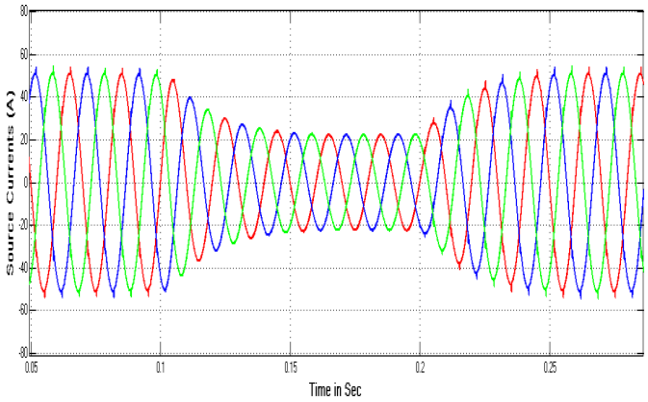

Figure 23: Three-phase source currents

Three-phase source currents are shown in figure 23. Load is varied from 0.1 seconds to 0.2 seconds. During this time, the source current decreases as the load decreases.

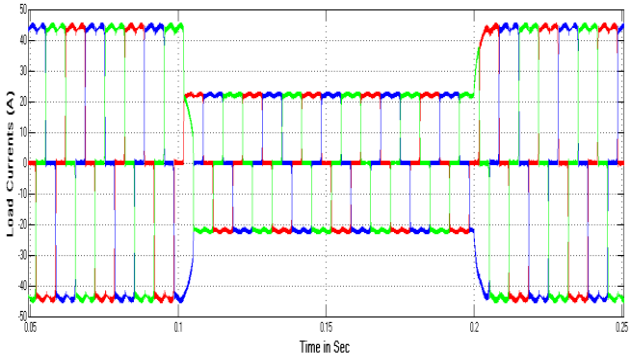

Figure 24: Three-phase load currents

The load is varied (decreased) from 0.1 seconds to 0.2 seconds. Figure 24 shows the three-phase currents drawn by the load. The load is non-linear in nature and hence load current is distorted. As the load decreases, current drawn by the load also is decreased as in figure 24.

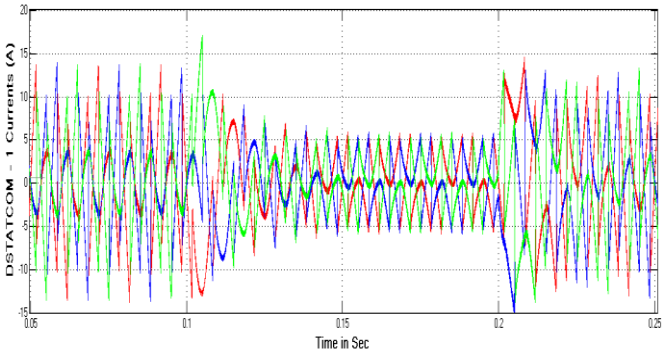

Figure 25: Compensating currents from DSTATCOM-1

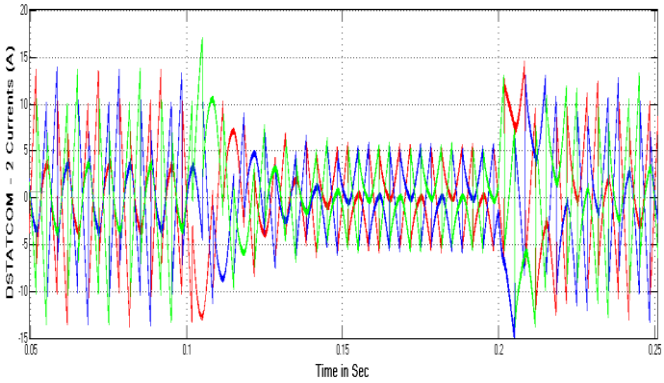

Figure 26: Compensating currents from DSTATCOM-2

Figure 25 and figure 26 illustrates the compensating currents induced to point of common coupling by DSTATCOM-1 and DSTATCOM-2 respectively, to refine the source current and ensure that the distortion of source current is within standard limits. As the load is decreased, compensating currents adjusts according to the required compensation.

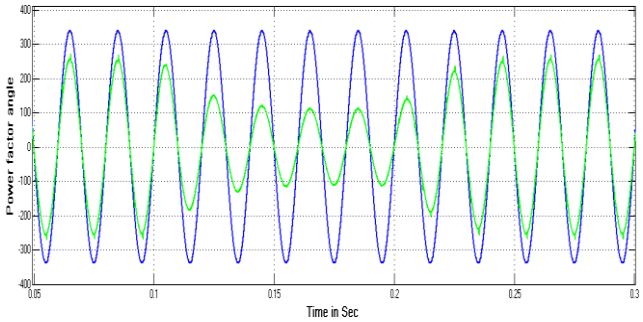

Figure 27: Power factor angle between the source voltage and source current

Figure 27 shows the power factor angle between the source voltage and source current. Source voltage and source current are not displaced with respect to phase angle and power factor tends to nearer unity.

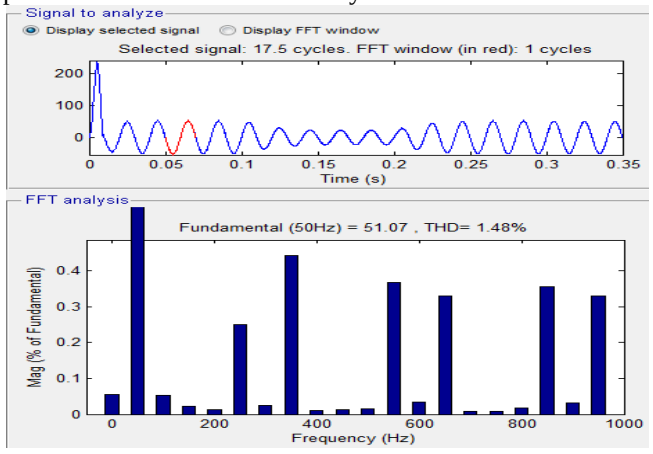

Figure 28: THD in source current

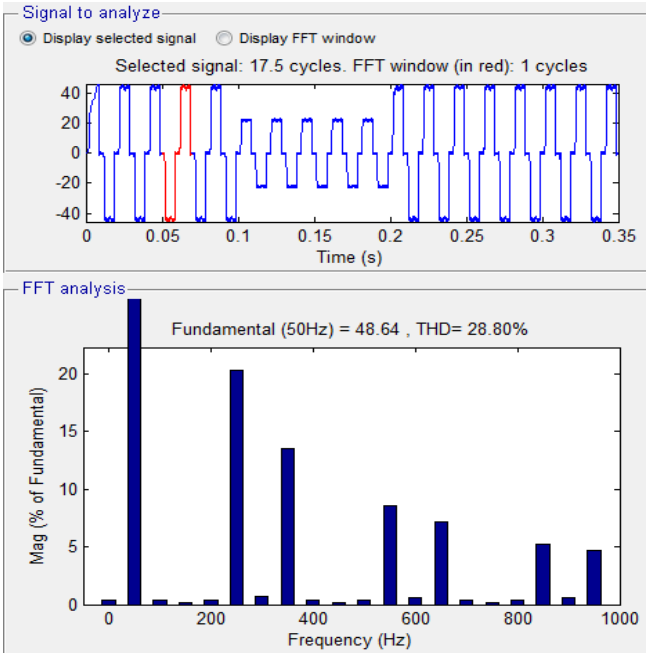

Figure 29: THD in load current

Harmonics distortion (with respect to fundamental) in source current and load current are shown in figure 28 and figure 29 respectively. The load is non-linear in nature and distortion is 28.80% and distorts the source current too. Compensating signals from parallel DSTATCOM refines the source current and distortion in source current is 1.48%. Table-1 illustrates the harmonic distortion analysis of isolated DC sources fed DSTATCOM and common DC-Link fed DSTATCOM working under constant load. Table-2 illustrates the number of DC sources required and number of voltage sensors required for isolated DC sources fed DSTATCOM and common DC-Link fed DSTATCOM.

Table-1: THD analysis

[1] THD (Constant Load Case)	[2] Source Current	[3] Load Current
[4] Isolated DC sources fed DSTATCOM	[5] 0.86 %	[6] 29.57 %
[7] Common DC source fed DSTATCOM	[8] 0.76 %	[9] 29.67 %

Table-2: Number of components

[10]	[11] Isolated DC sources fed DSTATCOM	[12] Common DC source fed DSTATCOM
[13] Number of DC Sources	[14] 2	[15] 1
[16] Number of voltage sensors	[17] 2	[18] 1

VI. CONCLUSION

This paper presents a common DC-Link fed parallel DSTATCOM for power quality improvement in the power distribution system. In conventional parallel DSTATCOM, two individual DC sources feed the two DSTATCOMs. The conventional parallel DSTATCOM topology increases the number of voltage sensors used to control the DC voltage. An increase in number of sensors increases the cost. Common

DC-Link fed parallel DSTATCOM requires only one sensor resulting in less maintenance besides reducing the cost. The advantages of common DC-Link fed parallel DSTATCOM are presented. The proposed system with common DC-Link fed parallel DSTATCOM is tested with variable and constant load operations. Harmonic distortion in source current of power system with individual DC-Link fed parallel DSTATCOM and common DC-Link fed parallel DSTATCOM are tabulated and distortion is within standard limits.

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