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A 3.3V, 24dBm CHT Integrated CMOS 180nm Power Amplifier for NB-IoT Application

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Abstract*: In this project, a 180 nm capacitive harmonic termination (CHT) CMOS-based power amplifier (PA) is designed for the Narrow-Band Internet of Things (NB-IoT) application. The PA's aimed operating frequency is between 1.9 GHz and 2.1 GHz. At schematic level simulation, the PA provides a power gain of 14 dB and a compressed output power of 24 dBm. With a resulting peak OIP3 of 33 dBm, the average power added efficiency (PAE) achieved is 40 %. The CMOS PA operates with a biasing gate voltage of 1.2 V under the voltage headroom of 3.3 V. The CHT CMOS PA provides good efficiency with negligible trade-off between linearity and output power.

Keywords: CMOS, NB-IoT, Class-J, power amplifier, linearity

I. INTRODUCTION

Cyberspace communication system design has recently led to the growing demand for wireless devices. In the rapidly increasing wireless communication network, low-power consumption devices are required to maintain and prolong battery life [1][2]. Narrow-band Internet of Things (NB-IoT) launched IoT applications based on a 3GPP standard based on low-power wide area.

The power amplifier (PA) should be effective in terms of efficiency and linearity across the required power level in order to provide an efficient and reliable data exchange between the RF receiver and transmitter in the transceiver system. CMOS PAs have been extensively studied to fulfill and satisfy low cost specifications for miniature range transceivers [3][4]. Due to the strict protocol requirements and the massive trade-off between efficiency and linearity in the CMOS process, the design of CMOS-based PAs has become arduous and challenging compared to low-trade GaAs-based Pas [5]. An optimum impedance matching network is needed to balance the trade-off between efficiency and linearity in CMOS Pas [6].

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By applying a precise impedance matching network between the main PA input and output stage, the optimum efficiency, linearity and output power can be obtained. The input matching network is needed to convert the 50-ohm input impedance into the optimum impedance seen at the gate of the main PA transistor to achieve optimal results.

Furthermore, to transform the drain impedance of the main PA transistor into 50-ohm output impedance, the output matching network is necessary. A highly efficient CHT PA is presented in this research, with a π input matching network and a LC output impedance network. Section II summarizes the PAs design methodology, while section III explains the findings of the schematic level simulation. Finally, the conclusion is presented in section IV.

II. DESIGN METHODOLOGY

A. Analysis of Output Impedance for CHT PA

The Class-J was first introduced by Cripps in 2006 [7]. The efficiency and linearity of the class-J PA is equivalent to that of the class-AB PA. Moreover, the frequency band that restricts the transmission line to short harmonics is not essential in which it contributes to the Class-J PA broadband operation [8]. By implementing the reactive harmonic termination technique, the efficiency in class-J PA is improved. A Class-J CMOS PA's basic schematic is depicted in Fig. 1. For the PA, a deep-class AB operation is configured to rectify the current waveform produced at the output signal.

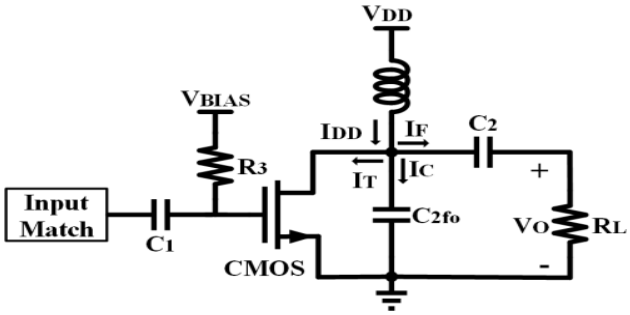


Fig. 1. Schematic of a CMOS class-J PA.

Therefore,

$$I_T = \begin{cases} -I_{\max} \sin\theta, \pi < \theta < \pi \\ 0, \pi < \theta < 2\pi \end{cases} \quad (1)$$

The fundamental current component through the output impedance matching network is given as:

$$I_F = I_1 \sin(\theta + \phi) \quad (2)$$

where ø exemplifies the output matching network's phase deviation. I_1 denotes the fundamental current. The current, I_C that flows through C_{2fo}, is:

$$I_C = I_{DD} - I_F - I_T \tag{3}$$

where $I_{DD} = I_{max} / \pi$. The output voltage, *Vo* is:

$$V_o = \frac{1}{\omega C_{2fo}} \left[\int_0^{\pi} I_C \, d\theta + \int_{\pi}^{2\pi} I_C \, d\theta \right] \tag{4}$$

Hence, for conduction angle of $0 < \theta < \pi$,

$$V_{o1} = \frac{1}{\omega C_{2fo}} \int_0^{\pi} \left(\frac{I_{\max}}{\pi} - I_1 \sin(\theta + \phi) - I_{\max} \sin\theta \right) d\theta$$
$$= -\frac{1}{\omega C_{2fo}} \left(I_{\max} + 2\, I_1 \cos\phi \right) \tag{5}$$

The out-of-phase current and voltage are indicated by the negative sign. For conduction angle of $\pi < \theta < 2\pi$, I_T in (3) is equal to 0. Thus,

$$V_{o2} = \frac{1}{\omega C_{2fo}} \int_0^{2\pi} \left(\frac{I_{\max}}{\pi} - I_1 \sin(\theta + \phi) \right) d\theta$$
$$= \frac{1}{\omega C_{2fo}} \left(I_{\max} + 2\, I_1 \cos\phi \right) \tag{6}$$

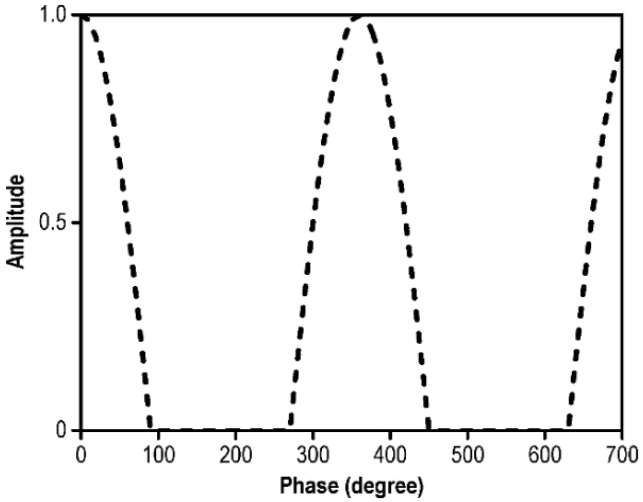
Fourier analysis was performed for the output voltage components of Vo1 and Vo2, and is given by V1 and V2 which is shown in (7) and (8). It can be perceived on the basis of (7) and (8) that the imaginary part of V1 is positive, while the imaginary part of V2 is negative. Therefore, the output impedance should be in a complex form with positive reactance. Another condition allows the impedance of the 2nd harmonic to be capacitive for class-J operation.

$$V_1 = \frac{1}{\omega C_{2fo}\pi} \left[I_{\max} \left[-2\sin\theta + \frac{1}{\pi}(\cos\theta + \theta\sin\theta - 1) \right] - I_1 \left[\sin\theta\cos\phi + \frac{1}{2}\theta + \frac{1}{4}(\sin 2\theta \cos\phi (1 + \cos 2\theta)) \right] \right]$$
$$+ j \frac{1}{\omega C_{2fo}\pi} \left[I_{\max} \left[\frac{1}{\pi}(\sin\theta - \theta\cos\theta - 2(1 - \cos\theta)) \right] - I_1 \left[\cos\theta(1 - \cos\theta) - \frac{1}{2}\left(\frac{1}{2}\cos\phi(1 - \cos 2\theta) \right) - \sin\theta\left(\theta - \frac{1}{2}\sin 2\theta \right) \right] \right] \tag{7}$$

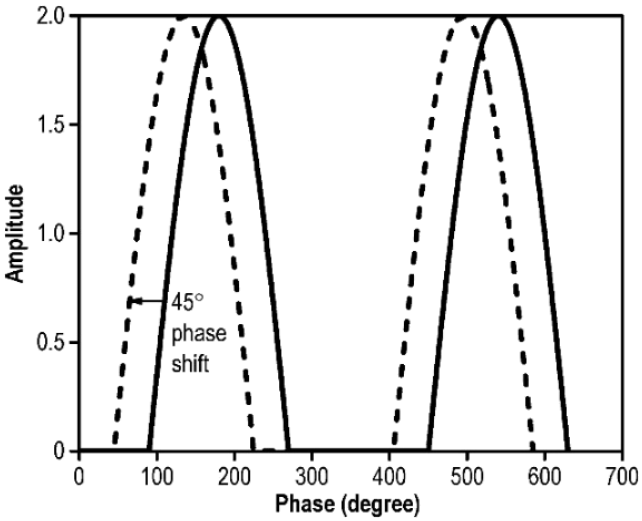
$$V_2 = \frac{1}{\omega C_{2fo}\pi} \left[I_{\max} \left[\frac{1}{\pi}\left(\frac{1}{2}\theta \sin 2\theta - \frac{1}{4}\cos 2\theta + \frac{1}{4} \right) - \sin 2\theta \right] + I_1 \left[\sin(\theta\cos\phi) - \frac{1}{3}\sin\phi - \frac{1}{6}\sin(3\theta\cos\phi) - \frac{1}{2}\sin 2\theta\cos\phi \right] \right]$$
$$- j \frac{1}{\omega C_{2fo}\pi} \left[\frac{1}{2} I_1 \left(\begin{array}{l} \cos\phi[1 - \cos 2\theta] + \cos\phi[1 - \cos\theta] - \frac{1}{3}\cos\phi[1 - \cos 3\theta] \\ -\sin\theta\sin\phi + \frac{1}{3}\sin 3\theta \sin\phi \end{array} \right) - I_{\max} \left(\frac{1}{2\pi}\left(\frac{1}{2}\sin 2\theta - \theta\cos 2\theta \right) + \cos 2\theta - 1 \right) \right] \tag{8}$$

B. Analysis of CHT PA

To conduct class-J operation from deep class-AB mode, the voltage waveform in the time domain has to be shifted. The shift in voltage waveform is contributed by the reactive components of (7) and (8). A half-wave rectified current waveform is depicted in Fig. 2 (a). Fig. 2 (b) exemplifies that the introduction of a capacitor harmonic termination provides a 45° shift in the voltage waveform. Equation (9) and (10) elucidate the characteristics of the current and voltage waveforms.



(a)



(b)

Fig. 2. (a) Half-wave rectified current waveform. (b) Modification of the voltage waveform.

$$I(\theta) = I_{\max}\left(\frac{1}{\pi} + \frac{1}{2}\cos(\theta) + \frac{2}{3\pi}\cos(2\theta) + ... \right) \tag{9}$$

$$V(\theta) = \pi V dc \left(\frac{1}{\pi} - \frac{1}{2}\cos(\theta + \delta) + \frac{2}{3\pi}\cos(2(\theta + \delta)) - ..... \right) \tag{10}$$

where δ is the phase shift of the voltage waveform.

In order to realize a class-J mode operation, the proportion of the 2nd order harmonic voltage and fundamental voltage, V_{2fo} / V_{fo} should be *cos* (45°)/2. Therefore, if V_{fo} = √2/2, then V_{2fo} = -1/4 and the 2nd order harmonic impedance is obtained from (11).

$$Z_{2fo} = \left(\frac{3\pi}{8}\right) \cdot R_{opt} \angle -90° \qquad (11)$$

C. Proposed Architecture

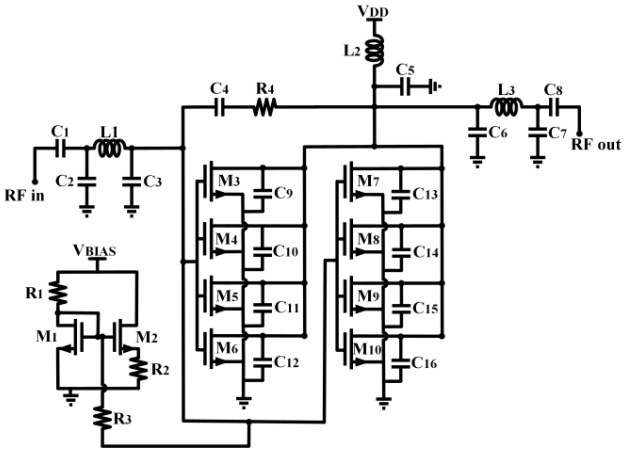


Fig. 3. Circuit architecture of the proposed CHT PA.

Fig. 3 shows the schematic of the proposed 180 nm CMOS CHT PA. The PA's quiescent current is 120 mA. As illustrated in Fig. 3, the inductor, L_1, and capacitors, C_1, C_2 and C_3 are the input impedance matching network. Meanwhile, the output impedance matching network comprises of L_3, C_6, C_7 and C_8. The capacitors, C_1 and C_8 act as the DC block for input and output stage. The inductor, L_2 is the RF choke for the PA and choke's high-quality factor helps improve filtering functionality. Noise from the power supply to the RF path is decoupled by the capacitor, C_5, in which it improves the power-added efficiency (PAE) of the PA. Capacitor, C_4 and resistor, R_4 is a RC feedback circuit utilized to improve the stability of the PA.

The conversion mechanism of DC power supply into output signal deliverability to the load reflects the PA's efficiency. This strictly influences the relationship between gain and output power as shown in (12):

$$PAE = \frac{G}{P_{DC}} X100\% \qquad (12)$$

where G = P_{out} – P_{in}, in which P_{out} and P_{in} refers to the output and input power respectively. G represents the gain of the PA.

III. SIMULATION RESULT

The proposed CMOS CHT PA is simulated at three different frequencies, which are 1.90 GHz (low frequency), 1.95 GHz (center frequency) and 2.10 GHz (high frequency) respectively. The s-parameters and stability K-factor are shown in Fig. 4. The small signal gain (S21) obtained is higher than 14 dB with input return loss (S11) of lower than -9 dB and output return loss (S22) of lower than -10 dB at all three frequencies aforementioned. The PA architecture is unconditionally stable up to 3 GHz which is replicated by the stability K-factor of more than 1.

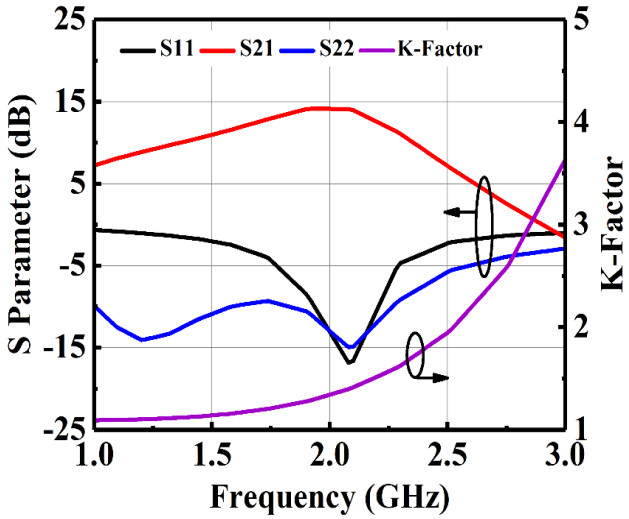


Fig. 4. S-parameter and stability factor performance of the proposed class-J PA.

Fig. 5 depicts the power gain and PAE performance of the PA across the output power for different frequencies. The power gain achieved is higher than 14 dB, while a peak PAE of 40% is attained by the PA. A saturated output power of 24 dBm has been produced by the PA.

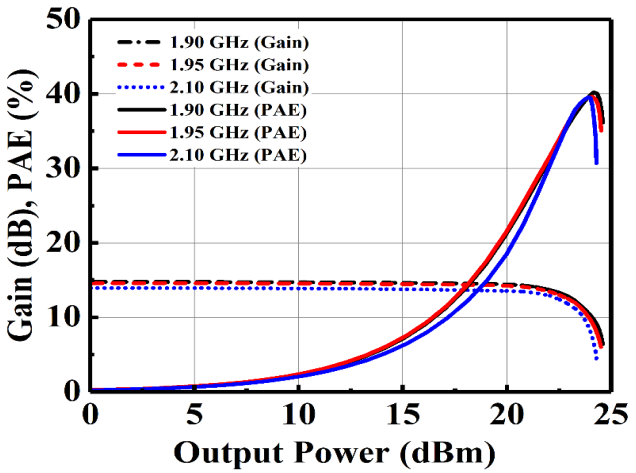


Fig. 5. Power gain and PAE performance of the proposed class-J PA.

The 3rd order output intercept point (OIP3) and the 3rd order intermodulation distortion (IMD3) achieved by the PA are depicted in Fig. 6. A maximum OIP3 of 33 dBm is achieved across the frequencies. The PA achieves an IMD3 of -33 dBc up to maximum output power of 18 dBm.

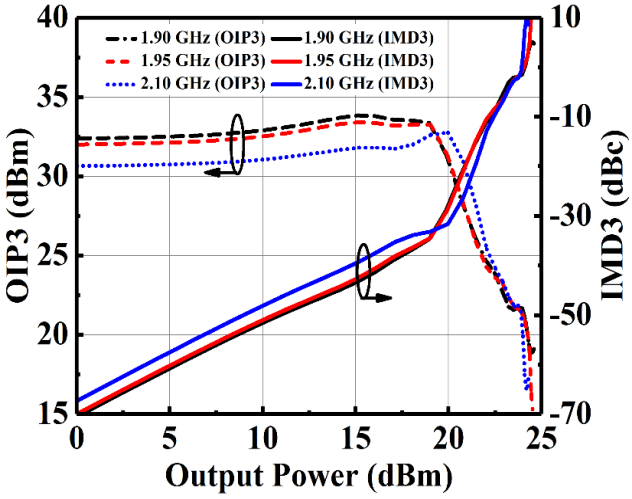


Fig. 6. OIP3 and IMD3 plot of the PA.

Table I: Performance summary of the designed PA.

Parameter	Result		
Frequency (GHz)	1.90	1.95	2.10
S11 (dB)	-9.45	-12.18	-16.60
S21 (dB)	14.08	14.29	13.93
S22 (dB)	-10.83	-11.74	-14.96
K factor	1.27	1.35	1.31
Power gain (dB)	14.75	14.59	13.94
Output power (dBm)	24.57	24.51	24.32
PAE (%)	40.19	39.58	39.54
OIP3 (dBm)	33.82	33.40	32.75
IMD3 (dBc)	-33		
Supply voltage (V)	3.3		
CMOS Technology (nm)	180		

Table II: Designed CMOS PA comparison with recent published works.

Ref	PA Tech (nm)	Max Linear Pout (dBm)	Peak PAE (%)	Gain (dB)	Freq (GHz)	Linearity	Supply (V)	Application
[14]	55	16	16	30	2.45	-33 dBc (IMD3)	1.8	WLAN
[15]	180	16.5	36.6	22	0.6	N/A	1.8	IoT
[16]	180	15.9	29.71	19.6	2.5	21 dBm (OIP3)	1.8	IoT
This work	**180**	**18**	**40.09**	**14**	**1.90 – 2.10**	**33.8 dBm (OIP3)**	**3.3**	**NB-IoT**

Table 1 shows the performance summary results of the CMOS class-J PA simulated in three different frequencies from 1.90 GHz to 2.10 GHz, while Table 2 shows the performance comparison with recent published works.

IV. CONCLUSION

In this paper, a 180 nm CMOS CHT PA J is presented. The schematic level simulation of the PA across three frequencies achieves a saturated output power of 24 dBm with a peak PAE of 40%. The PA attained a power gain of 14 dB as well as peak OIP3 of 33 dBm. The resultant IMD3 achieved is -33 dBc at maximum linear output power of 18 dBm. The PA achieves a good efficiency with minimum trade-off between the linearity and output power.

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