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Analysis of Clock trees for optimization through Multi point Clock Tree Synthesis

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***Abstract:** With rapid development of deep submicron (DSM) VLSI circuits design, building clock tree with minimal insertion delays and minimal skews has turned out to be challenging. In this Paper for a given specified block with a latency of 530 ns it is aimed to achieve a latency of 400ns and achieve optimal power. Here a Clock Tree Synthesis method is used to reduce the latency and obtain the timing closure for the given block. The analysis is made and compared in terms of clock skew and insertion delay by varying the tap points. In this process of achieving the timing closure it is observed power has optimized by selecting the appropriate tap points.*

***Keyword:** The analysis is made and compared in terms of clock skew and insertion delay by varying the tap points.*

I.INTRODUCTION

The clock network is one of the most important research points in VLSI designs. At the Deep Sub Micron (DSM) silicon technology levels, the clock network is facing new challenges [1]. First, with the development of DSM VLSI design, the device feature size continuous to shrink and the density of transistor and interconnect are increased significantly, also the circuit scale increases. While the leaks of the clock network are composed of triggers in the circuits, the scale of the problem increases rapidly with the sharp increase of the leaks. Second, as a nanometer geometrics moves into the 32 nm, 14 nm realms, the delay of interconnect becomes dominant factor of circuit performance [2], so the strict synchronization of the clock network is difficult to meet, which posed a challenge to the model and the accuracy of the clock routing.

Furthermore, an increase in the scale and the frequency of the system, the power consumption of the whole system also increases, where the power consumption of the clock network occupies about more than $1/3^{rd}$ of the total power consumption of the circuit, thus reduce the power consumption of the clock network is critical to minimize the overall system's power consumption.

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There are two normal clock distribution architectures actualized to meet the timing necessities of the system. One is traditional clock tree, which is generally utilized because of low power utilization and less routing resource utilization, as well as effortlessness of execution and simulation [3].

Notwithstanding, tree-based architecture can be very delicate to process, voltage, and temperature (PVT) variations, particularly in high-performance chip designs.

Clock mesh, the other architecture, provides better tolerance to variations [4]. By the by, with heaps of mesh nodes and uneven loads, clock mesh is hard to examine and robotize [5].

Multi-Point clock tree depict a novel clock distribution system that fills the methodology gap between the ordinary clock tree and clock mesh [6]. MPCTS is a hybrid clock structure containing the best aspects of conventional clock tree and clock mesh. Changes between the trees that sit past a collection of multi-source drivers prompt aberrations in local clock skew and addition delay, which may affect the buffer area minimization and inter-clock delay-balancing efforts adversely [7]. This paper concentrated on the performance and optimization of the multipoint CTS flow provided by a commercial EDA tool. In this paper analyze the quality of results (QoR) of the Single Point CTS and the Multi Point CTS on a real industrial design for a given specified block.

The Multipoint CTS Architecture is explained in the section 2. Section 3 elaborates the implemented approach on the given block for tap point and sink assignment. Section 4 discuss about the experimental results. Finally, conclusions in section 5.

II.MULTIPOINT CTS ARCHITECTURE

MultiPoint CTS is a hybrid method of conventional CTS and clock mesh. The structure is shown in fig 1, which consists of a mesh driven by a pre-mesh tree. Multi Point drivers connect to the mesh at a limited number of locations referred to as taps. A multi-point clock tree structure driven by the mesh consists of subtrees, each driven by a tap.

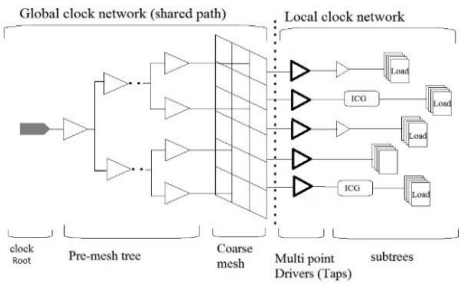

Fig. 1. Architecture of the Multi Point CTS. The vertical dotted lines divide the network into global and local clock network

A Multi Point CTS design comprises three different structures in the design.

- Pre-mesh Clock Tree
- Multi Point Mesh Fabric
- Moderately sized clock trees

2.1 Pre-mesh Clock Tree

Each buffer in the pre-mesh clock tree can drives four unique buffers, which deduces that the pre-mesh topology is completed using H-tree arrangement and routing. A H tree clock structure gives a uniform, versatile and unsurprising methods for disseminating the root clock over an expansive region.

2.2 Multi- Point Mesh Fabric

The Multi point mesh fabric identical to a power/ground mesh fabric, which is lesser in magnitude by one or two orders. The coarse fabric smoothest out any extraordinary clock arrival time contrasts from the diverse H-tree buffers that direct drive the fabric, whereby the skew evaluated at the mesh plane is effectively zero.

2.3 Moderately sized clock trees

The local sub trees are attached to the coarse mesh gives the technology its name. In this clock tree each clock buffer/inverter defined as one level. Designers may focus on the OCV execution level by focusing on the profundity of the clock tree.

The Benefit of the MPCTS is that designers can take a “divide and conquer” approach. This Method applied on the given specified block and analyzed the results.

III.IMPLEMENTATION OF MPCTS

Given with the rectilinear shaped block with an area of 2.5 mm^2 and having flip-flop count of 1521 with the initial insertion delay of 530 ns. further designs specifications are mentioned below.

3.1 Experiment Setup

The experiment is performed on a real industrial case applying 14 nm process and other characteristics are listed on the Table I. For all the experiments the flow uses the same placement results made from ICC2 tool. i.e. placement design exchange format file and placement netlist file as the input. The process starts with placing of the proper tap points i.e. proper selection of the clock points and calculating the insertion delays as per below equation. If the insertion delay is equals the targeted insertion delay i.e. the given latency the process is stopped, and target achieved. if the insertion delay is greater than it is required to increase tap points simultaneously change the locations until that required latency is achieved. Finally, analyzed the results after the CTS stage and before routing, and collect the data under the scenario operating on typical conditions.

Table-I Design Specifications

Case Name	ASIC
Process	14 nm
Number of Macro cells	26
Total Macro cell area	2475.014 μm^2
Total Std. cell area	34457.766 μm^2
Clock Routing Layers	M2-M7

Table-II Design Clock Specifications

Clock Name	CLK 2
Number of Sinks	1521
Period	0.56 ns
Frequency (GHz)	1.78
Max. Transition time (ps)	56

In this MPCTS implementation the locations of the multi-point tap drivers are chosen on the horizontal mesh traps for convenience and uniform distribution. To determine the tap point location, the first thing is collecting the information about each tap point placement and its connectivity to the corresponding flip-flop information. From this information the tap points are adjusted so the flip-flop cluster is distributed equally, the levels of sub-tree under each tap points reduces. Which in term reduces the number of buffers used by each tap to connect the flipflop.

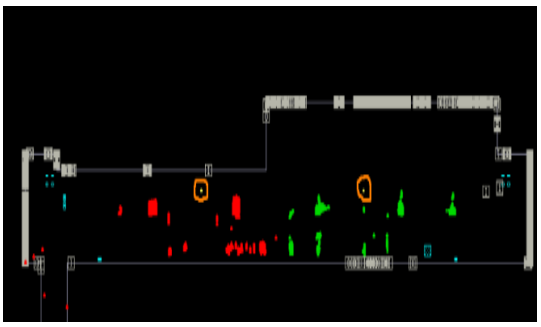

Fig 2. Loading based sink assignment

By adjusting the tap points 760 flip-fops are connected to each tap point so that it balances the skew. In this MPCTS process as the tap points are sequentially adjusted near to the flipflops the levels are reduced from 22 to the 11 levels. From each tap point with in the 11 levels all the flip-flops are connected.

When a tap driving a greater number of sinks and find that there are two pairs of these taps next to each other. To share the sinks with them, a new tap is inserted in the middle of each pair. From the outcomes, it can be observed that loading of taps turn out to be more adjusted than the original.

clock latency (or clock insertion delay) is characterized as the measure of time taken by the clock signal in heading out from its source to the sinks. To minimize the latency, observe the arrival time distribution of all sinks. Thus, to decrease the delay in the region where tap points are placed so that the driver drives to the sinks with minimum time, so that clock latency might be minimized.

IV.EXPERIMENT RESULTS

For the given block instead of single point CTS Multi point CTS method is applied to obtain the targets latency. Initially given with the clock insertion delay of 527.36 ns and the clock structure was built with the 22 levels. The clock period of that clock is 560 ns.

In Table-III it shows the Qor Results of the MPCTS method with the properly placed tap point insertion of a given specified data.

Table III: QoR of Multi Point CTS

Tap Points	1	2	3
Clock Name	CLK 2	CLK 2	CLK 2
No. of Sinks	1521	1521	1521
Clock Cells	106	73	75
No. of levels	21	14	11
Insertion delay (ps)	527.36	283.1	253.09
Global skew (ps)	56	27.44	26.03
Clock power (mw)	0.0267	0.0252	0.0253

It is observed that from the table with the single point CTS method the insertion delay is 527.36ns. with the help of 2 tap Points with the insertion delay is reduced by 40%. Global skew is reduced by 50% by inserting the two mesh root buffers. It is also observed that Insertion delay is reduced by 40%.

From the results, the difference between the Multi Point CTS and the Single Point CTS is obvious. For the single point CTS to balance the skew it uses a greater number of clock buffers, and as the clock buffers increases the power consumed by the clock network also increases tremendously.

It can be observed from the results that the power consumed by the clock network is reduced with the proper tap point placement for the given specified block. When compared with the single point CTS in multi pint CTS the clock insertion delay improved by 40%. From all the clock QoR results it is cleared that by inserting the two tap points the results are improved by 40%. But by increasing the tap points it can be observe that there are not much more improvements, so it can be concluded that tap point depends on the density of the instances and the size of the block.

4.1 Timing Reports

Timing reports are given for the design with respected to using the single point CTS and the Multi Point CTS methods. Taken an endpoint from the design and compare the insertion delay for that flop in both the cases.

From the design taken an endpoint named flop_CLK_2_584. Which is a launch flop. Below table compares the insertions delays for that sink flop in SPCTS and MPCTS method.

Table IV: Comparison of insertion delays

Sink point: flop_CLK_2_584	Insertion delay (ps) (Launch flop)
Single Point CTS	527.36
Multi Point CTS	283.1

4.1.1 Hold Timing Report in Single Point CTS Method

```
Start point: flop_CLK_2_584
        (rising edge-triggered flip-flop clocked by CLK_2)
 Endpoint: flop_CLK_2_585
        (rising edge-triggered flip-flop clocked by CLK_2)
 Last common pin: I2Cts_buffer_032/Z
 Path Group: CLK_2
 Path Type: min
 Min Timing Check Derating Factor: 1.1
 Sigma: 3.0

 Point                                  Incr      Path
 ---------------------------------------------------------------------------
 clock CLK_2 (rise edge)                0.0       0.0
 clock network delay (propagated)       527,36    527.36
 flop_CLK_2_584/CLK (flop4ul)           0.0       527.36 r
 flop_CLK_2_584/Q (flop4ul)             31.8 &    559.2 r
 flop_CLK_2_585/D (flop4ul)             6.5 &     565.7 r
 data arrival time                                565.7

 clock CLK_2 (rise edge)                0.0       0.0
 clock network delay (propagated)       479.3     479..3
 clock reconvergence pessimism          -28.7     508
 clock uncertainty                      3.0       511
 flop_CLK_2_585/CLK (flop4ul)                     511 r
 library hold time                      11.7      522.7
 data required time                               522.7
 ---------------------------------------------------------------------------
 data required time                               522.7
 data arrival time                                -565.7
 ---------------------------------------------------------------------------
 statistical adjustment                 -5.9      -48.9
 slack (VIOLATED)                                 -48.9
```

4.1.2 Hold Timing Report in Multi Point CTS Method

```
Start point: flop_CLK_2_584
        (rising edge-triggered flip-flop clocked by CLK_2)
Endpoint: flop_CLK_2_585
        (rising edge-triggered flip-flop clocked by CLK_2)
Last common pin: Cp_CLK_2 (port)
Path Group: CLK_2
Path Type: min
Min Timing Check Derating Factor: 1.1
Sigma: 3.0

Point                                  Incr      Path
---------------------------------------------------------------------------
clock CLK_2 (rise edge)                0.0       0.0
clock network delay (propagated)       283.1     283.1
flop_CLK_2_584/CLK (flop4ul)           0.0       283.1 r
flop_CLK_2_584/Q (flop4ul) <-          29.7 &    312.8 r
delay_buffer_457/Z (dly1ur)            39.9 &    352.7 r
flop_CLK_2_585/D (flop2ur)             0.0 &     352.7 r
data arrival time                                352.7

clock CLK_2 (rise edge)                0.0       0.0
clock network delay (propagated)       267.6     267.6
clock reconvergence pessimism          -0.3      267.3
clock uncertainty                      3.0       270.3
flop_CLK_2_585/CLK (flop2ur)                     270.3 r
library hold time                      15.0      285.3
data required time                               285.3
---------------------------------------------------------------------------
data required time                               285.3
data arrival time                                -352.7
---------------------------------------------------------------------------
statistical adjustment                 5.9       61.5
slack (MET)                                      61.5
```

From the timing is can be observed that for the given SPCTS method the insertion delay was 527.36ns and the skew was -48ns. With the amount of skew difference, the hold path violated With a slack of 48.9ns. With the MPCTS process the insertion delay reduces to the 283.1 ns and the skew difference was 17 ns for the flops flop_CLK_2_584 and flop_CLK_2_585. So the hold path met with the slack of 61.5 ps.

This is due to the difference in the clock path delays. It can be observed that MPCTS process can improve the insertion delay and clock skew which can make easier in timing closure of a given block.

When the farthest flop and the nearest flop to the root buffer are communicating each other. To balance the skew for those two flops, more clock buffers are added to the nearest flop. Due to this, the cell density might increase at the nearest flop which results in lack of routing tracks in that area and those routes might be detoured. It results in increasing the insertion delay of nearest flop and increases the skew between nearest flop and farthest flop. This is what happened in the single point CTS. Whereas in Multi point CTS, those two flops are connected to the nearest root buffer then it is easy to balance the skew with less no of buffers, and the insertion delay also reduced. As the insertion delay reduces, switching power also reduces.

From the fig 4.1 it is observed that clock path for the two flops. These two flops are connected to two different root buffers. Those two flops common point is clock port.

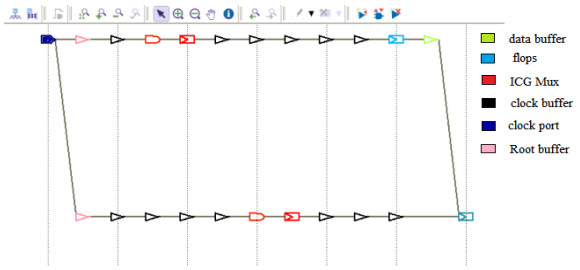

Fig. 4.1 Clock path for flop_CLK_2_585 in MPCTS

From the results it can be conclude that Multi Point CTS performs better when the target clock should cover larger area.

V.CONCLUSION

It can be concluded that by analyzing the single point CTS and the Multi Point CTS implemented with the ICC2 and prime time tool on a real industrial design. In this paper focus on the steps which can be controlled in the flow and implemented some heuristic approaches to improving the performance of multisource CTS, especially for insertion delay optimization. From the results, the proper placement for the tap points for a design are determined and that multisource CTS performs better when the target clock covers larger area. Though the results seem to be case-dependent, finally it can be concluded that insertion delay, skew and QoR may get better by performing tap and sink assignment, considering both location and timing relation of sinks. How to automate this flow is an important future research direction.

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