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Design of FinFET based 128 bit SRAM in 7nm & Various Effects near Threshold Operation for Ultra Low Power Application.

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Abstract: ***With the existing technology and survey it indicates the increasing the number of transistors count and exploring methodologies leads to innovative design in memories. In general SRAM occupies considerable amount of area and less performance due to leakage power that limits the operation under sub threshold region. The power consumption of the circuit design is primarily depends on the switching activity of the transistor that leads to increasing of leakage current at near or subthreshold operation. Some of the challenges like PVT variations, SEU, SEE, and RDF lead to reduction in performance, increasing the power, BTI, sizing, delay and yield. The research work in this paper primarily describes the challenges with the technology and effects on CMOS & Finfet designs. The second aspect of the paper is to represents the design methodologies of CMOS & FinFET models and its operation. The third part of the paper explains design tradeoff of FinFET SRAM. Final sections present a comparison of high performance, low power at normal and near threshold operation. The Comparisons is made on the basis of process parameters and made a conclusion with circuit functionality, reliability under different technologies. FinFET based SRAM's are the emerging memory trends by the performance under or near sub-threshold operation with the minimal variation in the leakage current, minimal gate delay is an alternate solution to the traditional CMOS memory designs as showed in the present work.***

Keywords: SEU, SEE, RDF, BTI, LET, RSNM, WSNM, FINFET, PR, PU.

I. INTRODUCTION

With the requirements of the customer specifications and requirements, there is a tremendous growth in the technology that leads to design the qualitative models which can satisfy the performance, reliability and Functionality. SRAM is the primary element in processor design.

The speed of operation of processor depends on the read and write functionality of SRAM. With growing technology the leakage power is the issue that needs to be considering under subthreshold operation.

A traditional CMOS SRAM designs are suffering with leakage current and performance of the circuit is effected with PVT variation, scaling effects (SEU-Single event upset, Sing event transient (SEE), Bias instability temperature (BTI)[1] and aging limits the performance of the circuit in designing level.

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The other parameters RDF(random dopant fluctuations), W/L Ratio, gate oxide thickness are the geometrical structures that leads to reduction in the reliability of the design and limits the performance of the design[1].

II. DESIGN METHODOLGY AND OPERATION

A. Operation CMOS 6T SRAM design:

The basic functionality of the SRAM has three important and essential operations ie read write and hold. These are important aspects while designing the SRAM to produce proper functionality.

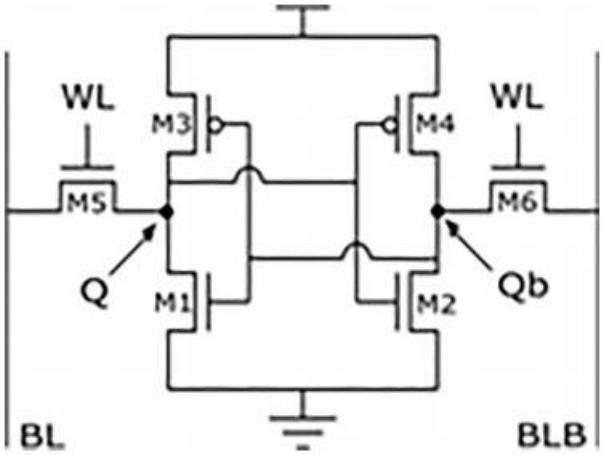

Fig. 1. 6 T SRAM cell of Electric model

Each of the operation activates some parts of the architecture. The Fig 1 represents most frequently used electrical model of 6T-SRAM having the advantage comparatively with other designs. The advantage over 4T SRAM is treated as Load less model [2], 5T is treated as port less configuration [3] to reduce the total area of the design.

The single ended 8T [4] and 10T [5] cells has designed for subthreshold operation to reduce or minimize energy consumption applications. The 13T model has designed to withstand for the radiation effects for the space applications [6].The 9T SRAM cell [7] avoids the half-select issues by eliminating the need to use read assistant circuit. All SRAM designs has an Q & Qb nodes to store a bit of data either '1' or'0' along with recharge and sense amplifier circuit to execute read and write operation. In 6T cell, the nodes Q and Qb are access only during functionality of read and write operation.

Word Line (WL) is enabled by row decoder and control the pass transistor ,that gets activated by access transistors to perform read and write operation. To store a value of bit 1, the write circuit performs the charging operation and discharges another bit line. Ie if BL=1,BLbar is 0 (BLB) is on the other end there by enabling the row decoder value across WL. Therefore Q and Qb vales are written.

The values of BL and BLB has to be pre-charged before itself. When the word line WL is high, the q is 0 and Qb is 1 there by promoting the value voltage difference of the signal will be accessed by the access transistor and presents the output. Basically SRAM cell is characterized by a) Worst delay (max read write operation), that affects operational frequency. b) Power consumed by circuit while in read or write mode c) RSNM & WSNM to estimate robustness of the cell .

B. Design Methodology of 6T SRAM FINFET design:

In order to observe the effects of nanometer technology, 128 bit FinFET SRAM is taken into consideration with a precharge circuit, sense amplifier and write driver circuit.

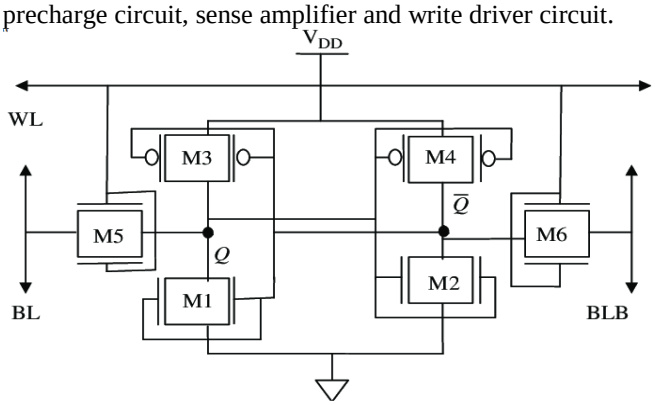

Fig. 2. FINFET 6 T SRAM design

The evaluation is made from high performance(HP) and low power(LP) (45nm) by CMOS design to the 16nm technology of CMOS with high performance and low standby power (LSTP) from 45nm to 16nm technology. Then the performance of FinFET is estimated with high performance and low-standby power from 16nm to 7nm [8]. The main parameters to bulk CMOS and FinFET technologies are represented in Tables 1 and 2 for Low Power and low standby power which holds nearer to the threshold operation. The Pull-up Ratio (PR) and Cell Ratio (CR) of 6-T SRAM sizing defines the CR is the ratio of WM1/WM5 and PR is the ration of WM3/WM5, where W is the width of transistor to achieve a balance between write ability and read stability. PR is usually to be set as 1 to improve the write ability with min sized transistor to and to reduce the size of the cell area [9]. CR is to be more than 1to improve read stability.

Table 1: CMOS design parameters

Parameter		45 nm	32 nm	16 nm
L (nm)		45	32	16
W (nm)		90	64	32
Tox (nm)	HP	1.25	1.15	0.95
	LSTP	1.8	1.6	1.2
Vth0 HP	NMOS	0.46893	0.49396	0.47965
	PMOS	−0.49158	−0.49155	−0.43121
Vth0 LSTP	NMOS	0.62261	0.63	0.68191
	PMOS	−0.587	−0.5808	−0.6862

Table 2: FINFET design parameters

Parameter		16 nm	7 nm
L (nm)		20	11
W_{FIN} (nm)		12	6.5
H_{FIN} (nm)		26	18
WF HP	NFET	4.41	4.42
	PFET	4.76	4.74
WF LSTP	NFET	4.58	4.61
	PFET	4.59	4.56

For bulk CMOS designs relation is equal to 2, where as for FinFET with one Fin. In order to estimate the performance in a systematic manner a flow diagram is represented in Fig. 3 to evaluate the electrical characteristics to in nominal and near-threshold operation.

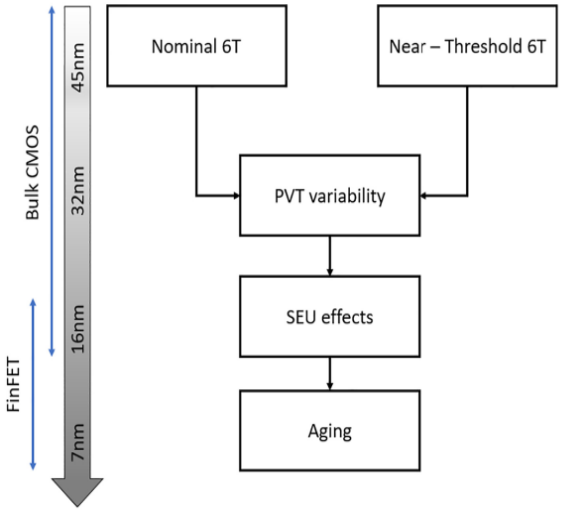

Fig. 3. Various effects in evaluation flow model

The Fig 3 represents the flow diagram of systematic evaluation process under normal or near threshold region. The sequence of SRAM operation starting from write operation ie write 0 / hold 0 / read0 continues is processed. The second of the sequence continues of write 1/ hold 1 / read 1 operation.

Writing and reading of the logical value and validating the power, timing analysis. PVT variability starts with the process of Monte Carson simulation results are executed over a normal distribution. This is the critical metric for this proportional work with a variability in voltage with ± 10% of supply voltage and temperature from 0 °C to 125 °C. The bulk CMOS has the threshold effect on the variations of process variability directly related to Vth 0 and PTM models. But the FinFET the variably on metal gate work fluctuation [10]. The Eqn (1) represents the The threshold voltage (Vth) on metal gate be expressed as Eq. (1),

$$V_t=f_{ms}+2f_f+(Q_n/C_{ox})-(Q_{ss}/C_{ox})+V_{in} \quad \text{----------} \quad (1)$$

Where QSS is charge in the gate dielectric, Cox is gate capacitance, QD is the depletion charge in the channel, fms between the gate electrode and the semiconductor, ff is Fermi potential.

$$f_f=(KT/q)\ ln\ N_A/N_i \quad \text{----------} \quad (2)$$

Eq. (2) is the Fermi potential of P type silicon, where NA is the acceptor concentration, and ni is the intrinsic carrier concentration. For ultra thin body and lightly dopes devices effects of QD and Qss on the Vth and Vth is compared to fr. Further, Vin is the additional surface voltage to 2fr to bring the required enough inversion charge to reach threshold. The Linear Energy Transfer(LET) is useful to estimate the radiation robustness starts considering the equal to 3 Mev·cm2/mg. [16], The effects are investigated to the SET of 010 and 101 in all SRAM device for minimum LET for bit variation in each technology. Aging is a factor which affects the performance. It is defined as percentage stress condition of the transistor when it is under operation. (TSP)[17].In inverter loop, In CMOS the read operation of the probability is about 50%, but in the hold condition takes the stress 98% and the sense amp will have only 1% and the read and write operation has only reaming 1%. In 128 bit SRAM from the evaluation, stress condition of the transistor is0.01% [18]

III. FINFET BASED SRAM DESIGN TRADEOFF's

Area vs. Yield:

The functionality is expected from a device when there is large amount of area by providing maximum design margins, determined by channel width (W) & length (L), supply voltage (Vdd), Threshold voltage (Vth). But when the size of the transistor is increasing, the noise margin is also increases that lead increase in the cell area.

a. Hold Margin

With the increasing technology the gate leakage current is increasing and degradation in Ion and Ioff states. In standby mode, the PMOS load transistor must be turning enough to compensate the subthreshold & leakage currents [11]. Therefore the reduction of supply voltage is needed results in reduce the static power consumption. This results in design more robust in memory designs coupled[12]. The property of the SNM defines the hold stability in standby mode. It is the min DC voltage disturbance, that is required to upset the cell state[13] and can be measured by length of the side of the maximum square that as sit as a butterfly structure by cross coupled inverters.

b. Read Stability Margin

Read noise margin can also be quantified by SNM of the cell during read operation. Cell voltage is increased from maximum to the minimum voltage of the resistive network [14], causing gain inverter gain characteristics will decrease to 0 resulting to RSNM, where the spacing between the characteristics reduces to minimum. That is the reason cell is to be treated as most vulnerable component, while read operation. Read noise margin can be increased by upsetting the pull down transistor causes to area penalty and/or increasing the gate length, results in variation in W/L ratio. This leads to increasing the delay.

c. Read margin

Read static noise margin (RSN) can be measured during the reading operation, the voltage may rise from max voltage, the characteristic will decrease [14], resulting to a reduction in separation between the butterfly curves and thus SNM reduces. Therefore size of the cell must most vulnerable to noise. This can be achieved by upsizing of Pull down transistor resulting in area penalty in area or increasing or decreasing the gate length of transistor. This leads to increasing the delay in WL, and affects the WNM.

d. Write Margin

The WNM can be increased by making the pull up device to be the size and upsizing the transistor cell minimum sized and access transistor w/l at the cell read noise margin at the cost of cell area.

e. Access Time

During the read or write operation, the WL is to be for specified time only, Performance of the operation depends on the WL value.

When WL value is minimum cell cannot successfully complete either read or write operation. For a successful read operation, when the voltage divider is able to pull up the voltage Vl below the threshold voltage of the transistor. Results into positive feedback of the transistor causes the flip state instantly changes. For a pre charge circuit with bit line operation, the sensing amplifier change the state between the lines will be developed before the wl is discharge.

Power

For a large embedded memory designs, power is the main factor and consumes larger power. The reason for the power consumption is due to short active and long idle power. Standby power is the important factor in large designs. Therefore the leakage power is essential in the low power VLSI circuits designs. This can be suppressed by increasing the channel length or by higher threshold voltage of transistor. But higher length leads to penalty in the cell area and increases the WL and capacitance of BL, leads to increase in the access time and power. Higher transistor threshold improves the read and write noise margin but impacts on the access time and min read current. Increasing the threshold voltage of NMOS leads to stronger impact on Vth[15].resulting in higher read and write noise margins. Normally maximum standby power is set to be lowered as (e.g. 0.4-0.5V) of the Vth in a process. Then the supply voltage to be set higher. Therefore some of the designing techniques to be used to reduce the leakage as well by using sleep transistors, body biasing. But these techniques reduce density and compromise stability.

IV. CHALLENGES OF THE FINFET DESIGN

The experimental results come with a broad set of data. The performance indication of the circuit depends on some factors and compared with the same technological nodes. The factors affecting the SRAM design are the PVT Variations, radiation robustness and aging. Functionality is evaluated under high performance (HP) and low power (LP) in normal operation indicated in fig: 3,4 and most effected devices are evaluated in near sub threshold operation represented in fig 5.

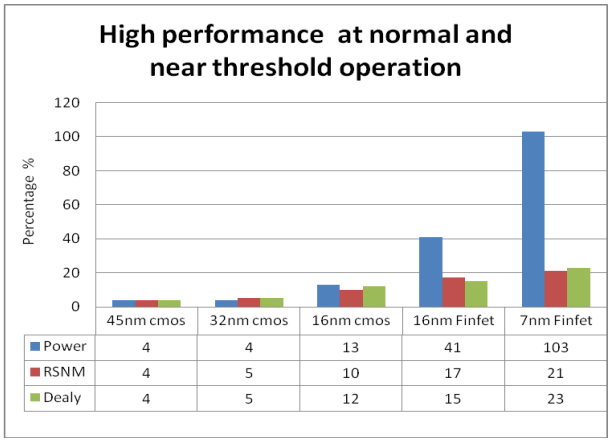

Fig3: High performance at normal and near threshold

Read static noise margin (RSNM) is effected more than the hold and write static noise margins (WSNM). The power is greatly affected in FinFET technology nearly 200% . But the read and write operations were effected mostly under sub threshold operation with the device scaling. Regarding the circuit variability in voltage between +10% and -10%.The performance of the power is effected more in -10% than the +10% is showed in fig 6,7.FinFET is the technology is higher robustness to voltage variability and has higher voltages than in low power 16nm with threshold reduction 90% .

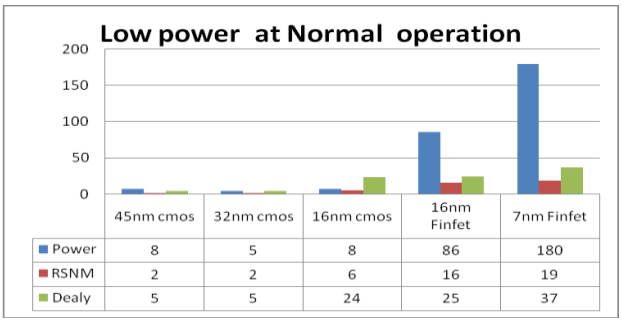

Fig4: Low power technologies at normal operation

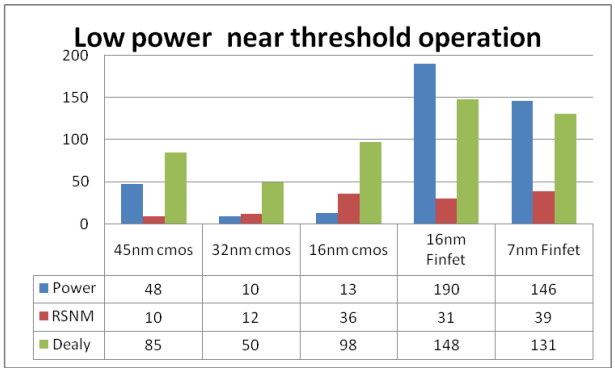

Fig 5: Low power technologies at near threshold operation

With the technology evolution, the circuit remains affecting the functionality. The circuit sensitivity is almost constant for all the technologies of 45nm.32nm, 16nm of CMOS and 16nm,7nm of FinFET technology. From the analysis it is possible to predict Q and Qb are most sensitive. This functionality evaluates the linear energy transfer function (LET) that provides a flip operation on 6T SRAM cell. Fig 8 indicates with the sensibility variations the technology reductions. The FINFET designs shows the twice of the reliability in high performance with low power approximately 65%. but the 7nm indicates the same level of variation in high performance devices.Table:3 shows the aging of the simulation for cmos technology. As expected. The Vth indicates the impact on negatively in the timing and power consumption is effected positively indicated in fig 6, 7.

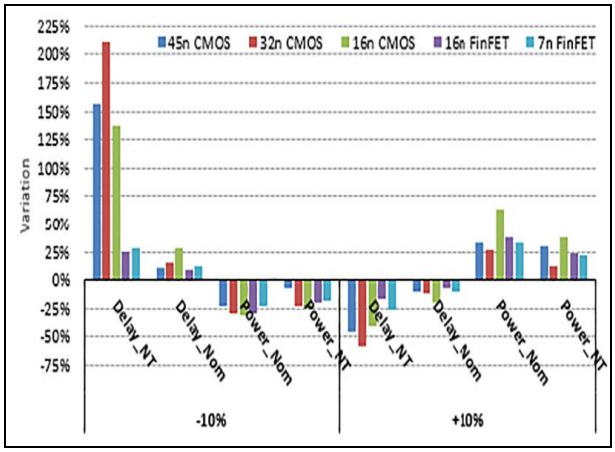

Fig:6 voltage variability in high performance node

Table 3: Relation between Delay (%) Power consumption

Bulk CMOS technology	Delay variation (%)	Power consumption variation (%)
45 nm HP	+2.4%	−15.1%
45 nm LP	+3.9%	−15.1%
32 nm HP	+3.4%	−13.0%
32 nm LP	+5.3%	−9.2%
16 nm HP	+6.6%	−36.0%
16 nm LP	+8.4%	−12.1%

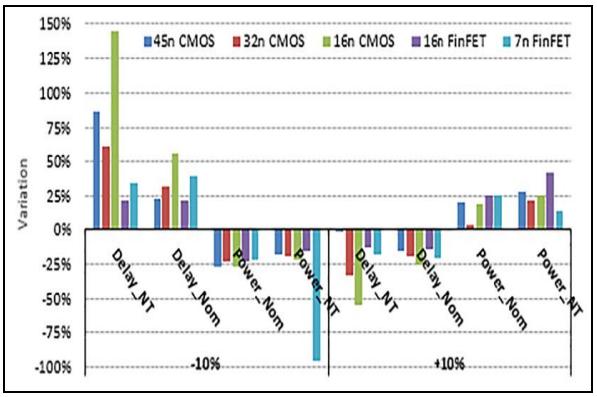

Fig: 7 Voltage variability on Low power technology

Therefore this is taken as a reference and smaller technologies, which are more affected and influenced and by aging. Therefore from the results one can understand the delay degradation is approximately 40% in each technology nodes with the same threshold voltage. It is impacted more on low power devices than the high performance devices. Results indicate the difference in reduction of the technology scaling.

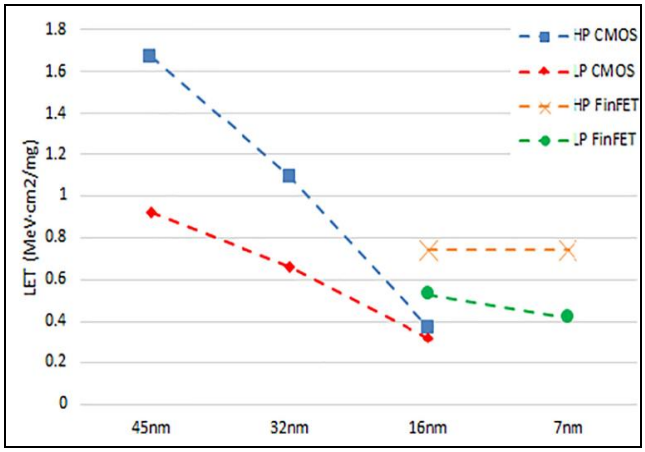

Fig: 8 Linear energy transfer is minimum at 0 node.

V. RESULTS & DISCUSSIONS

A comparative analysis is made on the performance of CMOS & FinFET SRAM models. Critical analysis is based on the functionality of 128bit SRAM on design parameters and estimating high performance, low power at normal and near threshold operation. In cmos design parameters the width of the parameter is to be selected normally twice of the length. Where as in FinFET technology, the width is approximately half of the value.

Table 4: Power, RSNM, Delay Variations (%)with technologies

Technology	45nm	32nm	16nm	16nm	7nm
Design	CMOS	CMOS	CMOS	FINFET	FINFET
High performance at normal and near threshold in %					
Power Decrease		1	3	10	26
RSNM Drop		1.2	2	4.2	5.1
Delay Reduction		1.2	3	3.2	3.75
Low power technologies at normal operation in %					
Power Decrease	16		16	16.4	36
RSNM Drop	1		3	8	10
Delay Reduction	1		5.8	5	7.4
Low power technologies at near threshold operation in %					
Power Decrease	4.8		1.3	19	14.6
RSNM Drop		1.2	3.6	3.1	3.9
Delay Reduction	1.7		1.96	2.96	2.62

The voltage variability of high performance with +10% and -10% variation in the supply voltage provides the accurate performance. But in 16nm shows the higher reduction in FinFET low-standby power with -10% of VDD at near-threshold regime reduction that close to 90%. Linear energy transfer is a function the investing the effects of changing the states from 010 to 101in all devices of SRAM. At 45nm technology high performance and low power is twice of the difference and the 32nm difference is the minimum, whereas at 16nm cmos technology difference is very minimum.

VI. CONCLUSION

The work presented here is the 6T of 128bit SRAM with adequate amount of information on behavior under PVT variability, radiation by SEU and aging under different technologies. The results show a fair comparison and highlighting the behavior of the SRAM to the next generation devices. The higher technology nodes have problem with the process variability that effect with process parameters and challenges of power and delay. The RSNM is the parameter that is affected by PVT variations mostly. At the high performance voltage operations the power consumption has an exponential characteristics, but minimum in lower technologies. FinFET SRAM has a highest robust to voltage variation effects. In high performance showed the highest variation than the low power technology. Where as in FinFET technology the function of LET is gradually varied from 16nm technology to 7nm technology. Therefore 6T SRAM can be greatly used in memory design for high-performance, but with a little care on the other end in process variability. Process parameters can be improved by adopting advanced digital techniques to improve the performance in process variability & reliability. The great efforts to be taken care to improve the SRAM operation and performance to make the design more meaningful.

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