Real Time Sobel Edge Detection Based on Reconfigurable Computing

Priscilla Whitin, V. Jayasankar

Abstract: ***Edge detection is a fundamental operation in many image and video processing applications. It is used in various fields like industries, aerospace, surveillance, medical fields, traffic monitoring system, lane detection, driverless vehicles, crack detection in roads and several other applications. Most of the edge detection algorithms are software based but in real time applications these are not efficient hence in this paper we have explored about Hardware platform. The reason for selecting Sobel edge detection operator is it incorporates both the edge detection and a smoothing operator to provide good edge detection capability in noisy environment. This design uses Verilog HDL language for design and Vivado is used for simulation.***

Keywords: Edge detection, FPGA, Sobel, RGB, grayscale

I. INTRODUCTION

Edge detection is used to detect outline of objects, boundaries, extract certain required information about position and size of objects. It is the most basic step in computer vision and other image processing applications [1-5]. It is also used for reducing the data to be processed by selecting only those area where we are interested to analyse .There are two domains of edge detection algorithm: gradient based and Laplacian based [6]. The gradient based methods are Sobel operator, Prewitt operator and Robert operator. The complexity of gradient based methods are less complex compared to Laplacian methods, hence we have used sobel operator since it performs better than Prewitt for real time edge detection. Certain real time image processing is time consuming. Field programmable gate array (FPGA) have arrays of logic blocks that enable parallel processing in edge detection thereby reducing the time consumption [7] .With lot of advances in VLSI technology, hardware implementation is made possible which results in parallelism and faster processing.[8]

II. SYSTEM DESCRIPTION

This section describes overview of the proposed implementation. Fig. 1 shows the block diagram of the design which involves a camera sensor, camera module, sobel module, HDMI module and LCD. The camera sensor captures the still image which is in bayer pattern then camera module translates the image to RGB format and sobel module handles it. The RGB format is transformed to grayscale format before processing the data. Sobel module then performs the gradient calculation to identify the pixels which are edge pixels and again image is converted to RGB format for displaying purpose, then the image containing only edges is sent to LCD for display through a HDMI interface.

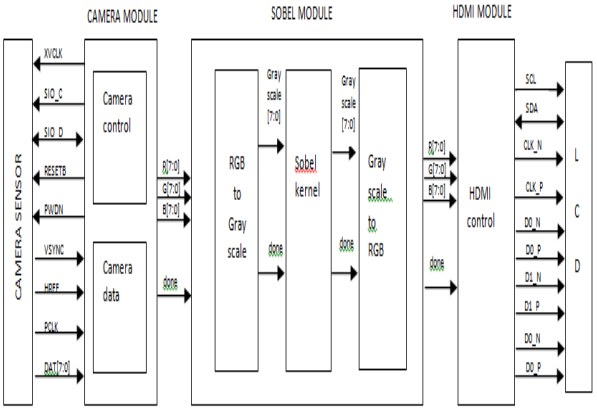

Fig.1 .System block diagram

A. Grayscale Image Transformation

The image from camera is in bayer pattern which is converted to 24 bit RGB format .RGB format consists of three 8 bit representation for representing the luminance of each colour i.e., red ,green and blue respectively. The RGB format is further converted to grayscale format which is only 8 bits, all three colour in a grayscale image are represented using the same intensity value. Still a grayscale format gives the whole idea of the picture but processing data is reduced and the speed will be increased. For RGB to grayscale transformation, there are two method: Average method and luminosity method. In average method the average of all three colour intensity is taken, in this luminous method is used. Luminosity equation is given as follows:

$$Y = 0.299*R + 0.59*G + 0.11*B \quad (1)$$

Implementing floating point in FPGA is very tedious hence equation (1) is modified as shown below

$$Y = (R >> 2) + (R >> 5) + (G >> 1) + (G >> 4) + (B >> 4) + (B >> 5) \quad (2)$$

$$Y = \frac{R}{2^2} + \frac{R}{2^5} + \frac{G}{2^1} + \frac{G}{2^4} + \frac{B}{2^4} + \frac{B}{2^5} \quad (3)$$

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Y = R (0.25 + 0.03125) + G (0.5 + 0.0625) + B (0.0625 + 0.03125) (4)

Y= R (0.28125) + G (0.5625) + B (0.09375) (5)

Equation (1) is approximated as equation (5) and implemented in FPGA by using only shifters and adders instead of floating point multiplications.

f(x-1,y-1)	f(x,y-1)	f(x+1,y-1)
f(x-1,y)	f(x,y)	f(x+1,y)
f(x-1,y+1)	f(x,y+1)	f(x+1,y+1)

B. Sobel Edge detection Algorithm

In sobel method, there are two template Gx and Gy are used, Gx detects edges in horizontal direction and Gy detects edges in vertical direction respectively.

$$Gx = \begin{bmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{bmatrix}$$

$$Gy = \begin{bmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{bmatrix}$$

Consider the pixel value of 3x3 sub window of an image function as shown in fig.2

f(x-1,y-1)	f(x,y-1)	f(x+1,y-1)
f(x-1,y)	f(x,y)	f(x+1,y)
f(x-1,y+1)	f(x,y+1)	f(x+1,y+1)

Fig.2.A 3x3 sub window image

Applying the sobel template on the two dimensional image function yields gradient expression as given by equation (6) and (7)

Gx = fx(x,y) = f(x-1,y+1) + 2(f(x,y+1) + f(x+1,y+1) - f(x-1,y-1) - 2f(x,y-1) - f(x+1,y-1) (6)

Gy =fy(x,y) = f(x+1,y-1) + 2(f(x+1,y) + f(x+1,y+1) - f(x-1,y-1) - 2f(x-1,y) - f(x-1,y+1) (7)

$$G = \sqrt{Gx^2 + Gy^2}$$

In FPGA it is complicated to compute square root function, so we change the function

Finally |G| = |Gx| +|Gy| (8)

The magnitude |G| is collected in a matrix called G(x,y).Each pixel value in G(x,y) is compared with a set threshold value to determine whether the matrix element is an edge pixel or not. The threshold value is preset based on light intensity and application purpose.

2.3. FIFO buffer

The image pixels are stored in FIFO buffers which facilitate sobel gradient calculation.Consider the 5x4 image given in fig.3 .To calculate the gradient for P5 all pixels P1 to P9 are involved.The third rows will be available only after the first 2 rows are outputted ,hence to store the remaining pixels in those row two FIFO buffers are used .Each FIFO buffer will store pixels from one row as shown in fig. 3. FIFO buffers are used to store the two rows of matrix element since to calculate a gradient pixel, 9 neighbouring pixels are required .For edges of image there are no neighbours hence a border of single line pixel is attached to the original image for calculating the gradient of image edge and corner pixel of the image.

P1	P2	P3
P4	P5	P6
P7	P8	P9

Fig .3. A 5 x 4 image

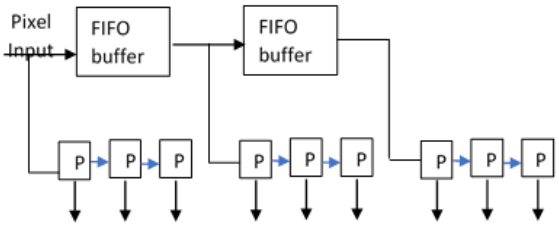

Fig.4. FIFO Buffer

III. SIMULATION AND RESULT

The Verilog code describing the design was executed on vivado 2018.3 version for various 640x480 pixel image .zhang et al[8] have increased the direction of gradient direction ,so that wrong edge detection does not happen along with vertival and horizontal direction ,45° and 135° directions also included .In this paper, threshold was set to 60,and the edge were detected as given in fig.4.mamta mittal et al [9] have used multiple threshold for better error handling.The original colour image was first converted to grayscale image and then then given as input for sobel gradient calculation based on threshold set the edge detected image was obtained.

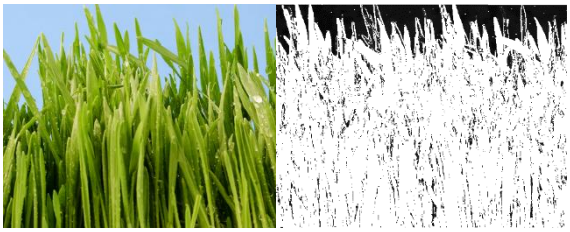

Fig. 4.Original image and edge detected image

Table 1 shows the logic utilization by different modules in the design. It shows that only a small amount of FPGA resources are utilized from the available resources to implement this design. This ensures we have enough resources available for implementing other modules as well.

Table 1.Hardware logic resource utilization

	Sobel Mod	Grayscale to RGB	RGB to Grayscale	Sobel Kernel
ce LUTs (10400)	584	0	24	560
Slice registers(20800)	325	9	9	307
Bonded IOB(170)	45	0	0	0
Bufgcntl(32)	2	0	0	0

IV. CONCLUSION

This paper illustrates the implementation of real time edge detection using sobel algorithm. The proposed system is implemented on hardware FPGA which enables faster processing speed, parallel processing and high reliability. Different test images were used for evaluation .In future work it can be extended for live edge detection in video format.

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