Design and Implementation of Sequential Circuit Based on Reversible Gate in Emerging Technologies for HCI

Ravitesh Mishra, Sanjeev Gupta

Abstract:- Affective computing is a growing research area used to develop the system in such a way to recognize, interpret, process and simulate the human emotions in a systematic manner. The main application of Affective computing is the human computer interaction, in which the communication between the human and the machine enhances by giving an appropriate response to the user in an effective and empathic manner. This paper mainly concentrates on the systems which can extract the previous, past and present information based on sequential circuit. Design sequential circuit (SC) with the help of reversible gate (RG) because RG is an emerging technology and consume low power and area. The SC is implemented Xilinx software and calculates parameters.

Keywords: HCI, RG, SC, Low Power

I. INTRODUCTION

The investigation of human PC communication was taken in the mid of 1990s as the World Wide Web, email, and Windows 95 burst upon the scene. As per relationship for registering apparatus “discipline worried about the plan assessment and execution of intelligent PC frameworks for human use and with the investigation of significant marvels encompassing them” (1992). The Dix says "human PC cooperation is the investigation of individuals, PC innovation and the ways these impact each other [l]. The investigation of human PC association is to decide by what means can make this PC innovation increasingly usable by individuals" (1998). Concurring the Carroll, "human PC association is the examination and practice of ease of use. It is tied in with comprehension and making programming and other innovation that individuals will need to utilize and will discover viable when utilized. Human PC communication now and then known as man-machine association, this idea was naturally spoken to with the developing innovation of PC, to make the human amicable, increasingly intuitive and proficient workplace with the machine. The idea of human PC communication additionally says that how human associates with the PC: not fundamentally the investigation of human, not basically the investigation of PC, it is the extension between them, which incorporates perception of communications among individuals and PCs. The explanation, actually, is clear most complex machines are useless except if they can be utilized appropriately by men. This idea thinks about numerous parts of human practices and should be valuable. In this way, in structure of human PC connection, the level of movement that includes a client with a machine ought to be altogether thought. The client movement has three unique levels; physical, psychological, and full of feeling.

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The physical angle decides the mechanics of collaboration between human what's more, PC while the psychological angle manages ways that clients can comprehend the framework and connect with it [2]. The full of feeling angle is a later issue and it attempts not just to make the connection a pleasurable encounter for the client yet in addition to influence the client such that make client keep on utilizing the machine by changing dispositions and feelings toward the client.

II. HCI ARCHITECTURE

Most important factor of a HCI design is its configuration. In fact, any given interface is generally defined by the number and diversity of inputs and outputs it provides. Architecture of a HCI system shows what these inputs and outputs are and how they work together. Following sections explain different configurations and designs upon which an interface is based.

A. Unimodal HCI systems

B. Multimodal HCI system

Unimodal HCI systems: - As mentioned earlier, an interface mainly relies on number and diversity of its inputs and outputs which are communication channels that enable users to interact with computer via this interface. Each of the different independent single channels is called a modality. A system that is based on only one modality is called unimodal. Based on the nature of different modalities, they can be divided into three categories:

Visual-based: The visual based human computer interaction is probably the most widespread area in HCI research. Considering the extent of applications and variety of open problems and approaches researchers tried to tackle different aspects of human responses which can be recognized as a visual signal. Some to the main research areas in this section are as follow:

- Facial Expression Analysis
- Body Movement Tracking (Large-scale)
- Gesture Recognition
- Gaze Detection (Eyes Movement Tracking)

Fig. 1: The Readable: a multitouch interface for playing music

Audio-based: The audio based interaction between a computer and a human is another important area of HCI systems. This area deals with information acquired by different audio signals. While the nature of audio signals may not be as variable as visual signals but the information gathered from audio signals can be more trustable, helpful, and in some cases unique providers of information. Research areas in this section can be divided to the following parts:

- Speech recognition
- Speaker recognition
- Auditory emotion analysis
- Human-made noise/sign detections (gasp, sigh, laugh, cry, etc.)
- Musical interaction

Fig. 2: Speaker recognition

Sensor-based: This section is a combination of variety of areas with a wide range of applications. The commonality of these different areas is that at least one physical sensor is used between user and machine to provide the interaction. These sensors as shown below can be very primitive or very sophisticated.

- Pen-based interaction
- Mouse & Keyboard
- Joysticks
- Motion tracking sensors and digitizers
- Pressure sensors
- Taste/smell sensors

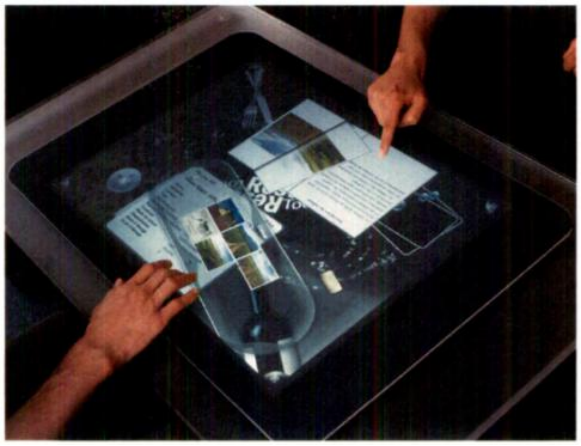

Fig. 3: Microsoft's 'Surface

Multimodal HCI systems: - The term multimodal refers to combination of multiple modalities. In MMHCI systems, these modalities mostly refer to the ways that the system responds to the inputs, i.e. communication channels. The definition of these channels is inherited from human types of communication which are basically his senses: sight, hearing, touch, smell, and taste. The possibilities for interaction with a machine include but are not limited to these types. A multimodal interface acts as a facilitator of human-computer interaction via two or more modes of input that go beyond the traditional keyboard and mouse. The exact number of supported input modes, their types and the way in which they work together may vary widely from one multimodal system to another.

III. PROPOSED METHODOLOGY

Central Processing Unit (CPU) concept of reversible architecture involves in an attempt to reduce the execution time. Type of microprocessor used for CPU is mostly Reduced Instruction Set Computers nowadays since they can execute instruction very fast because the instructions are so simple. Reversible CPU consisting of various components includes are as follows: Control Unit (CU), Arithmetic and Logical Unit (ALU), Register files and other important components such as Accumulator, Temporary Register, ALU Result Resister, Status Register, program Counter, Instruction Register etc. And the functional units like Main memory, Buses, and I/O. The data path and control unit perform the actual processing task using ALU. Control unit directs the operation within the processor based on the signal received from data path by directing I/O of the system. These signals control the data flow between the CPU and main memory and I/O. The most important feature of reversible CPU is to decode the information. Control unit retrieves the instruction from memory and carries out a sequence of operation required for ALU. It also fetches the instructions from the instruction registers, where an input to control logic comes from a reversible decoder. The decoder is the important block of a control unit which provides the information means an ability to execute one instruction per cycle. ALU is used to perform the arithmetic and logical operations of CPU on data contained in different registers. Each operation is carried out in sequence.

Reversible ALU contains submodules like the reversible adder, subtractor, multiplier etc., using reversible gates. Elements in ALU is implemented in a reversible manner with low power using VHDL (VHSIC-Hardware description Language) to reduce execution time. Basically, signals are communicated through memory unit.

Harvard architecture is used instead of Von Neumann, i.e program and data are accessed on separate buses as shown in the Figure 4. The main advantage of using Harvard architecture is that address and data buses are separate, so single clock cycle can perform both read and write operations. The memory access is done directly as well indirectly.

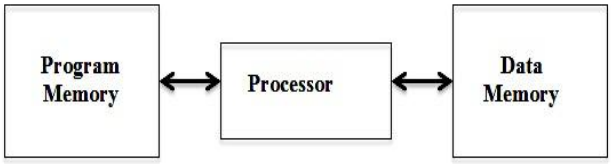

Fig. Error! No text of specified style in document.**: General Structure of Harvard Architecture**

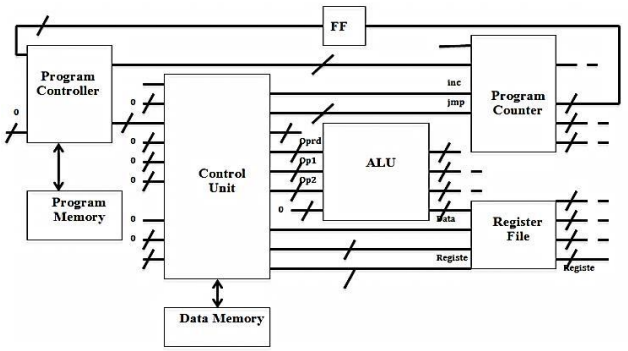

Fig. 5: A Review Block Diagram, Which We Have to Improve

In order to make the logic style for ease-of-use and simple, the design should be established in a way that it should be approachable and generalized.

- Design Constraints for Reversible Logic Circuits
- Reversible Logic circuits must have minimum gate levels
- Design should be optimized in way, to have minimum quantum cost
- Reversible Logic circuits should have minimum garbage output
- Reversible Logic circuits must contain minimum number of constant inputs
- A reversible logic must not allow fan-outs
- Design specification: Several results will be achieved to identify the different approaches and different search methods, based on which design specifications. Implementation algorithm is chosen carefully, in contrast, to reduce the designer's time and work

Flip flops are the basic memory element to store information in a register. By using, a search technique proposed a reversible D Flip-Flop (FF) instead of using JK flip flop with minimum design cost as compared to existing in [14]. The advantage of using D flip-flop over JK flip-flop is the simple structure that is input and out is identical and can be presented in one clock period. Mainly at the industry level in integrated circuit D flip-flops are selected by the manufacturer because of their good balance for power consumption, performance, efficient resource utilization.

One-Bit Memory Element

It is realized by using only one MG-1 gate. D flip-flop is a memory element which captures the value of the input at rising or falling edge when a clock is high. The characteristic equation for proposed D flip-flop is Q = Clk.D ⊕ Clk.Q. Proposed D flip-flop produces only one garbage output, has the quantum cost of 11.

IV. SIMULATION RESULT

Proposed reversible memory element for 1 bit D flip-flop is implemented using MG gate instead of JK flip-flop. And further one-bit memory element is cascading together to form 4- bit memory element. RTL schematic and output simulation waveform for cascaded memory element are represented in Fig. 6 and 7 respectively. The synchronous sequential design has zero inertial delays with an assumption. In a case of reversible design applying clock in a synchronous manner increases the cost. So it is better to consider each part of the delay. Firstly it will store a value at first flip-flop then in next clock pulse data will be shifted towards a right to the next flip-flop serially bit by bit and final output is captured at Q (Q3). A comparative study shows that the proposed design achieves the improvement of 26.21% in terms of quantum cost, 8.33% in terms of quantum depth and 25.39 % in terms of total cost for a 4-bit shift register. D- flip flop design achieved in our work sacrificing the Comparison of proposed an existing reversible memory element is tabulated in Table I.

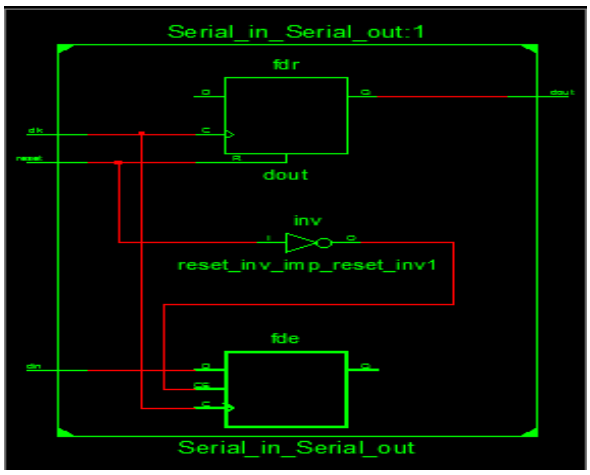

Fig. 6: RTL Schematic Diagram of Reversible Memory Element

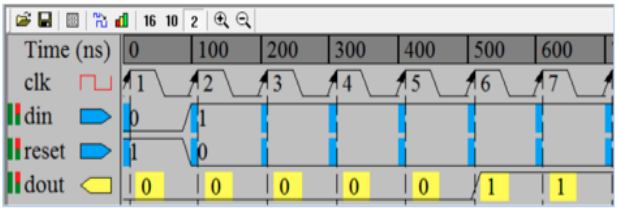

Fig. 7: Output Simulation Waveform Diagram of SISO Shift Register

Table I: Comparative Study of Various Parameters for Reversible Memory Element

Parameters	Quantum Cost	Garbage Output	Constant Input	Delay	Gate Count	Total Cost
Existing design	48	4	4	4	48	100
Proposed	44	4	4	4	44	92
Remarks	Best	No change	No change	Worst	No change	Best

Table II: Various Parameters for Reversible Comparator

Reversible Designs		Quantum Cost	Garbage Output	Constant Input	Delay	Gate Count	Total Cost	Power
Reversible Comparator	Existing	26	15	10	10	34	75	1992.2
	Proposed	10	2	3	10	10	22	1565.3

V. CONCLUSION

This thesis mainly focuses on a novel design of reversible processor components. Internal architecture components i.e., ALU, CU, register files and PC having better performance with proposed circuitry as compared to previous counterparts. Also, registers and the memory for program and data fall into the category of improved performance with reduced delay. Memory access pattern, execution, and complexity of instruction are kept in mind improve the execution time by using Harvard architecture instead of von Neumann. Power dissipation is also less about negligible since an overall system is designed using reversible nature of logics. With all above demonstration, using proposed designs improve the performance of CPU and execution time will be faster. Previously introduces methods and algorithm are used as the reference to realize the newly designed sequential circuitry. Various circuits are constructed with different approaches using a tight constraints algorithm while doing mathematical estimation for each parameter in parallel.

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