FPGA Based Accident Detection and Monitoring System for Safety Traffic

Fazal Noorbasha, K. D. M. Vikash Pani, K. Seetharam, S. Narendra

Abstract*: *In extremely inhabited countries like India, the population increases day by day because of this problem so many new types of the innovations are developed but in this project mainly focus on the automobiles. For industry reputation purpose car are made with high boost engines which is nearly speed equal to the trains. Due to this over speed so many accident will happen so many lives will lose. Even when the vehicle is travel in unpopular area if there is any accident happen it intimate to the relatives, hospitals and as well as the polis near by the location. In this project first it detects the output from the sensor and that sensor gives the disturbances happen in the directions of the vehicle. And this sensor make to communicate with the other people by using cross communication devices it particularly dedicated for the short range communication. Presently this technology is used in V2V communication .But in this project we mainly focus on the getting the location from the user devices to any other mobile number which are registered before. Major part of the paper we designed in the Verilog implementation whenever the input crosses the threshold voltage it automatically send the information to the user

Keywords: Verilog, Accelerometer, Accident detection, Test bench

I. INTRODUCTION

This paper is mainly locating the position whenever the accelerometer sensor input crosses the threshold voltages along in the any direction of the movement. If accident happens it sends the information to the registered numbers in the device. This uses a GPS to understand the precise position of the vehicle with associate degree accuracy of a couple of feet [1,2]. In this project we develop the code for the accident detection by using Xilinx vivado to develop the Verilog code. In this code we are writing the different types of modules in order to find whether the accident happen or not whenever the accident happen It send the location of the vehicle to the pre-programmed numbers. We verify the outputs for two wheeler, three wheeler and four wheeler vehicles. Based on the above parameters should be verified. Major part of the paper we designed in the Verilog implementation whenever the input crosses the threshold voltage it automatically send the information to the user. Due to latency we lose the lives of people to minimize this problem in this paper we accommodate user details based on the register number of the vehicle [3]. The position of the vehicle grab from the GPS sensor to send the location to the other people. In order to minimize the accidents happening on the roads. Hence the facilities provide to the people instantly to help the people without any delay. From this paper we develop the Verilog code to avoid the accident on the roads. Fig. 1 shows thee working model of accident detection system.

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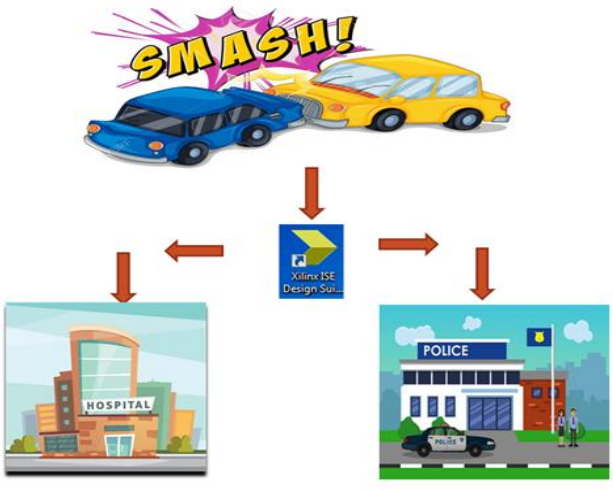

Fig. 1 working model of accident detection system

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II. SYSTEM BLOCK DIAGRAM

This paper is custom made for the heavily populated countries like India. Accident warning system is employed to avoid wasting the person‘s life by creating the medical facilities incoming in time. The conveyance trailing system will be utilized by the owner of the vehicle to trace the position of the vehicle and can also be utilized by the individuals in public transportation systems[4,5]. In this paper Xilinx acts as a bridge between the communications to the user. First create a new ISE project which will connect to the FPGA device on the Spartan-3e. To create the new project based on the application I have developed and create the design sources for the accident detection, vehicle type whether the vehicle is two wheeler, three wheeler and four wheeler in order to find the vehicle type we create the serial number for the each model of the vehicle and that serial number is synchronised with the vehicle tracked device. After the detecting the accident its information is sends to the programmed numbers. Based on the analysis of the measuring instrument sensing element is employed to observe any accident which can trigger a symbol just in case of accidents.

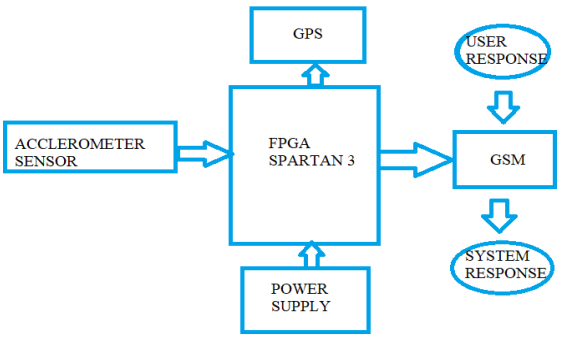

Fig. 2 Block diagram of FPGA based accident system

A. GSM Modem

Electronic equipment may be a specialized form of electronic equipment that accepts a SIM card, and operates over a subscription to a mobile operator, a bit like an itinerant. From the mobile operator perspective, a GSM electronic equipment appearance a bit likes an itinerant. A wireless modem behaves like a dial-up modem. The main distinction between them is that dial-up electronic equipment sends and receives knowledge through a set phone line whereas wireless electronic equipment sends and receives knowledge through radio waves[6].

A GSM electronic equipment are often Associate in Nursing external device or a laptop Card/ PCMCIA Card. Typically, Associate in Nursing external GSM electronic equipment is connected to a laptop through a serial cable or a USB cable. GSM electronic equipment within the variety of a laptop Card / PCMCIA Card is meant to be used with a laptop computer. It ought to be inserted into one in all the laptop Card / PCMCIA Card slots of a laptop computer. Like a GSM itinerant, GSM electronic equipment needs a SIM card from a wireless carrier so as to control. Both SIM300 modems and dial-up modems support a standard set of ordinary commands.

B. GPS

The Global Positioning System (GPS) is a space-based global navigation satellite system (GNSS) that provides reliable location and time information in all weather and at all times and anywhere on or close to the world once Associate in Nursing wherever there's an clear line of sight to four or additional GPS satellites. The position is then displayed, perhaps with a moving map display or latitude and longitude; elevation information may be included [7]. Many GPS units show derived data like direction and speed, calculated from position changes.

C. FPGA

Verilog is a hardware description language (HDL) used to model electronic systems in the semiconductor and electronic design industry. Verilog HDL, not to be confused with VHDL (a rival language), is most commonly used in designing, checking and implementing digital logic chips at the abstraction stage of register transfer. It is also used in analog and mixed-signal circuit testing.

Generally hardware systems for FPGAs are designed using Hardware Descriptive Languages (HDL) such as Verilog, System Verilog and VHDL (HDLs are considered as low level languages). As the name suggests, you can describe hardware (digital electronic circuits) using HDLs. But to design hardware on FPGAs using HDLs require digital electronics knowledge. High Level Synthesis was introduced to minimize the electronics knowledge required to design hardware. It also makes the hardware design flow easier when it comes to achieving a certain behavioural model required by the hardware without worrying to much about the electronics underneath. When you developed HLS synthesis can be used general programming languages like C, C++. From this tool we developed the HLS code which is very efficient it is also calculated the power required for the development for this device. And tells about the different parameter that is effected by the outside environment. Also it gives the details information about the I/O ports, LUT’s count.

In this project we are using this vivado tool. The Vivado Design Suite of any version supports an IP-centric design flow that helps you easily modified designs and synthesis into reusable IP. The Vivado IP Catalogue is a fuse IP store that provides the framework for the IP-centric design algorithm. This catalogue contains IP from all sources including Xilinx IP, third-party IP, and end-user designs targeted for reuse as IP into a single environment. The Vivado IP packager tool is a unique design reuse feature, which is based upon the IP-XACT standard. The IP packager tool provides you with the ability to package a design at any stage of the design flow and deploy the core as system-level IP.

D. Accelerometer Sensor

we are using the accelerometer sensor to detect the accident happen or not in this particular value we can fix the threshold voltages of the vehicle in different roads we are considering all hazardous conditions to sense the disturbance along the three axis[9]. If the value is cross over the respective axis values to sends the all details to the FPGA. From FPGA we are sending the all information related to that accident

III. IMPLEMENTATION

In this schematic we are enabling the circuit if the accident detection input attains the value high only it proceed for the another module.

In the second module we are enabling the location based on the input accident detection from the accelerometer sensor. Particularly grabbing the location we are using the SIM 300 sensor which is connected to the FPGA board. After completion of this module we are moving on to the vehicle type based on the serial number which type of the vehicle is subjected to the accident in which location to gathering the all details regarding about the accident and send the information to the registered contacts. Fig. 3 shows the FPGA schematic in view of system.

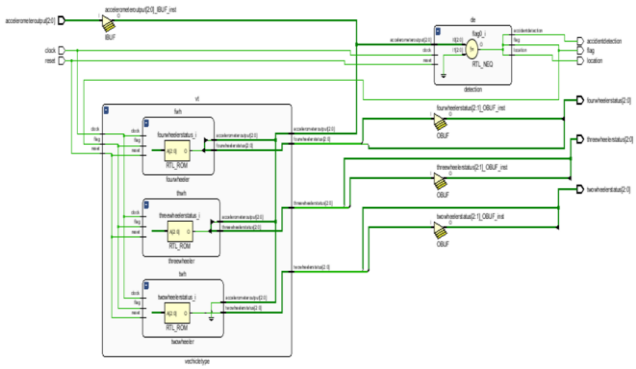

Fig. 3 FPGA schematic in view of system

IV. RESULT AND DISCUSSION

From Fig. 4 we can identify a waveform generator for the variable accident detection that means an accident occurred. Since the occurrence of the accident is true the type of vehicle, vehicle number and the location of the vehicle will be fetched. Location also detected whenever the accident detection is observed by the sensors which are accommodate to the vehicle.

Fig. 4 Type of vehicle and accident detection

By using Xilinx vivado a comparator is designed with two inputs one is reference inputs and other is the output of the system if the both the inputs are equal and indicates that accident occurred. Then the latch will be enabling. when the latch is enable it will send the message which consists the following details type of vehicle that is either two wheeler or three wheeler or four wheeler ,vehicle number and the location. The entire system is designed by using Verilog code and it is compiled with test bench in Xilinx vivado. We can infer from the figure3 there is no signal generated which indicates no accident occurred.

V. CONCLUSION

In this paper we had designed FPGA based accident detection and monitoring system using the Verilog HDL. The accident information is automatically sent to the pre-programmed contacts. Based on the details immediate action is takes place from the hospitals as well as the police. After detecting the accident it automatically sends the information to the contacts with latitude and longitude position. This system gives information in different modules in order to determine the accident location, vehicle type and details about the owner of the vehicle. Based on the serial number to assign for the vehicle it also detects the type of the vehicle based on the type we need to know how many people are injured due to the accident can also be detected by using the project.

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AUTHORS PROFILE

Fazal Noorbasha was born on 29th April 1982, Vedullapalli, Bapatla, Guntur, Andhra Pradesh, India. He received his, B.Sc. (Electronics) Degree in Physical Sciences from BCAS College, Bapatla, Affiliated to the Acharya Nagarjuna University, Guntur, Andhra Pradesh, India, in 2003, M.Sc. Degree in Electronics Sciences from the Dr. HariSingh Gour Central University, Sagar, Madhya

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